NREL/TP-413-5334 • UC Category: 273 • DE93000078

NREL/TP--413-5334

DE93 000078

Non-H_2Se, Ultra-Thin CIS Devices

Annual Subcontract Report
10 March 1992 – 9 November 1992

A. E. Delahoy, J. Britt, Z. Kiss
Energy Photovoltaics, Inc.
Princeton, New Jersey

NREL technical monitor: H.S. Ullal

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A Division of Midwest Research Institute
Operated for the U.S. Department of Energy
under Contract No. DE-AC02-83CH10093

Prepared under Subcontract No. XG-2-12051-1

February 1993

NOTICE

Printed in the United States of America
Available from:
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

Price: Microfiche A01
Printed Copy A04

Codes are used for pricing all publications. The code is determined by the number of pages in the publication. Information pertaining to the pricing codes can be found in the current issue of the following publications which are generally available in most libraries: *Energy Research Abstracts (ERA)*; *Government Reports Announcements* and Index (*GRA* and I); *Scientific and Technical Abstract Reports (STAR)*; and publication NTIS-PR-360 available from NTIS at the above address.

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EXECUTIVE SUMMARY

Energy Photovoltaics (EPV), Inc. began a 3-phase, cost-shared contract on March 10, 1992 with the objective of demonstrating 12% total area efficiency copper indium diselenide (CIS) solar cells and 50 W CIS modules averaging at least 8 W/ft^2. At the end of Phase I (duration 8 months) EPV delivered to NREL a 1.1 cm^2 CIS cell with an active area efficiency of 10.5%.

The CIS was prepared by selenization of appropriately treated Cu-In layers using elemental selenium. This process, developed by EPV, is self-stabilizing, and does not involve the highly toxic gas hydrogen selenide. The Cu and In layers were deposited in a load-locked magnetron sputtering system.

Heat treatment of the Cu-In precursors was shown by x-ray diffraction to change the dominant intermetallic compound from $CuIn_2$ to $Cu_{11}In_9$. Following selenization, the relationship between resulting CIS thickness and initial total thicknesses of the Cu and In layers was examined.

The CIS films were further analyzed by x-ray diffraction and electron microprobe. Single phase, polycrystalline $CuInSe_2$ was generally obtained, with the ordered chalcopyrite structure being observed. It appeared to be a possibility that grains with the disordered sphalerite structure were also present. The film composition was frequently observed to be of the form $Cu_{1-\delta}In_{1+\delta}Se_{2+\delta}$ with δ ranging from 0.02 to 0.16. In strongly In-rich films the compound $CuIn_2Se_{3.5}$ was detected.

Devices of the form ZnO:Al/CdS/CIS/Mo/soda lime glass substrate were fabricated and analyzed. Chemical bath deposition (CBD) of the CdS window layer using the acetate salts was found to result in more reproducible junctions and gave higher short-circuit current densities than did vacuum evaporation of the CdS. A high resistivity/low resistivity bi-layer was employed for the ZnO transparent conductor, and deposition conditions were optimized to give a sheet resistance of about 20Ω/sq. for 1μm films while maintaining 90% white light transmission.

A careful study of the effect of Cu/In ratio in both precursors and CIS films on device performance was completed. This showed an approximate plateau in conversion efficiency for CIS Cu/In ratios in the range 0.89-0.83, with a very strong decline in the range 0.83-74. In the plateau region a ±6% variation in precursor Cu/In ratio resulted in a ±3% variation in cell efficiency, supporting the claim that the selenization process is self-stabilizing.

Optimization of the selenization rate/temperature/time profile and CBD CdS layer, together with careful device engineering, resulted in a 10.5% active area efficiency CIS solar cell. The parameters of this cell are summarized in Table 1.

Table 1 Parameters for CIS cell delivered to NREL

Cell #	V_{oc} (mV)	I_{sc} (mA)	FF (%)	Active area (cm^2)	Active area efficiency (%)
11-11-1-6-3C	441	39.6	66.0	1.10	10.5

Scale-up of the CBD CdS and sputtered ZnO was accomplished, thereby allowing fabrication of 30.5 x 30.5 cm^2 (1 ft^2) modules. Patterning of the Mo was successfully performed using both chemical etching and laser techniques. Mechanical scribing was employed for the CIS and ZnO isolation scribes. The 1 ft^2 modules consist of 55 serially-interconnected cells, 0.5 cm in width.

An active area efficiency of 5.6% was achieved for a 15 cell, 30 cm^2 module. A V_{oc} map showed good uniformity of response for all cells. Fill factor limitations due to interconnect resistance were observed, and work is underway to identify and rectify the various problems.

Efforts in Phase II will focus on further improvement of CIS material quality and total area cell efficiency, more uniform selenization, the production of efficient 1 ft^2 modules based on uniform material layers and high quality interconnects, and scale up of deposition equipment to allow CIS formation on 0.5 x 1.25 m^2 substrates.

SECTION 1.0
INTRODUCTION

The market for photovoltaic modules continues to rise. Traditionally, modules based on crystalline or polycrystalline silicon wafers have filled this need. In the future, however, modules based on thin film materials will capture a significant market share by virtue of their lower manufacturing cost. The first generation thin film material, amorphous silicon, has been shown to be readily manufacturable, but is currently hampered by a relatively low stabilized power density. Second generation thin film modules are now under intensive development, and are generally based on polycrystalline compound semiconductors such as copper indium diselenide ($CuInSe_2$/CIS) or cadmium telluride (CdTe). CIS modules have been reported that produce power densities of 100 W/m^2 [1], but these modules appear to have been fabricated using the highly toxic gas hydrogen selenide (H_2Se).

The overall objective of this subcontract is to develop techniques capable of producing efficient, large area $CuInSe_2$ - based PV modules in a manner consistent with the demands of a manufacturing process, namely with good control, high yield, high material utilization, and with safety. A particular objective is the demonstration of a 50W CIS module.

EPV intends to realize the above objectives using an all-vacuum approach for material deposition. The CIS is produced using a process developed at EPV, namely selenization of appropriate precursors using elemental selenium and not H_2Se [2].

A useful review of earlier work in the field is given by Zweibel and Mitchell [3] while recent advances are described by Ullal et al. in [4].

SECTION 2.0
CIS PREPARATION AND ANALYSIS

2.1 DESCRIPTION OF PROCESS

The process developed at EPV for the formation of $CuInSe_2$ (CIS) involves the selenization using elemental selenium of appropriately prepared, sputtered Cu-In layers. The selenium is evaporated according to a proprietary Se rate/substrate temperature/time profile.

At the present stage of development 30.5 cm x 30.5 cm (1 foot square) soda lime glass substrates are employed. Following cleaning, the glass is loaded into a cryo-pumped, load-locked magnetron sputtering system and is translated sequentially past Mo, Cu, and In cathodes. A molybdenum layer is deposited to a thickness of about 0.5 μm, and serves as a back contact for subsequently prepared CIS devices. The glass cleaning process and Mo sputtering conditions employed result in good adhesion of the Mo to the glass. Next, a copper-indium stack of the form $\Sigma_i Cu_{xi} In_{yi}$ is deposited under controlled conditions and with specific gradients. Considerations regarding the number and thicknesses of these layers are discussed in Section 2.2. The desired thickness of each layer is obtained through choice of substrate scan speed and sputtering power.

After deposition of the metal layers the glass substrate is removed from the sputtering system and placed in the selenization chamber. The Cu-In stack is annealed in vacuo at a temperature T_1 in the range 100 - 175°C to promote reaction of the Cu and In layers to form desirable Cu-In intermetallic compounds. The resulting Cu-In layer is referred to as the precursor layer. A small amount of selenium is initially evaporated onto the precursor while the substrate is still at temperature T_1 and selenization is completed during a temperature excursion between T_1 and T_2 (where T_2 is in the range 400 - 500°C) according to EPV's Se rate/temperature/time profile. The resulting film is

polycrystalline $CuInSe_2$ having a grain size of about 1μm and a band gap of 1.0 eV. The thickness of the CIS layer is generally chosen to be in the range 1 - 2 μm and is controlled by the total thickness of the Cu layers in the Cu-In stack.

Device fabrication next requires the formation of a semiconductor heterojunction. This is accomplished by deposition of an n-type, wide band-gap window layer such as CdS (band gap 2.4 eV) onto the p-type CIS. To reduce the surface resistance of the device, a thick (2 μm) conductive layer of In-doped CdS can be used. However, to reduce the (already small) cadmium level in devices, and to improve their short wavelength response, EPV has chosen to use a thin (ca. 300A) undoped CdS layer overcoated with a transparent conductor such as Al-doped ZnO (band gap 3.3 eV). The basic device structure is thus of the form glass/Mo/CIS/CdS/ZnO:Al.

2.2 PRECURSOR FORMATION AND TREATMENT

2.2.1 Number and Thickness of Layers

If we imagine stoichiometric $CuInSe_2$ to be formed by reacting three separate layers of Cu, In, and Se, then we may calculate the required thickness ratios of these layers as follows. Since the number of Cu atoms is equal to the number of In atoms, we have

$$(pt/M)_{Cu} = (pt/M)_{In} \qquad (1)$$

where p (Greek rho), t, and M are respectively density, thickness, and molecular weight. This gives for the In/Cu thickness ratio

$$t_{In}/t_{Cu} = 2.21 \qquad (2)$$

For the Se/Cu thickness ratio we have $(pt/M)_{Cu} = 1/2\ (pt/M)_{Se}$, and this gives

$$t_{Se}/t_{Cu} = 4.6 - 5.2 \qquad (3)$$

depending on the assumed Se form, and hence density. Finally, from the masses of the individual layers, we have

$$(pt)_{Cu} + (pt)_{In} + (pt)_{Se} = (pt)_{CIS} \quad (4)$$

and this equation predicts a definite relationship between CIS thickness and copper layer thickness, namely

$$t_{CIS}/t_{Cu} = 8.2 \quad (5)$$

As an example, the following separate layers of Cu, In, and Se contain the appropriate numbers of atoms to form 1.64 μm of CIS:

2000 A Cu
4420 A In $\rightarrow\rightarrow$ 1.64 μm CIS
9280 A Se

Preparation of the precursor requires the deposition of a Cu/In/Cu/In... stack with appropriate thicknesses of the Cu and In sublayers. If no Cu or In were to be lost from the layer during selenization, then we see from the paragraph above that the ratio of the total In sublayer thickness to the total Cu sublayer thickness should be 2.2 in order to obtain stoichiometric CIS. Similarly, the measured CIS thickness should be 8.2 times the total Cu sublayer thickness.

The optimal number of sublayers is a matter for experiment. For example, it might be anticipated that the number of sublayers would affect the homogeneity of the reacted Cu-In layers. Yet it has been our general experience that the nature of the reacted Cu-In layer (precursor) exerts a profound influence on the subsequent selenized film (see also sections 2.2.2 and 2.3.2). It has also been reported that co-deposited precursors have given superior device performance compared to sequentially deposited precursors [5]. Regarding the number of sublayers, our experiments have

covered the range of from 1 to 6 Cu and In sublayers in the Cu-In stack (2-12 layers total), sometimes with and sometimes without a gradient in the Cu/In ratio throughout the stack.

2.2.2 Effect of Annealing

We have made two important observations regarding the Cu-In layers. First, that the Cu-In layers have to be annealed at a temperature of about 150°C prior to selenization in order to obtain good devices from the resulting CIS. And second, that a permanent visual change in the Cu-In layers becomes apparent at a critical temperature of about 142°C. This is lower than the melting point of bulk indium (156.6°C).

The critical temperature was determined by slowly heating on a hotplate a 30 cm long soda lime glass substrate coated with standard Mo and 6 alternating sublayers of Cu and In (see Figure 2.1). A growing patch with a discernibly changed appearance was observed as the substrate heated up. A demarcation zone about 2 mm in width existed around the perimeter of the patch. The inner boundary of the demarcation zone was considerably more distinct than the outer boundary. The temperature of a planar, thin film Pt resistance thermometer held in thermal contact with the film with silicone grease was determined to be 142°C as the demarcation zone crossed the thin film element. (At a temperature of 137°C the demarcation zone had not reached the element and at 147°C it had passed the element entirely). After exceeding 142°C the precursor film became shiny, less scattering, more uniform in appearance, and mechanically softer. These properties were preserved upon cooling to room temperature. The finite width of the demarcation zone suggests that the transformation of the Cu-In layers is only partial until the inner boundary is reached.

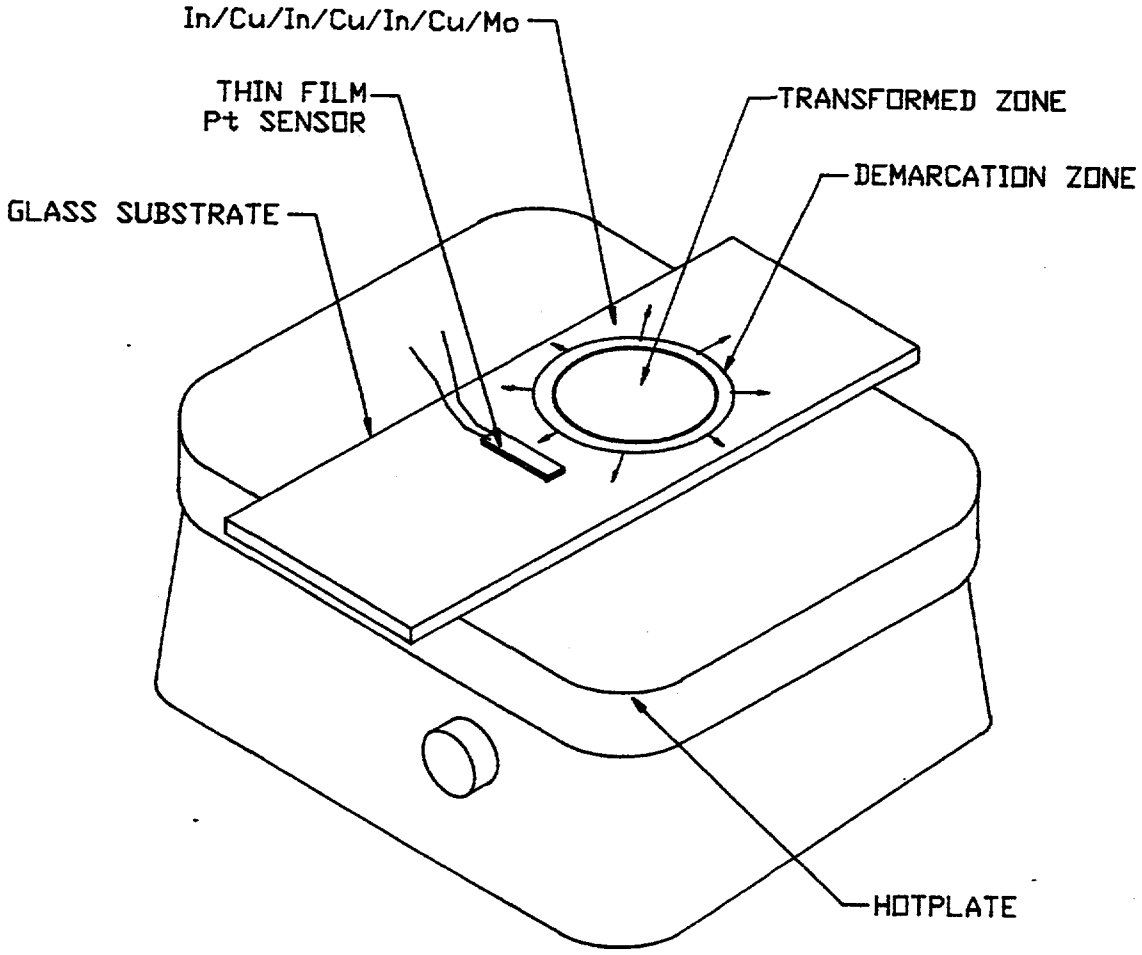


Figure 2.1 Determination of the critical annealing temperature for the $(Cu-In)_3$ precursor

We also found that a typical $(Cu-In)_3$ stack increases in thickness upon annealing above the critical temperature. In the as-deposited state a thickness of 5325 A was measured, while after annealing the thickness was 6500 A, a 22% expansion.

2.2.3 X-ray Diffraction Analysis of Precursors

The observation that the Cu-In stack requires annealing (see Section 2.2.2 above) led us to explore the nature of both the as-deposited and annealed precursors by x-ray diffraction. The as-deposited $(Cu-In)_3$ stack had a spectrum of diffraction peaks which could be interpreted as one strong peak due to Mo (at $2\theta = 40.3°$) and the remainder entirely due to the intermetallic compound $CuIn_2$ (34.4°, 43.0°, 43.2°, 38.5°). There were no sets of peaks corresponding to free Cu or In. After two months at room temperature there were essentially no changes in the x-ray diffraction pattern of the sample. Part of this spectrum is shown as the lowest curve in Figure 2.2a.

The sample was then heated in air at 100°C for 30 minutes and the spectrum re-measured. There was a slight decrease in the intensity of the $CuIn_2$ spectrum and two new diffraction peaks at $2\theta = 29.6°$ and 42.3° appeared. This is shown in the middle curve of Figure 2.2a. After heating in air to 150°C for 20 minutes the $CuIn_2$ spectrum disappeared and a spectrum of new lines at $2\theta = 29.7°$, 33.0°, 42.3°, and 54.5°, appeared. This spectrum is shown as the uppermost curve in Figure 2.2a and was identified as being due to the compound $Cu_{11}In_9$. This dramatic change from $CuIn_2$ to $Cu_{11}In_9$ after heating to 150°C can be seen more clearly on the expanded scale of Figure 2.2b, which shows the spectra after heating to 100°C and 150°C, respectively. Broadly similar conclusions (with slight differences in detail) were reached by Kessler et al. [6].

We have also examined by x-ray diffraction a $(Cu-In)_3$ precursor film subjected to interrupted selenization. In this experiment the standard selenization sequence shown in Figure 2.6

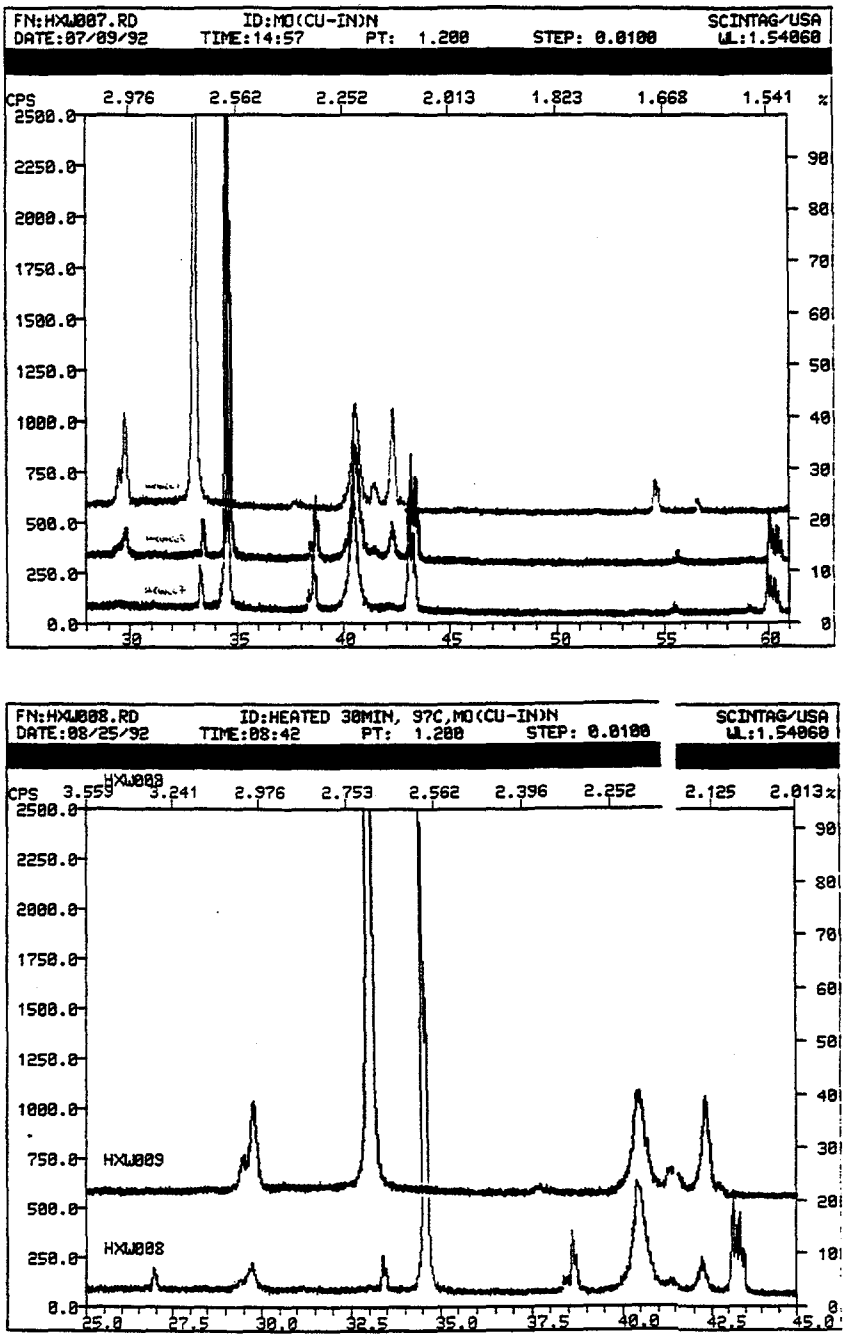


Figure 2.2 X-ray diffraction spectra for a $(Cu-In)_3$ stack on Mo-coated glass before and after heating.
Fig a. lower curve: as-deposited
middle curve: after heating to 100°C (30 min.)
upper curve: after heating to 150°C (20 min.)
Fig b. middle and upper curves of Figure a with expanded scale.

was followed until a substrate temperature in the range 200 - 225°C was reached, at which point the Se source was turned off and the substrate allowed to cool. The x-ray diffraction pattern consisted of the strong Mo line at 40.5° together with the four prominent peaks due to $Cu_{11}In_9$. No other diffraction peaks were found, and in particular, the strong (112) peak of $CuInSe_2$ was not observed. Further experiments are planned to determine the temperature at which $CuInSe_2$ appears.

2.2.4 Deviations from Ideality

We have assumed in the sections above that the Cu and In layers are of constant thickness across the substrate. In practice, both short range variations in thickness (i.e. roughness) and long range variations in thickness (i.e. gradients) are encountered. We have also observed a continual (long-term) drift in the In deposition rate for apparently fixed sputtering conditions. This presumably results from erosion of the In target. Because of the dependence of CIS composition on the In/Cu ratio in the precursor, both thickness gradients and rate drifts are potentially troublesome issues.

A discontinuous change in In deposition rate was also noticed upon replacement of the In sputtering target. Given these changes in In rate, the task of optimizing the In/Cu ratio in the precursor was considerably ameliorated by the in-house development of a sensitive stylus profilometer for thickness measurement. This profilometer was cross-calibrated against a commercial Tencor machine and associated standards.

Because of the low melting point of In, it was found important to control the substrate temperature prior to In deposition, and to limit the temperature rise of both the substrate and In target during deposition. While the Mo and Cu films were found to be smooth, the In films exhibited considerable surface roughness. These local variations in thickness are evident in the profilometer trace shown in Figure 2.3a. The magnitude of these variations is

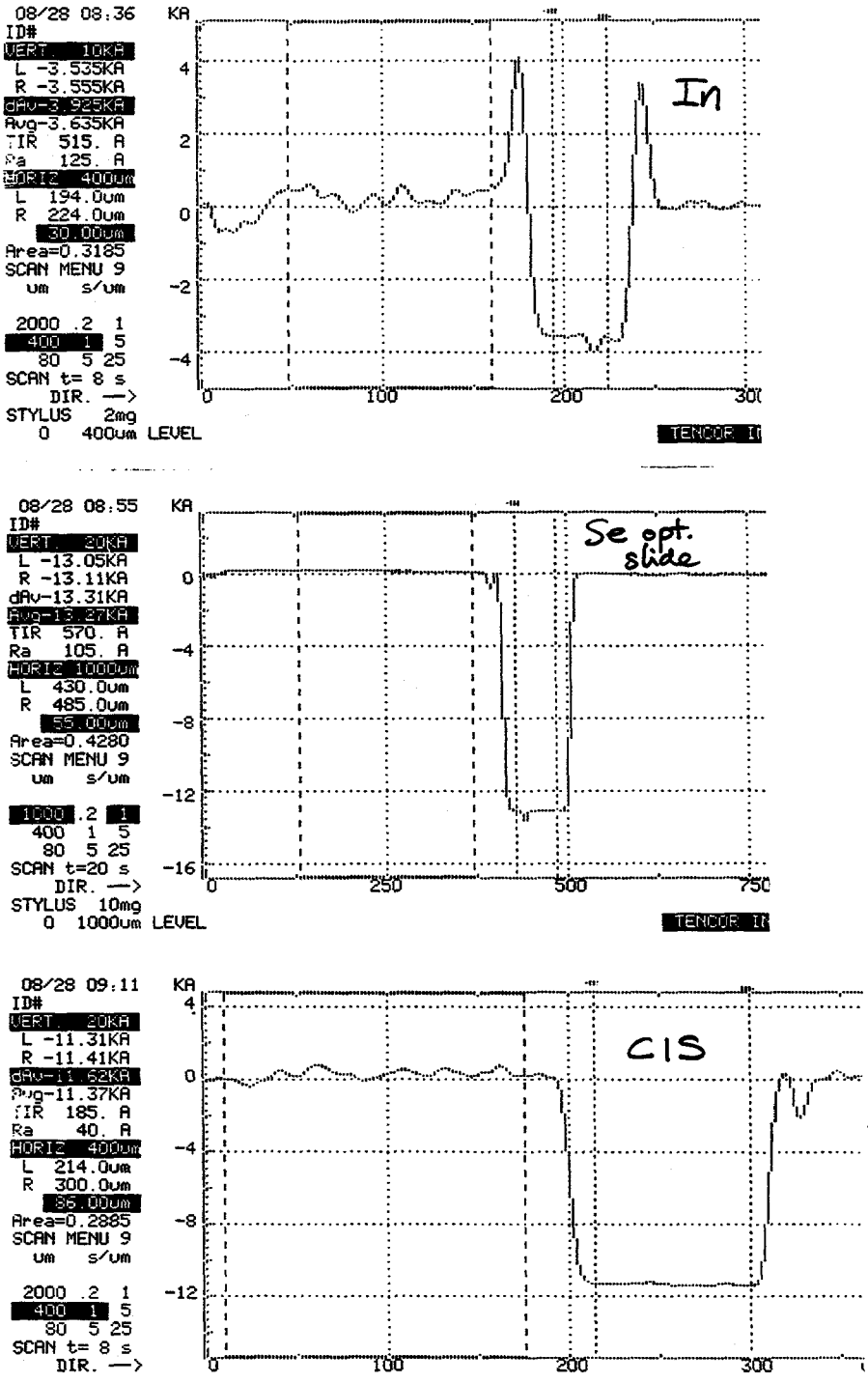


Figure 2.3 Stylus profilometer traces for In, Se, and CIS films of their surfaces and of an inscription made down to the glass surface

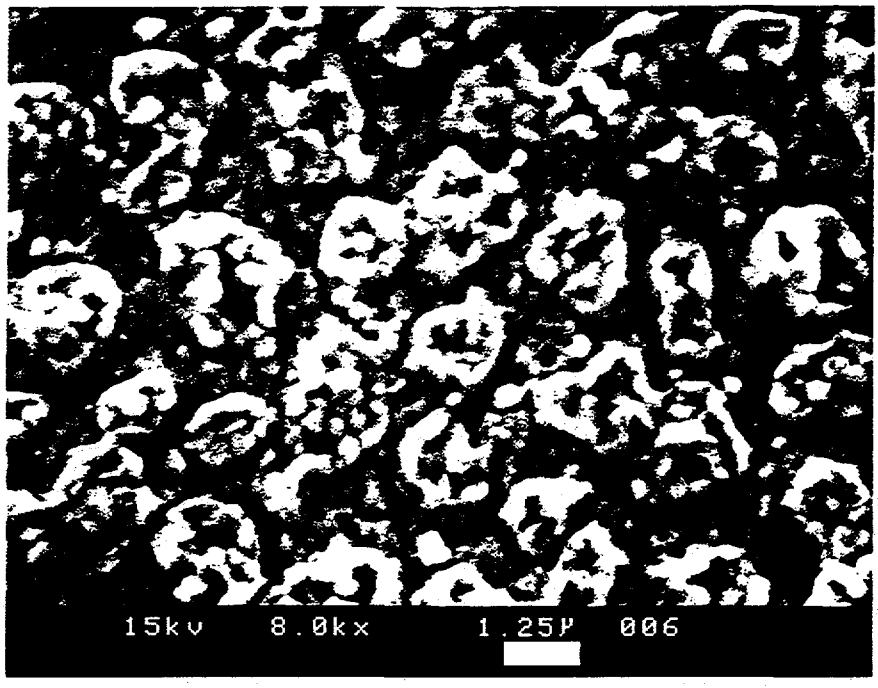


Figure 2.4 SEM micrograph of as-deposited $(Cu-In)_3$ stack

about 15% of the film thickness, with a length scale of about 15 - 40 μm.

As shown in Figure 2.3c, the CIS films also exhibit surface roughness (about 7.5% of the film thickness) over a similar length scale. On the other hand, both the Cu and Se films are perfectly smooth (see, for example, Figure 2.3b). As is evident from the SEM micrograph of Figure 2.4, the uniformity of a typical as-deposited $(Cu-In)_3$ stack leaves much to be desired. Although the In roughness plausibly accounts for the observed CIS roughness, we have not yet studied whether this is the sole cause, nor have we examined the potentially important question of to what degree initial variations in In thickness might cause inhomogeneities in the annealed Cu-In precursor and, ultimately, local variations in CIS composition.

Thickness gradients in the metal layers have been detected by profiling diagnostic samples cut from 30 x 30 cm^2 substrates. For both Mo and Cu films the thickness variation is confined to a range of $\pm$ 5% about the mean thickness.

The experimentally determined ratio of CIS thickness to total Cu layer thickness frequently appears to be larger than the ideal ratio (8.2) calculated above. This data is discussed in Section 2.3.2.

2.3 SELENIZATION USING ELEMENTAL SELENIUM

The equipment used for the vacuum selenization process developed by EPV using elemental selenium is shown schematically in Figure 2.5. A 30 x 30 cm^2 glass substrate, coated with the as-deposited Mo, Cu, and In layers, is mounted on a rotatable platform and can be radiatively heated to temperatures up to 550°C. The selenium is evaporated from a carbon crucible, and the optical sensors D_1 and D_2 monitor the thickness of the deposited selenium and material re-emitted from the substrate. (The melting point of selenium is 217°C, and at 240°C its vapor pressure is 10^{-2} Torr).

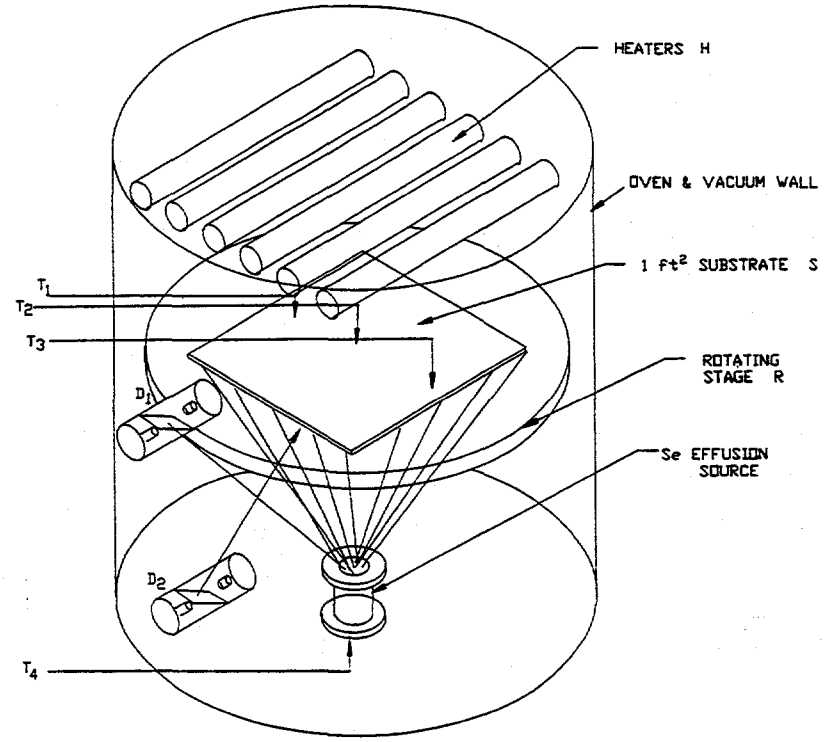


Figure 2.5 Schematic of selenization equipment used in Phase I for 30 x 30 cm² substrates, with optical monitoring of Se fluxes

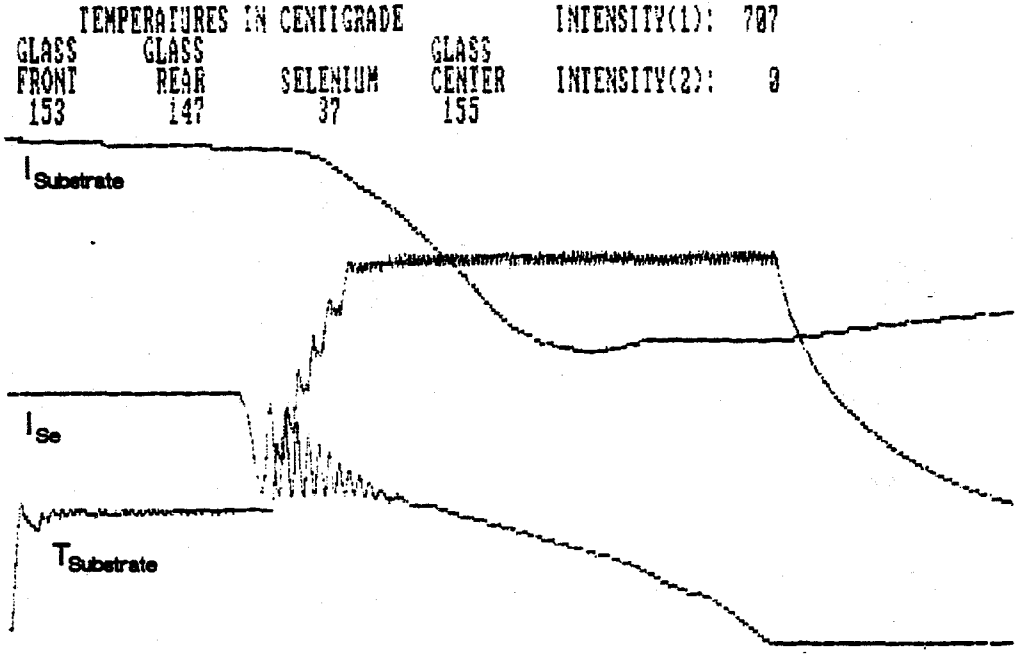


Figure 2.6 Computerized process monitoring during selenization showing substrate temperature, incident Se flux, and re-emitted material flux versus time

The outputs from the optical sensors and relevant thermocouples are recorded by computer.

2.3.1 Rate/temperature/time Profile

A qualitative description of the selenization process is as follows. The Cu-In stack is first annealed in vacuo at about 150°C to promote formation of the appropriate Cu-In precursor compound. This step can be seen in Figure 2.6 which is a computer printout of the substrate temperature and output of the two optical detectors during a typical selenization run. The precursor is then exposed to Se while it is still at 150°C, and after a predetermined amount of Se is deposited the substrate temperature is ramped to the range 430 - 500°C. At least half of the Se is evaporated by this point, as can be seen by counting the fringes obtained from the Se sensor D_1. The substrate is maintained at this temperature in an atmosphere of Se, and then cooled.

A detailed understanding of the selenization process has not yet been reached. In the EPV process, the Se deposition rate is an important variable, and the substrate temperature profile is carefully adjusted to match this rate. It is also important not to heat the Cu-In stack to too high a temperature before the introduction of selenium to prevent compositional segregation. An excess of indium in the precursor is required, even beyond what is required to produce slightly Cu-poor device-quality CIS films. This implies In loss from the film during selenization, presumably in the form of a volatile indium selenide such as In_2Se. An excess of Se beyond what is required for stoichiometric CIS is also required by the selenization process. Although we have not verified this, it is possible that an increased Se flux may inhibit In loss by favoring the formation of stable In_2Se_3. Excess Se is both reflected and re-emitted from the hot CIS, and this re-emitted Se flux is detected by the second optical sensor (D_2) in Figure 2.5.

It is generally thought that selenization proceeds by

formation of intermediate Cu and In selenides (e.g. $Cu_{2-x}Se$, InSe) followed by their interdiffusion and reaction to form $CuInSe_2$ [7-9]. Evidence for such interdiffusion has been presented by Dimmler et al. [7]. These notions also suggest the possibility of employing Cu and/or In selenides directly as the precursor layer.

2.3.2 Film Thickness Studies

We have made preliminary studies of the thicknesses of the individual Cu, In, and Se layers employed and the resulting CIS thickness. The results of a careful study made early in this program are shown in Table 2.1, including results for Mo and evaporated CdS.

Table 2.1 Summary of Constituent Film Thicknesses Employed in Early Devices

Material	No. of Sublayers	Total Thickness	Surface Roughness
Mo	3	1850 A	-
Cu	3	1200 A	-
In	3	3920 A	600 A
Se	1	1.15 μm	-
Se (monitor)	1	1.33 μm (11.5 fringes)	
CdS	1	2930 A	-
CIS	3 + 3 + 1	1.02 - 1.16 μm	900 A

In this study the Cu-In stack employed for the precursor consisted of a total of 6 sublayers, namely Cu(90)/In(36)/Cu(90)/In(18)/Cu(90)/In(24), where the numbers in

parentheses refer to the scan speed in cm/min of the substrate past the pertinent cathode. In separate depositions the 3 Cu sublayers were put down successively, as were the 3 In sublayers. These films proved to be 1200 A and 3920 A in thickness, respectively. This gives an actual In/Cu thickness ratio of 3.3, in contrast to the theoretical figure of 2.2 required for $CuInSe_2$ calculated in Section 2.2.1. After selenization of the precursor, during which 12 fringes were recorded for the Se, the resulting CIS film was found to have a thickness in the range 1.02 - 1.16 μm. This gives a CIS/Cu thickness ratio of about 9.1, compared to the expected value of 8.2 (see Section 2.2.1). In a separate selenium evaporation, 11.5 fringes were recorded, corresponding to 1.33 μm Se on the Se optical slide and 1.15 μm on the substrate. This implies that the evaporated Se/Cu thickness ratio is about 10, i.e. a factor of two higher than that required to form $CuInSe_2$.

More recent data yielded a CIS thickness of about 1.65 μm for a non-graded $(Cu/In)_3$ precursor, while measurement of separate Cu and In depositions (3 sublayers each) implied total Cu and In precursor thicknesses of 0.143 μm and 0.443 μm, respectively, when scaled to the appropriate scan speeds. These numbers imply thickness ratios of 11.5 for CIS/Cu, and 3.1 for In/Cu. The CIS/Cu ratio is higher than expected, and may be indicative of a residual indium selenide phase.

For constant total Cu thickness in the Cu-In stack, the thickness of the CIS is found to depend on the total In thickness employed. These data are shown in Figure 2.7 in which CIS thickness is plotted aganinst substrate scan speed past the In target.

For the selenium evaporation, significant non-uniformities are observed in the thickness of a deposited layer due to the point-source nature of the existing source. These data are shown in Figure 2.8, in which variations in thickness of $\pm$ 0.2 μm are evident in a nominal 1 μm Se layer deposited on a stationary 1 ft^2 substrate. Although these variations are not believed to be a

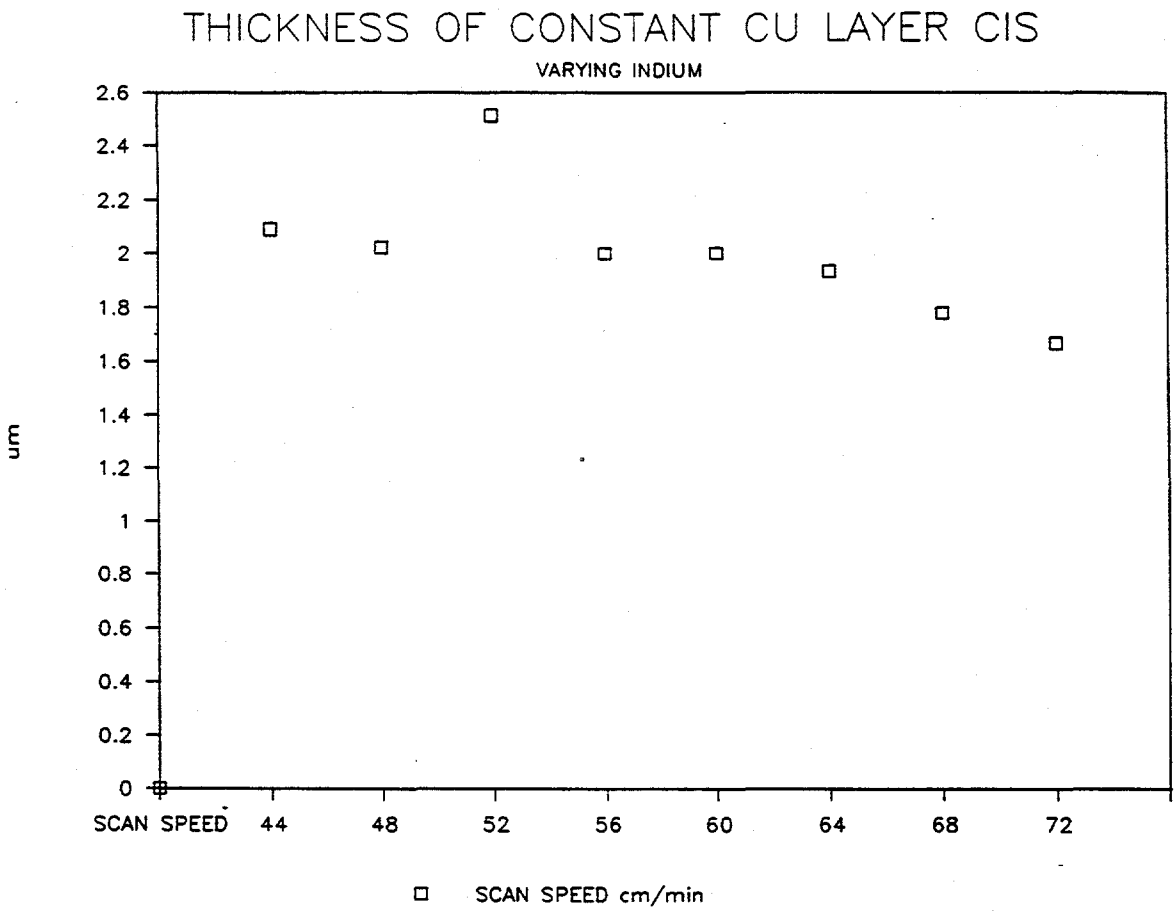


Figure 2.7 Dependence of CIS thickness on scan speed for In with Cu thickness held constant

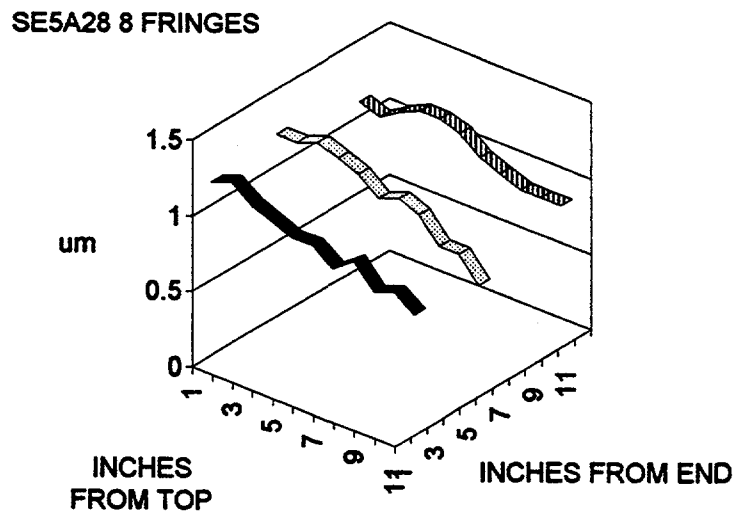


Figure 2.8 Variation of selenium thickness across a 1 ft² plate

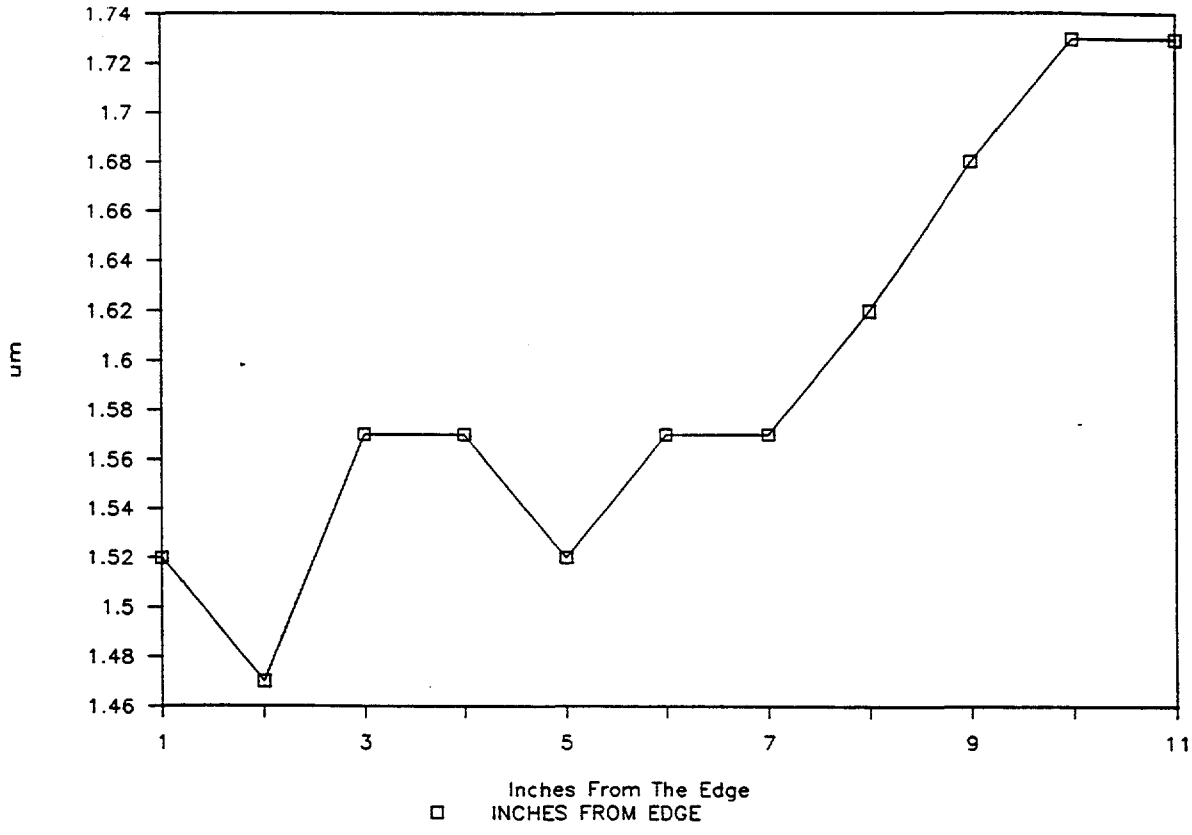


Figure 2.9 Gradient in CIS thickness across a 1 ft² plate

serious problem (provided an excess of Se is always present), an entirely new selenization system has been built to allow more uniform selenization and better Se utilization (see Section 4.1.3).

As would be expected, the gradient in CIS thickness across a 1 ft^2 plate is more modest, a variation of $\pm$ 0.12 μm being observed for a 1.6 μm layer (see Figure 2.9). Further studies are necessary to more clearly correlate gradients in CIS thickness to gradients in Cu and In layers, substrate temperature, and selenium flux.

2.4 FILM COMPOSITION AND STRUCTURE

2.4.1 Electron Microprobe Analysis

In order to determine the range of CIS composition normally encountered, samples from 6 runs were analyzed at NREL by wavelength dispersive spectrometry using a Cameca MBX electron microprobe. The data are summarized in Table 2.2. Since at 10 keV the electron range in CIS is 0.78 μm, the compositions apply to a region lying between planes about 0.4 to 0.8 μm from the surface. Based on mass totals of almost exactly 100%, the films are fine-grained and non-porous, and the observed small standard deviations imply that the films are laterally homogeneous. No oxygen was detected (<0.5 at. %). Film 4-14-1 (23.3/26.4/50.3) was produced under our standard deposition conditions and exhibited the slightly Cu-poor composition generally acknowledged to be optimum for device performance. None of the films were Cu rich.

2.4.2 Stoichiometry and Molecularity

The data in Table 2.2 shows that as the Cu/In ratio decreases, the Se content increases. For material deviating from the exact stoichiometry of $CuInSe_2$ let us write

$$[Se] = \frac{[Cu]+[In]}{2} \cdot (2+\delta) \qquad (6)$$

Table 2.2. Film composition (atomic %) and the quantities δ, r and Cu/In

Sample #	Cu	In	Se	δ	$\frac{1-\delta}{1+\delta}$	Cu/In
4-13-1	19.71	28.32	51.97	0.16	0.72	0.70
4-14-2	20.02	28.29	51.69	0.14	0.75	0.71
4-9-2	20.09	28.21	51.70	0.14	0.75	0.71
4-14-3	21.34	27.42	51.24	0.10	0.82	0.78
1-21-2	21.64	27.28	51.08	0.09	0.84	0.79
4-14-1	23.32	26.43	50.26	0.02	0.96	0.88

where δ is to be found from the experimental data. These values of δ are also shown in Table 2.2, as are values for the ratio $r = (1-\delta)/(1+\delta)$ and Cu/In. It is clear that δ is a predictor of the Cu/In ratio, and that, except for the last film, r is approximately equal to Cu/In. This implies that the film composition is usually of the form $Cu_{1-\delta}In_{1+\delta}Se_{2+\delta}$, or equivalently:

$$\text{CIS composition} \approx (1-\delta)Cu_2Se + (1+\delta)In_2Se_3 \qquad (7)$$

From the standard definitions of the deviation of molecularity $\Delta x = (Cu/In) - 1$ and valence stoichiometry $\Delta z = 2Se/(Cu+3In) - 1$ we see that these films exhibit $\Delta x < 0$ and $\Delta z \approx 2(2+\delta)/(1-\delta+3+3\delta) - 1 = 0$. Actual values of Δz vary from -0.007 to -0.02, indicating only a very slight deficiency of the anions (Se) over cations. (Significant deviations from $\Delta z = 0$ could signal the presence of a secondary phase). Thus despite deviations from atom stoichiometry ($\Delta x < 0$), the valence stoichiometry is correct for the number of cation valence electrons to satisfy the anion octet.

For all six CIS films listed in Table 2.2, the In/Cu ratio is less than that of the unselenized metal layers (see Section 2.3.2). This implies In loss from the film during selenization, perhaps due to In_2Se emission. Also, despite the use of excess Se in the

selenization, the final Se content of the CIS automatically converges to that required for valence stoichiometry.

2.4.3 Auger Analysis

Auger depth profiles of EPV's CIS films showed that the concentrations of Cu, In, and Se are constant throughout the depth of the film. The only exception to this was the observation of an In-rich surface on one sample.

A preliminary Auger analysis of material emitted from the film during selenization showed the presence of Se only. The apparent absence of In (at a sensitivity of 1%) is hard to understand given the larger In-Cu ratio in the precursor than in the final CIS film.

2.4.4 X-ray Diffraction of CIS

$CuInSe_2$ crystallizes with a face-centered tetragonal unit cell. The chalcopyrite structure is a superlattice of sphalerite, and arises from the ordered substitution of the zincblende metal by two metals with the same average valence (see for example [10]). This is shown in Figure 2.10. (The other I-III-VI_2 compounds $CuInS_2$ and $CuInTe_2$ crystallize similarly). If, on the other hand, the cations are distributed randomly, then the cubic zincblende structure results, and certain x-ray reflections disappear.

We have examined the CIS films produced at EPV by x-ray diffraction using CuKα radiation (wavelength 1.542 A). The diffraction spectrum for a typical film is shown in Figure 2.11. The principal peaks occur at the 2θ values listed in Table 2.3. The table also shows the assignment of these reflections to $CuInSe_2$. The indices hkl are related to θ by the relation

$$\sin^2\theta = \frac{\lambda^2}{4}\left(\frac{h^2 + k^2}{a^2} + \frac{l^2}{c^2}\right) \qquad (8)$$

where the lattice constants for $CuInSe_2$ are a = 5.784 A and c = 11.614 A (c/a = 2.008). These data confirm that the film is polycrystalline, single-phase $CuInSe_2$.

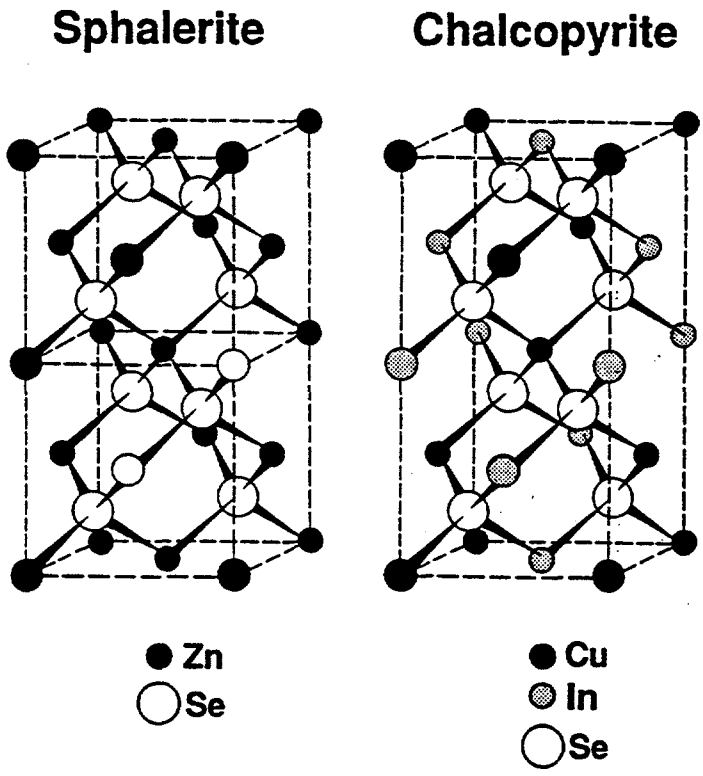


Figure 2.10 **Relationship of the chalcopyrite unit cell to the zincblende structure**

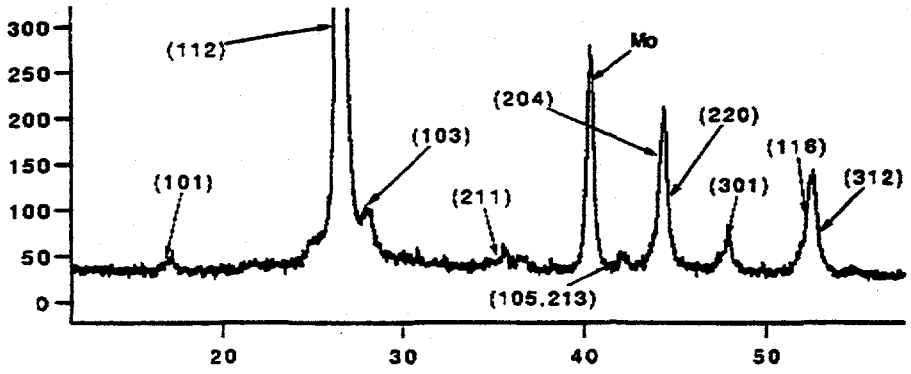


Figure 2.11 X-ray diffraction pattern (intensity versus 2θ) of thin film CIS on Mo

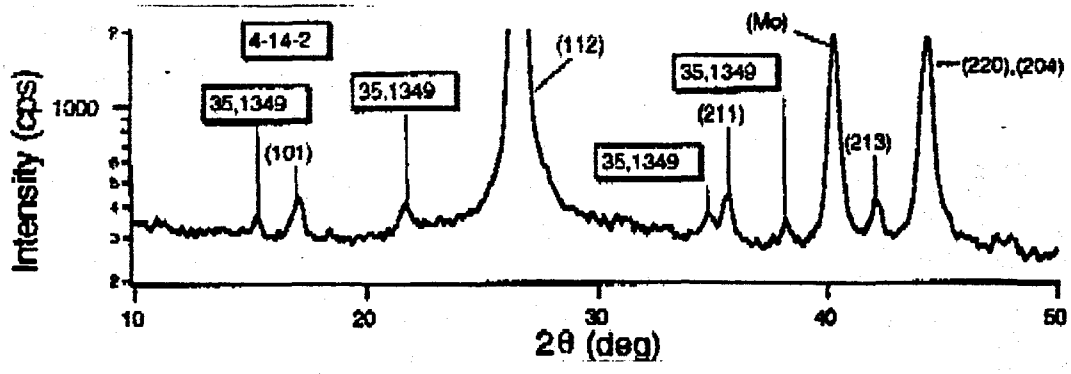


Figure 2.12 X-ray diffraction pattern of strongly Cu-poor CIS showing evidence of the $CuIn_2Se_{3.5}$ phase (JCPDS # 35-1349)

Table 2.3 Principal Reflections Observed in the X-Ray Diffraction of CIS Thin Films and Their Assignment to $CuInSe_2$ and $CuIn_2Se_{3.5}$

2θ	d(A)	hkl		
		$CuInSe_2$	$CuIn_2Se_{3.5}$*	Mo
15.4*	5.76		002	
17.1	5.18	101		
21.8*	4.08		110	
26.6	3.34	112		
27.7	3.22	103		
35.5	2.52	211		
38.1*	2.35		114	
40.5				110
41.9	2.15	105/213		
44.2	2.05	204/220		
47.8	1.90	301		
52.3	1.75	116/312		

* seen only in strongly Cu-poor films

A strong (112) preferred orientation (film growth perpendicular to the 112 planes) is indicated by the ratio of the 112 to 204/220 peak heights, the ratio being 8 compared to 1.5 for a random orientation. The existence of ordered material (chalcopyrite structure) is assured by the appearance of the (101) reflection indicating alternating Cu and In planes [11]. However, it is not clear to us that disordered material (zinc blende structure) could not also be present especially given the weakness of the (101) reflection. Such cation disorder would probably reduce carrier mobility.

In strongly Cu-poor films we also appear to see a Cu-poor phase of $CuInSe_2$, namely $CuIn_2Se_{3.5}$. Structural studies of this phase (JCPDS #35-1349) indicate tetragonal symmetry with lattice constants only slightly smaller than for $CuInSe_2$, an ordered In

lattice, and ordered Cu vacancies. The diffraction pattern for CIS film 4-14-2 with composition Cu 20.0%/In 28.3%/Se 51.7% is shown in Figure 2.12. Comparison of this spectrum to that of Figure 2.11 reveals additional peaks at 15.38°, 21.8°, and 38.1°. As shown in Table 2.3, these peaks are assigned to $CuIn_2Se_{3.5}$. Given that an In-rich surface phase has been found desirable for good photovoltaic performance (perhaps resulting in an inversion layer) [12], it would be of interest to know whether the observed $CuIn_2Se_{3.5}$ phase is uniformly dispersed throughout the film, or whether it is present only as an In-rich surface layer.

SECTION 3.0
DEVICE RESEARCH

3.1 DEVICE FABRICATION AND EARLY CELL RESULTS

The device structure employed by EPV is soda lime glass substrate/Mo/$CuInSe_2$/CdS/ZnO, where the ZnO consists of a thin, highly resistive layer adjacent to the CIS to reduce junction shunting, and a much thicker, highly conductive Al-doped layer to reduce the sheet resistance.

In the early stages of this program CIS layers of about 1μm thickness were prepared using composition-graded precursors as described in Section 2.3.2, and evaporated CdS films were used as the window layer. The CdS films were prepared by heating 0.5 - 0.75 g of high purity (99.999%) CdS powder in a graphite crucible to about 975°C. No pre-treatment of the CIS surface was employed, and the substrate was maintained at a temperature of 150°C. Film thicknesses ranged from 0.3 to 1.0μm. The point source configuration resulted in considerable thickness non-uniformity across the 30 x 30 cm^2 substrates.

The ZnO was prepared by rf magnetron sputtering of an alumina-doped ZnO target. Films about 0.8 - 1μm in thickness were employed resulting in a sheet resistance of about 25 - 40 ohms/square. The thickness of the insulating layer was about 1000 A. Evaporated Al contact pads were applied, and the cells were defined by mechanical scribing.

The best cell efficiency at this stage was about 5.6%, the cell parameters being V_{oc} 417 mV, I_{sc} 6.45 mA, FF 48.9%, total area 0.235 cm^2 (J_{sc} 27.4 mA/cm^2). Subsequent analysis of these cells revealed several non-CIS related limitations, namely series resistance effects (Mo, ZnO, and Al sheet resistance), contacting method, and CdS absorption. In addition, a survey of devices revealed a wide spread in reverse leakage currents, suggesting that junction formation and/or CIS properties were not under good

control. As described in Sections 3.3 - 3.7, attention to series resistance effects, the CIS In/Cu ratio, and the introduction of chemical bath deposition for the CdS considerably improved device performance and reproducibility.

3.2 TEMPERATURE-DEPENDENT STUDIES FOR JUNCTION ANALYSIS

A vacuum dewar was set up to enable material and device measurements to be performed over the temperature range 100 - 400 K. A thin-film Pt resistance thermometer operated from a constant current source is used to determine the sample surface temperature.

As part of a program to understand what controls V_{oc} in CIS solar cells, temperature dependent measurements were performed on evaporated CdS/CIS devices and are described in sections 3.2.1 and 3.2.2 below. We aim to repeat these studies using CBD CdS/CIS devices at a later date.

3.2.1 Dark I-V-T Data and Analysis

Using the dewar described above, the dark I-V characteristics for a 0.3 cm^2, low-leakage, evaporated CdS/CIS device were measured at five different temperatures for both forward and reverse bias [2]. The data are shown on a semi-log plot in Figure 3.1. It is apparent that the straight line mid-section of the forward bias curves are approximately parallel and shift with respect to the voltage axis with a temperature coefficient of about -2.4 mV/degree. This is larger than the temperature coefficient of V_{oc} (see below). At low temperatures and high forward bias a considerable fraction of the applied voltage appears to be dropped across a reverse-biased junction at the CIS/Mo interface.

For the straight line sections of the forward bias curves we may write

$$J = J_o(T)\ [e^{\alpha V}-1] \qquad (9)$$

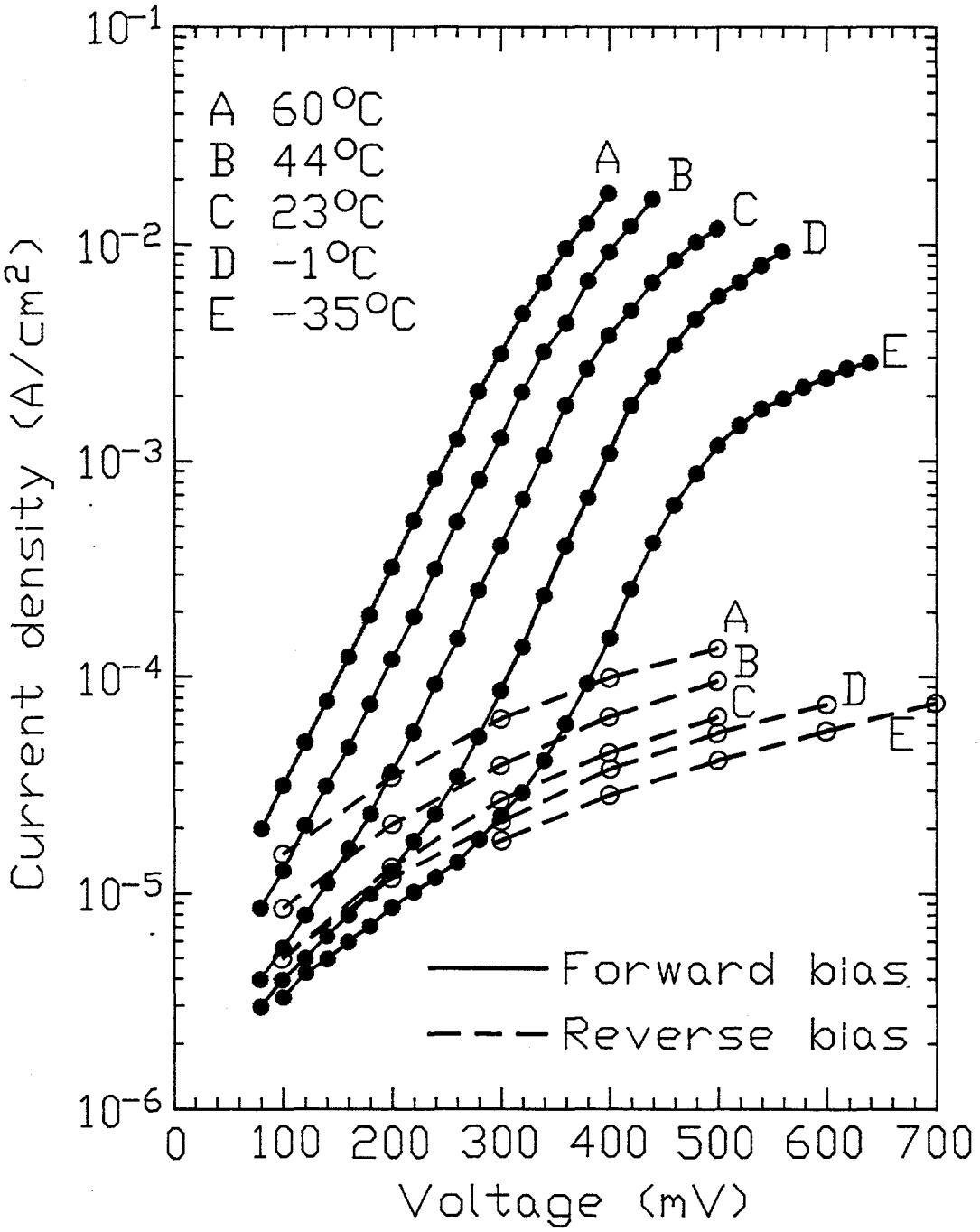


Figure 3.1 Dark J-V characteristics from -35°C to 60°C for an Al/ZnO/CdS/CIS device

where $\alpha = q/nkT$, the reverse saturation current is $J_o = J_{oo} \exp(-E_a/kT)$, and E_a is the activation energy. From the data we calculate the diode parameters listed in Table 3.1. A plot of ln J_o versus 1/T is given in Figure 3.2. This plot appears to confirm that, for temperatures above 270K, J_o is thermally activated, with $J_{oo} = 220 A/cm^2$ and $E_a = 0.52eV$.

The above analysis shows that E_a is approximately one half of the bandgap, as would be expected for recombination within the space charge region of a homojunction for which $J = J_o \exp(qV/2kt)$, and $J_o = J_{oo} \exp(-E_g/2kT)$. For the recombination current in a heterojunction, one model predicts $J = J_o \exp(qV/nkt)$, and $J_o = J_{oo} \exp(-qV_b/nkT)$, so that $E_a = qV_b/n$ where V_b is the band bending (barrier height) [13]. The problem here is that n is in practice found to be temperature dependent. (Indeed, nT, and hence α, is almost temperature-independent). For stepwise tunneling and recombination a current the form of $e^{\beta T} e^{\alpha V}$ is predicted but no appreciable thermal activation is involved. We tentatively believe the current to be controlled by recombination in the space charge region, but also conclude that none of the existing models for the J-V characteristics of heterojunctions account for the data on CIS in a fully consistent manner.

Table 3.1 Diode parameters as a function of temperature

T (K)	α (V^{-1})	n	J_0 (A/cm^2)
333	23.8	1.46	2.7×10^{-6}
317	24.3	1.51	9.3×10^{-7}
296	24.7	1.58	2.4×10^{-7}
272	25.5	1.67	4.0×10^{-8}
238	26.1	1.87	4.4×10^{-9}

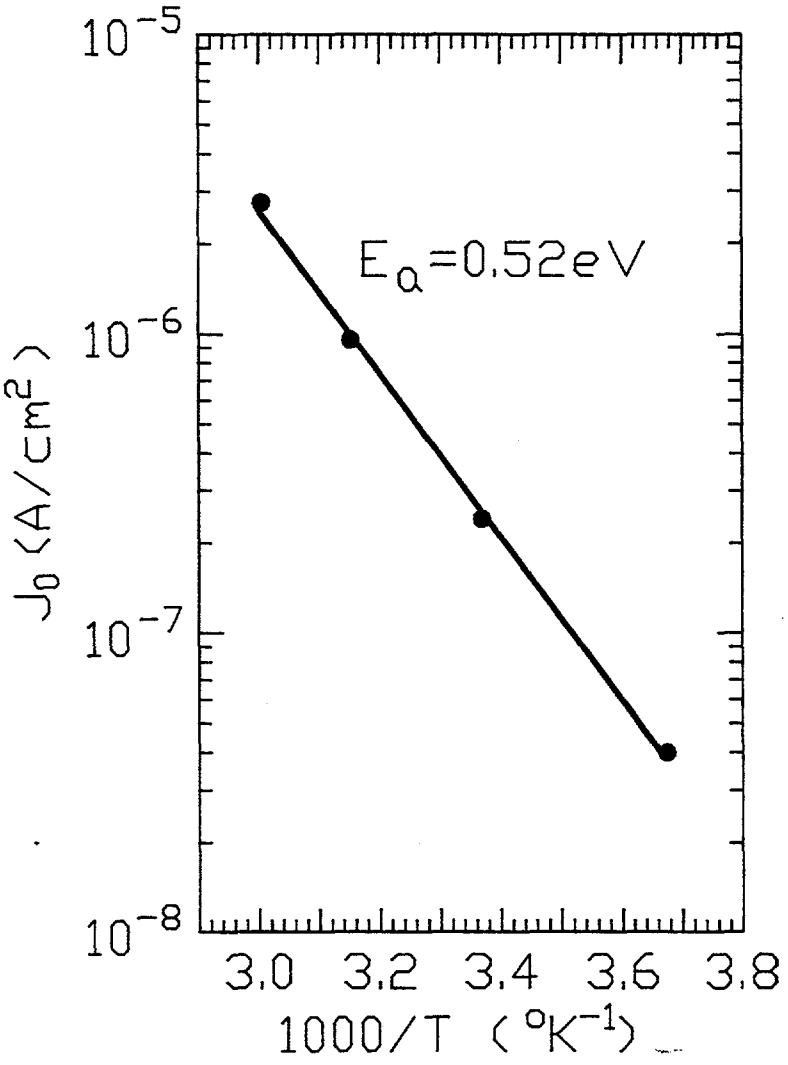


Figure 3.2 Activation energy plot for the reverse saturation current J_o

3.2.2 Open-circuit Voltage versus Temperature

Figure 3.3 shows the open-circuit voltage of a CIS solar cell (evap. CdS window layer) as a function of temperature for two levels of illumination (0.59 suns and 0.19 suns) [2]. Data below 300°K at 0.59 suns intensity is shown in the inset. For temperatures above 270K, V_{oc} is linearly dependent on temperature. Extrapolation of this data to 0°K yields voltage intercepts of 1.001 V and 0.996 V (see inset). From Eq.9 the intercept is nE_a/q, i.e. V_b. As expected, the built-in voltage so determined is independent of intensity. An increase in V_b through improvement of the junction should result in a correspondingly higher V_{oc}.

The slope of the linear portion of the $V_{oc}(T)$ plot is also of interest. This was -2.03 mV/K at 0.59 suns and -2.16 mV/K at 0.19 suns. The slope is controlled by the recombination constant J_{oo}, which in turn depends on the minority carrier lifetime. Thus, for a given V_b, improvement of the lifetime should also improve V_{oc}.

The observed increase in V_{oc}, constancy of I_{sc}, and increase in FF [13] as the temperature is lowered indicates that good CIS solar cells are limited by junction properties, and not by carrier collection. This in turn suggests that considerably higher V_{oc}'s may be obtained by junction modification (see also [14]).

3.3 ZINC OXIDE OPTIMIZATION

Following the realization that early ZnO films were too resistive, a systematic program for ZnO optimization was initiated. For characterization, equipment was set up to allow rapid and reliable assessment of ZnO films as regards sheet resistance and transmission. The reported figures for white light transmission were calculated as the ratio of currents measured by a CIS detector for glass/ZnO and plain glass substrates inserted into the beam from a 20 W tungsten lamp. This procedure automatically averages over interference fringes and takes into account the fall-off in transmission in the IR due to plasma absorption.

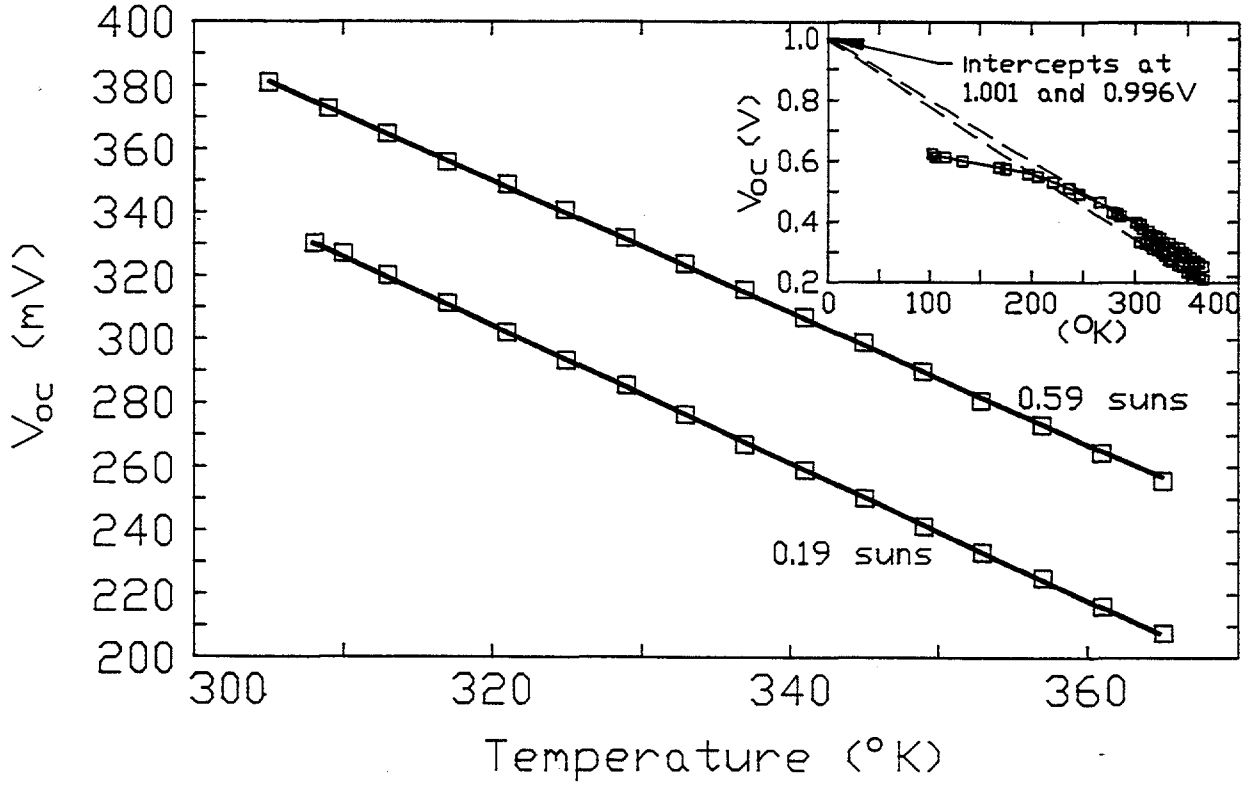


Figure 3.3 Open-circuit voltage versus temperature

In the first stage of optimization, ZnO films were prepared under various sputtering conditions and with different thicknesses, but with a fixed dopant concentration determined by the target (1% Al_2O_3 as dopant). The results of their characterization are summarized in Figure 3.4, and improved sputtering conditions were identified. The new conditions give lower sheet resistance for a given transmission and also improved spatial uniformity.

The next stage of optimization requires procurement of targets with different doping levels.

The optical transmission versus wavelength of our current ZnO:Al (conductivity 500 $(ohm\ cm)^{-1}$, thickness 1μm) is shown in Figure 3.5. A small, but not insignificant, decline in transmission is observed in the IR due to plasma absorption.

3.4 CHEMICAL BATH DEPOSITION OF WINDOW LAYERS

Adherent films of CdS have been deposited by chemical bath deposition (CBD) from an aqueous solution at 90°C using the acetate salts. The solution contains CdAc, NH_3Ac, NH_4OH, and thiourea at concentrations in the ranges of 10^{-4} -10^{-3} M, 5 x 10^{-3} - 10^{-2} M, 0.1 - 0.5 M and 5 x 10^{-4} - 5 x 10^{-3} M, respectively. The bath pH is maintained at 9.6. The solution is heavily buffered to suppress reaction rates and promote heterogeneous formation of CdS films. Typical film thicknesses are 0.05 - 0.10 μm. The films have been successfully applied as window layers to form CdS/CIS devices.

Other wide gap layers that have been deposited by chemical bath deposition include CdZnS and In_2S_3, a non-Cd containing potential window layer.

3.5 COMPARISON OF WINDOW LAYERS

A direct comparison has been made of CdS films prepared by evaporation and chemical bath deposition and applied as window layers to CIS thin film solar cells. Similarly prepared

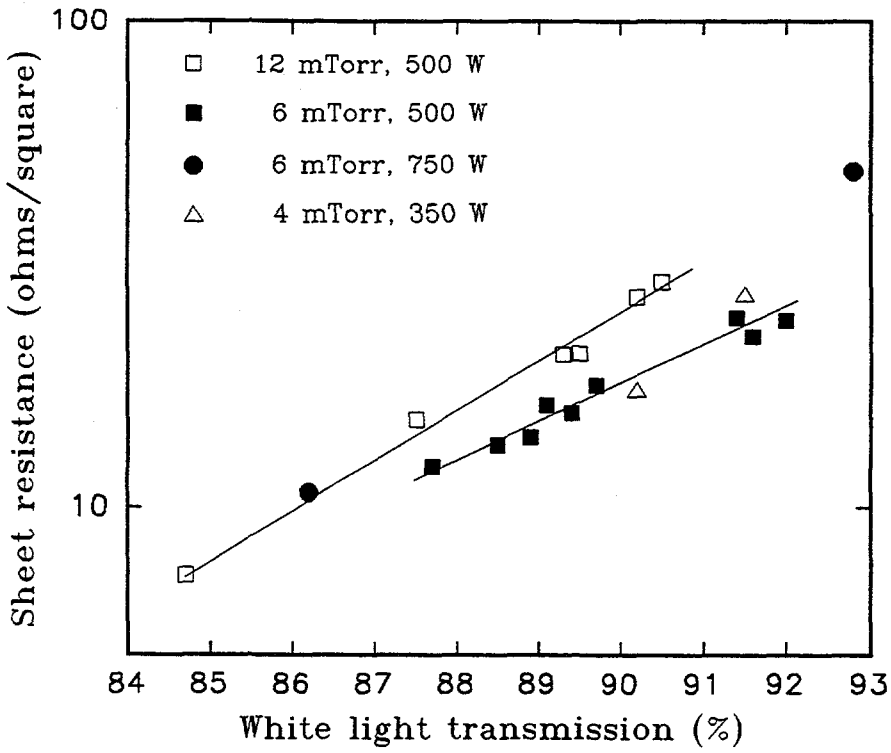


Figure 3.4 Sheet resistance versus white light transmission for ZnO films of different thickness and for different deposition parameters

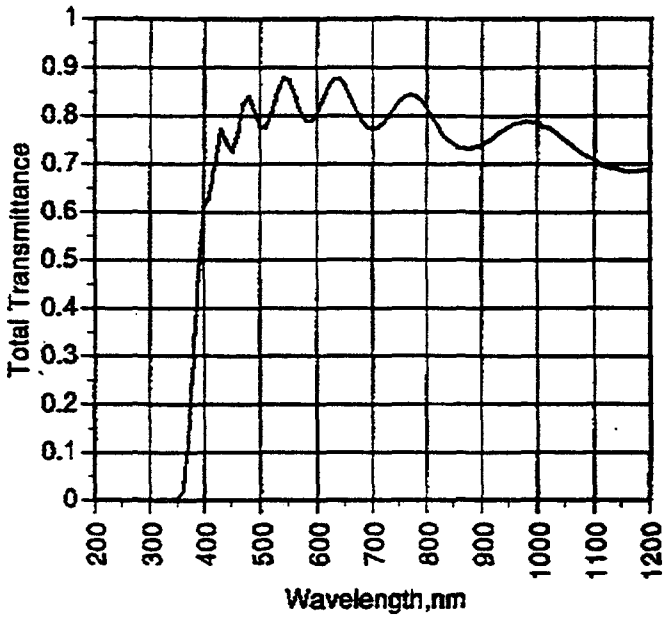


Figure 3.5 Total transmittance versus wavelength for ZnO:Al

CIS/Mo/glass samples were used.

The most notable difference between evaporated and CBD CdS was the improvement in J_{sc} on cells prepared with CBD CdS. The gain was typically 2 - 3 mA/cm^2. The main reason for this appears to be the enhanced optical transmission of the thin CBD films relative to the evaporated CdS films in thicknesses optimized for PV performance. This is shown in Figure 3.6. For the evaporated CdS films, the transmission falls rapidly to zero for wavelengths below the band edge i.e. below 520 nm, while the CBD films still offer 50% transmission at 400 nm. The sub-gap transmission of the CBD CdS is also superior to that of the evaporated CdS.

Spectral response measurements of CdS/CIS junctions confirm that there is a significant contribution to the photocurrent for wavelengths below 500 nm for junctions with CBD CdS. Quantum efficiency data are shown in Figure 3.7 for devices with the two types of CdS. Attempts to compare evaporated and CBD films of similar thickness have so far not been successful because of the difficulty of preparing thin (<0.1 μm) evaporated CdS/CIS junctions without excessive shunting.

The second difference that we have noted is that the CBD technique produces more reproducible junctions than does evaporation of the CdS. Side-by-side comparison of the two techniques on opposite halves of a 1 ft^2 CIS/Mo/glass plate demonstrated superior uniformity as well as higher V_{oc}'s in the half with the CBD CdS coating. Over many samples, the deficit in V_{oc} with evaporated CdS ranged from zero to 150 mV. In a further experiment, "dead" evaporated CdS/CIS plates with very low V_{oc}'s were resurrected by chemically removing the CdS and re-coating with CBD CdS. The CBD technique may remove oxides, excess Se, or $Cu_{2-x}Se$ from the CIS surface, resulting in improved junction characteristics. The CdS evaporation set-up and procedure probably requires modification to ensure the reproducible deposition of stoichiometric CdS films. The latter problem will be addressed in the future.

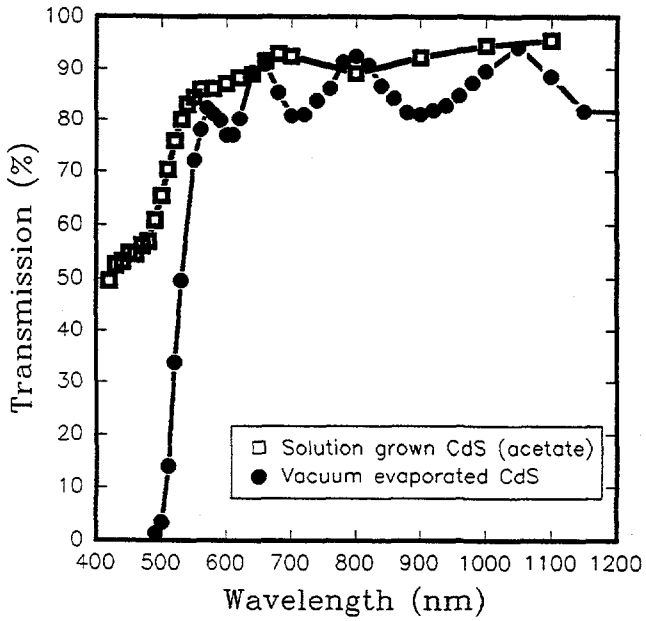


Figure 3.6 Optical transmission versus wavelength for solution-grown (CBD) CdS and vacuum evaporated CdS thin films in thicknesses optimized for PV performance

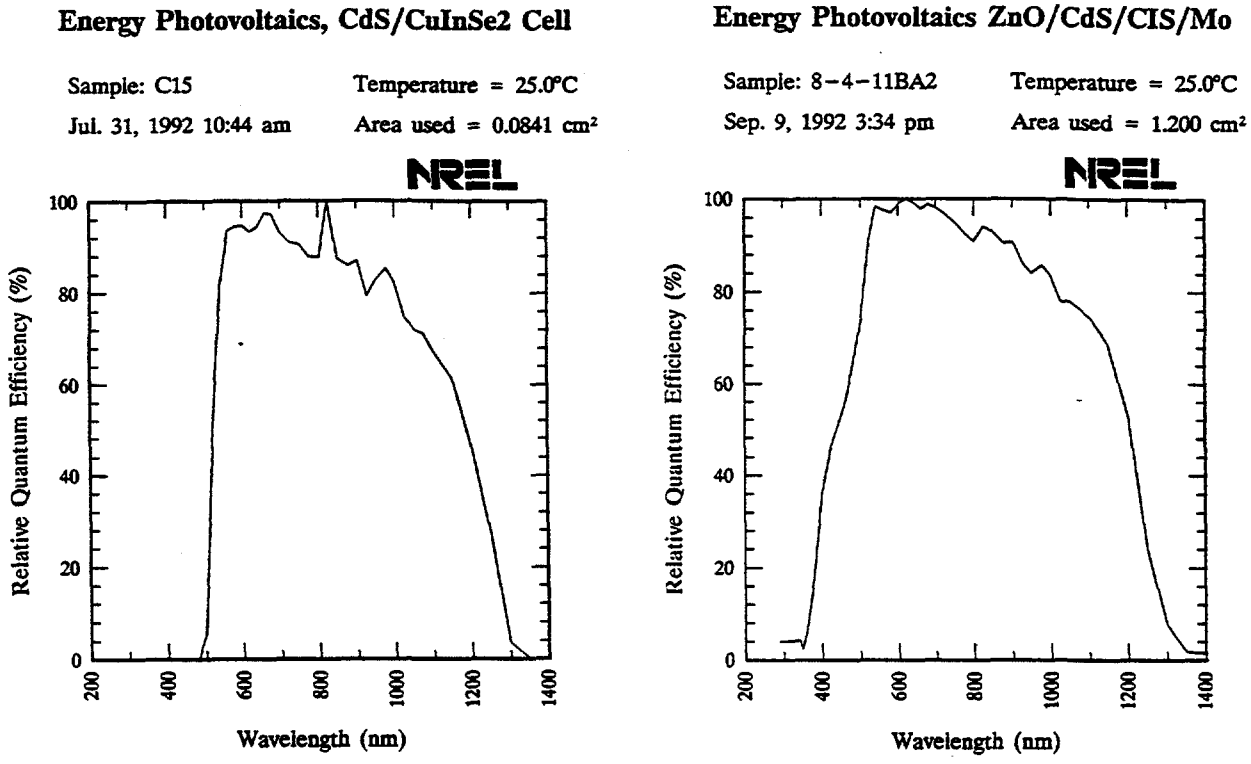


Figure 3.7 Normalized quantum efficiency data for CIS solar cells with window layers consisting of evaporated CdS (left) and CBD CdS (right)

3.6 EFFECT OF In/Cu RATIO ON DEVICE PERFORMANCE

A series of CIS films were prepared using precursors spanning a range of In/Cu thickness ratios. Specifically, identical Cu sublayers were employed for all films, while the substrate scan speed past the In cathode was varied from 44 to 72 cm/min in steps of 4 cm/min. The films were identically processed into devices (using evaporated CdS window layers) and measurements were made of their photovoltaic parameters (V_{oc}, J_{sc}, QE (680 nm), FF, efficiency). Subsequently, the ZnO and CdS films were removed by etching (50/50 H_2O/HCl at 60°C), and the same set of CIS films were analyzed by electron microprobe for Cu, In, and Se content.

The measured composition of these films is given in Table 3.2. The observed trend in In/(In + Cu) ratio correlates reasonably well with the progression in In scan speed with the exception of the film prepared at a scan speed of 60 cm/min. This film in fact possessed the lowest In/(In + Cu) ratio. Also, the films prepared with In scan speeds of 44 and 48 cm/min possessed almost identical compositions, as did those prepared at 52 and 56 cm/min. These observations suggest that the In deposition rate or In loss during selenization were not under complete control.

The photovoltaic parameters measured at 100 mW/cm^2 for the best device on each film are shown plotted against the measured Cu/In ratio of the CIS in Figure 3.8. (The Cu/In ratio for the film prepared at 64 cm/min was estimated by interpolation.) Because of slight variations in the area of these devices, the variation in current density is not shown, but rather the measured quantum efficiency at 680 nm.

Table 3.2 Measured composition of CIS films used in the In/Cu ratio device study

Film #	In Scan Speed	Cu	In	Se	Cu/In	In/(In+Cu)
	(cm/min)	(%)	(%)	(%)		
5-14-3	44	20.8	27.9	51.3	0.743	0.573
5-15-1	48	20.8	28.1	51.1	0.742	0.574
5-19-1	52	22.1	27.5	50.4	0.805	0.554
5-21-1	56	22.0	27.3	50.6	0.806	0.553
5-27-2	60	23.6	26.4	50.0	0.894	0.528
5-20-5	64	film not analyzed			0.828*	
5-22-1	68	22.8	27.1	50.2	0.841	0.543
5-27-1	72	23.2	26.8	50.0	0.866	0.536

* interpolated

Figure 3.8 shows an approximate plateau in conversion efficiency for Cu/In ratios lying between 0.89 and 0.83, with a very strong decline in the range 0.83 to 0.74. The principal reason for the strong decline in efficiency is a steep fall in fill factor. This might be caused by the CIS becoming more resistive as it becomes very In rich. The open-circuit voltage appears to decline steadily with decreasing Cu/In ratio, although the slowness of the decline makes V_{oc} a fairly insensitive measure of CIS quality, especially for very In rich films. A slight decline in quantum efficiency is also observed for decreasing Cu/In ratio, perhaps due to parasitic absorption of a residual indium selenide or a reduced minority carrier diffusion length. Future work will investigate the wavelength dependence of this effect.

Finally, we should caution that cell performance may not be a

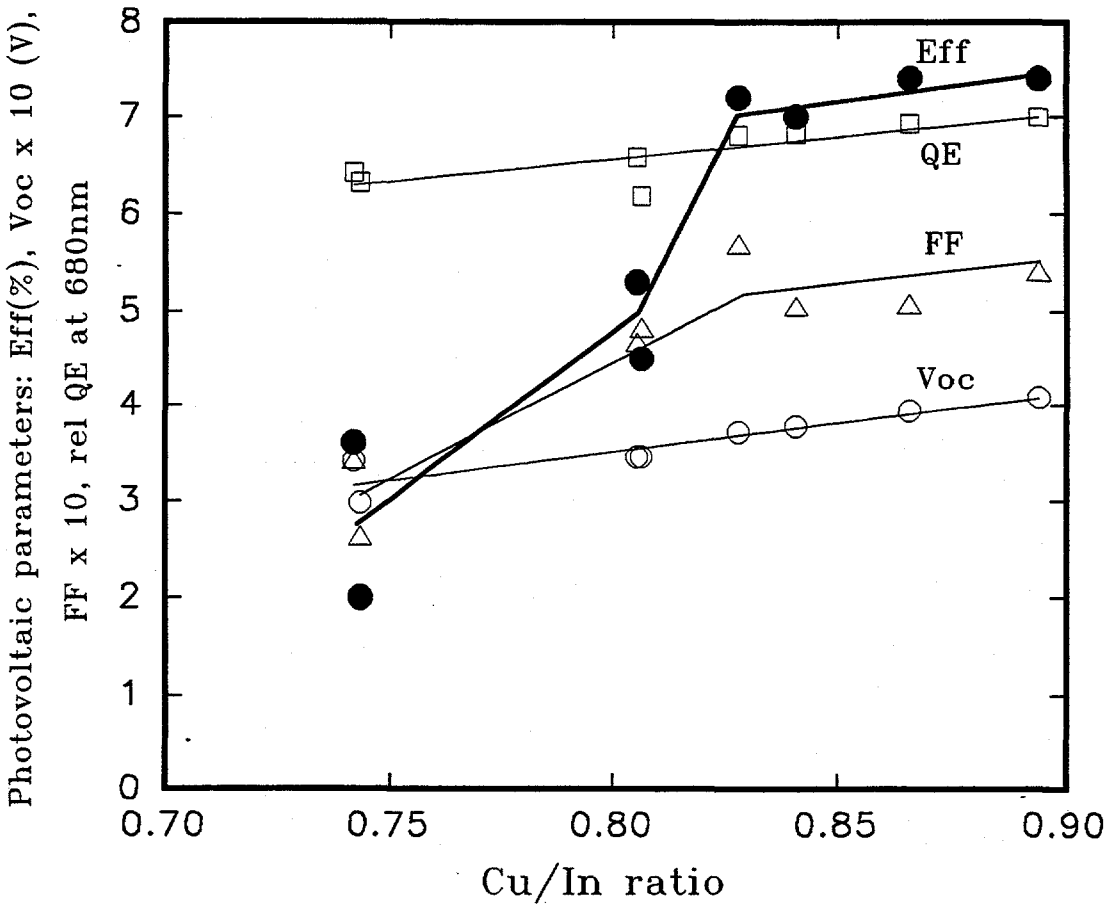


Figure 3.8 Photovoltaic parameters versus Cu/In ratio of the CIS

unique function of the CIS Cu/In ratio, and that the Cu/In ratio for the precursor may turn out to be a more fundamental parameter. Operationally, however, the above study shows that a ±6% variation in precursor Cu/In ratio results in a ± 3% variation in cell efficiency in the plateau region, i.e. the process is self stabilizing.

3.7 HIGH EFFICIENCY CELLS

A steady improvement in active area cell efficiency has resulted from analysis of the deficiencies of early cells and advances in the following areas:

- reduction of series resistance effects
- improved CIS quality
- improved junction formation and CdS
- addition of anti-reflection (A/R) coating

Increased attention has also been given recently to total area efficiency, and therefore to grid design. We discuss these areas in greater detail below, with reference to Table 3.3 which summarizes the performance of cells sent to NREL for efficiency verification.

3.7.1 Reduction of Series Resistance Effects

Early fill factor limitations (see first entry of Table 3.3) were minimized through the use of thicker Mo to reduce its sheet resistance, the use of In solder on the Mo to lower both series resistance and measurement probe contact resistance, and the adoption of improved ZnO sputtering conditions (as described in Section 3.3) to lower the ZnO sheet resistance to about 20 ohms/sq. while maintaining transmission. For 1 cm^2 cells, serious limitations were also discovered in the achievable sheet resistance of the evaporated Al used for grid formation. A shadow mask was

designed for 1 cm^2 cells with the goal of largely preserving the intrinsic cell fill factor consistent with the then achievable ZnO and Al sheet resistances. Depending on the overall cell dimensions, the area loss associated with this mask ranged from 25 - 30%. This mask was employed for all four of the 1 cm^2 (nominal) cells reported in Table 3.3. More recently, In or In-Ag has been substituted for the Al as the grid material, resulting in sheet resistances of the order of 0.08 ohms/square.

3.7.2 Improvement in CIS Quality

Conducive to the achievement of higher efficiency cells has been the improvement of the CIS in terms of reproducibility, uniformity, and electronic properties. Reproducibility was increased through careful attention to the precursor deposition temperature and Cu/In ratio. The Cu/In ratio is maintained below the level at which CIS delamination is occasionally observed. Spatial uniformity of the CIS across 30 x 30 cm^2 substrates was improved through a re-design of the substrate heater lamp assembly for better temperature uniformity during selenization. Electronic properties of the CIS were improved through a refinement of the rate/temperature/time profile for selenization.

Device efficiency was also found to depend on the thickness of the CIS layer. An increase in CIS thickness from about 1.2 μm to 1.55 μm resulted in an increase in J_{sc} of 2 - 3 mA/cm^2. Future work will explore this thickness dependence more carefully.

3.7.3 Improved CdS and Junction Formation

Sections 3.4 and 3.5 described the preparation of CdS by chemcial bath deposition and the application of these layers to CdS/CIS heterojunctions resulting in improved short wavelength response. Thinning of the CBD CdS subsequently led to further increase in J_{sc}. Modification of the bath chemistry has recently led to improved open-circuit voltages, with V_{oc}'s in the range of 420 - 440 mV being observed with no loss in fill factor. Cadmium

zinc sulfide has also been prepared, resulting in V_{oc}'s of up to 450 mV, but the films are so far too resistive.

We have also observed that a KCN etch of the CIS surface prior to CdS deposition is in most cases helpful in improving junction quality and V_{oc} by 10 - 20 mV.

3.7.4 Anti-Reflection Coating and Grid Design

A reliable procedure was developed for the deposition of a quarter-wave coating of AlF_3 onto completed cells. The refractive index of AlF_3 in thin film form is 1.36 at 600 nm (1.34 at 1000 nm) [15]. The films are unaffected by water, and have zero water absorption [16]. In this respect AlF_3 is unlike MgF_2 which grows only to 80% of bulk density and hence admits moisture into voids. Aluminum fluoride films are clear, smooth, and hard, and exhibit excellent durability and adhesion. They are currently used for mirror coatings in excimer lasers. We are not aware of any previous use of AlF_3 as a solar cell A/R coating, except by one of the authors (AD) as an A/R coating on glass for a-Si:H solar cells on a glass superstrate. We have deposited AlF_3 films at a rate of 12 A/s by thermal evaporation (sublimation) from AlF_3 lumps contained in a tungsten basket. The substrate was not deliberately heated, although substrate temperatures of 250°C are recommended for the highest density, water resistance and hardness. The correct thickness is obtained by monitoring in-situ the reflectivity of a ZnO/CdS/CIS test piece at 630 nm during evaporation of the AlF_3. Improvements in J_{sc} of 4.5 - 5.0% under EPV's simulator are routinely obtained. An incremental increase in V_{oc} automatically results from the improved J_{sc}.

The reduction of grid line resistance through the use of In or In-Ag recently allowed re-design of the grid mask in order to obtain less shadowing of the cell and higher total area efficiency. A highly efficient branching design was devised based on minimization of current path length, and relecting the symmetry of the cell. The mask was received at the end of Phase I. The dead

area is about 10%, compared to 25 - 30% for the mask previously used. An increase in V_{oc} of 10 - 12 mV is also observed owing to the reduced forward current in the dark diode underlying the grid. The metallization pattern is shown in Figure 3.9.

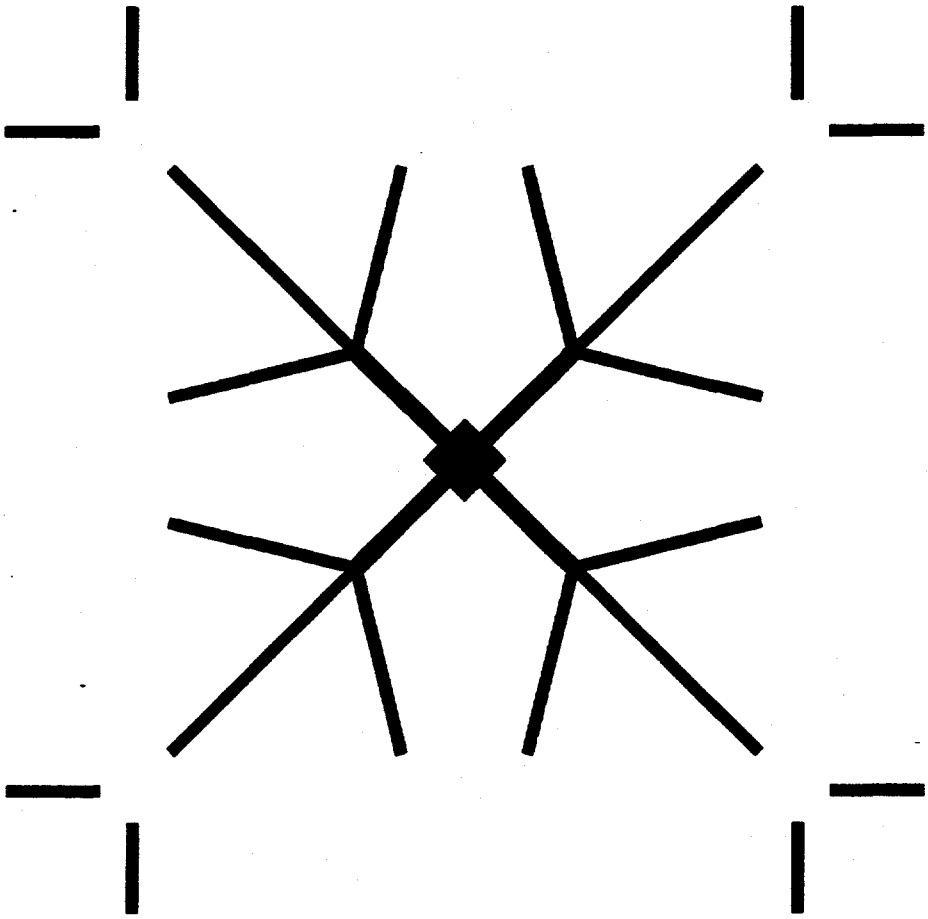


Figure 3.9 Metallization pattern featuring low voltage drop and reduced shading

3.7.5 Results

The advances described in section 3.7.1 - 3.7.4 were incorporated into CIS prepared near the end of Phase I and into cells fabricated using this material. The best cells resulting from this effort are listed in Table 3.3. The new metallization masks arrived too late to be used for any of the cells reported in Table 3.3, so that total areas are considerably larger than active areas.

Table 3.3 Performance of cells/modules sent to NREL

Date Meas'd	Area act/tot (cm^2)	V_{oc} (mV)	I_{sc} (mA)	J_{sc} act/tot (mA/cm^2)	FF (%)	Eff act/tot (%)	Comments
pre-'92	?/0.235	417	6.45	?/27.4	48.9	?/5.6	
7/1/92	0.423/0.485	360	12.5	29.6/25.8	62.3	6.65/5.8	
8/3/92	0.062/0.0713	411	2.07	33.4/29.1	62.1	8.54/7.4	
9/10/92	0.83/1.2	408	29.1	35.1/24.2	62.9	9.01/6.2	
9/10/92	1.60/1.96 24.0/29.4	391 5860	52.5	32.8/26.3	43.8	5.6/4.6	per cell 15 cells
12/23/92	1.10/1.463	429	38.9	35.5/26.6	66.6	10.1/7.6	A/R
12/23/92	1.14/1.510	443	41.5	36.3/27.5	64.3	10.3/7.8	A/R, LS
12/23/92	1.10/1.466	441	39.6	36.0/27.0	66.0	10.5/7.9	A/R, LS

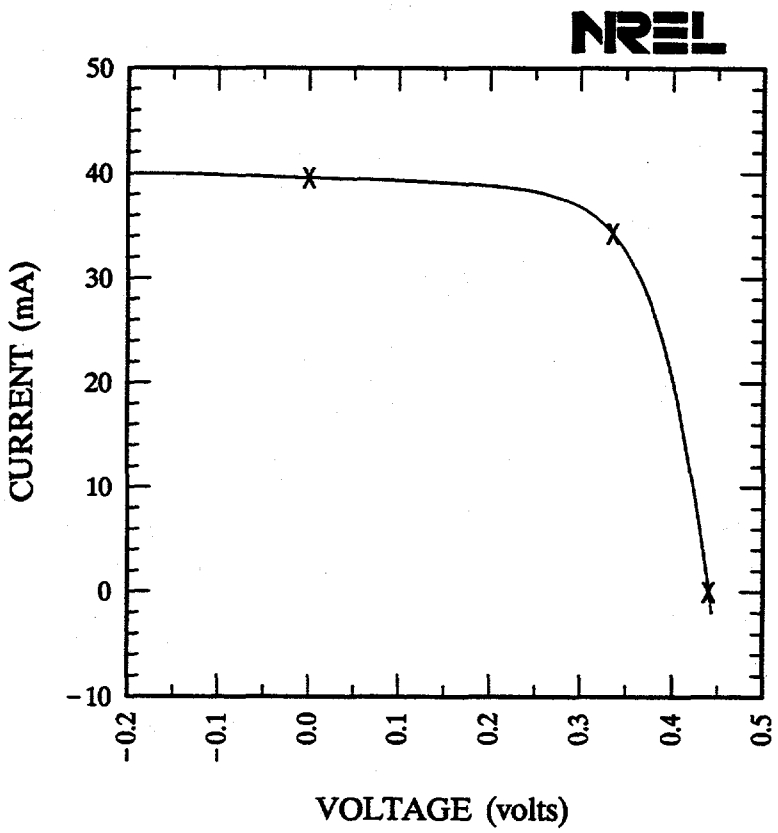
Total area data measured at NREL; active area data calculated from NREL data using active areas measured at EPV.

An active area efficiency of 10.5% was achieved for a cell with 1.466 cm^2 total area and 1.10 cm^2 active area. The other parameters were V_{oc} 441 mV, J_{sc} 36.0 mA/cm^2 (active area), and FF 66.0%. The NREL-measured I-V curve for this cell is shown in Figure 3.10. This I-V curve was recorded after the cell had been light soaked for 20 minutes, resulting in a 1.5% gain in power.

Energy Photovoltaics, CIS/Glass 20' soak

Sample: 11-11-163C Temperature = 25.0°C

Dec. 23, 1992 4:01 pm Area = 1.466 cm²



V_{oc} = 0.4407 volts	I_{sc} = 39.59 mA
J_{sc} = 27.00 mA/cm²	P_{max} = 11.52 mW
Fill factor = 66.01 %	I_{max} = 34.29 mA
Efficiency = 7.9 %	V_{max} = 0.3358 V

Figure 3.10 **I-V curve for a 1.47 cm² total area (1.10 cm² active area) CIS solar cell with CBD CdS and AlF_3 A/R coating. Efficiency under standard test conditions (AM1.5 global, 100 mW/cm², 25°C) is 7.9% on a total area basis, corresponding to 10.5% on an active area basis**

For the 10.3% efficient cell of Table 3.3 the power gain was 5% after light soaking, most of the improvement stemming from a rise in fill factor from 61.6% to 64.3%. The dark I-V curve of the 10.3% cell is shown in Figure 3.11. The spectral response of these high efficiency cells are all quite similar to that shown for the cell with CBD CdS in Figure 3.7. We attribute the fall off in quantum efficiency between 700 - 1150 nm to both absorption in the ZnO and inadequate carrier collection in the CIS for deeply absorbed light. Roughly equal weight is given to each of these effects, as may be judged from the ZnO transmission curve of Figure 3.5. This implies that higher J_{sc}'s are attainable by reducing the ZnO absorption and increasing the CIS minority carrier diffusion length.

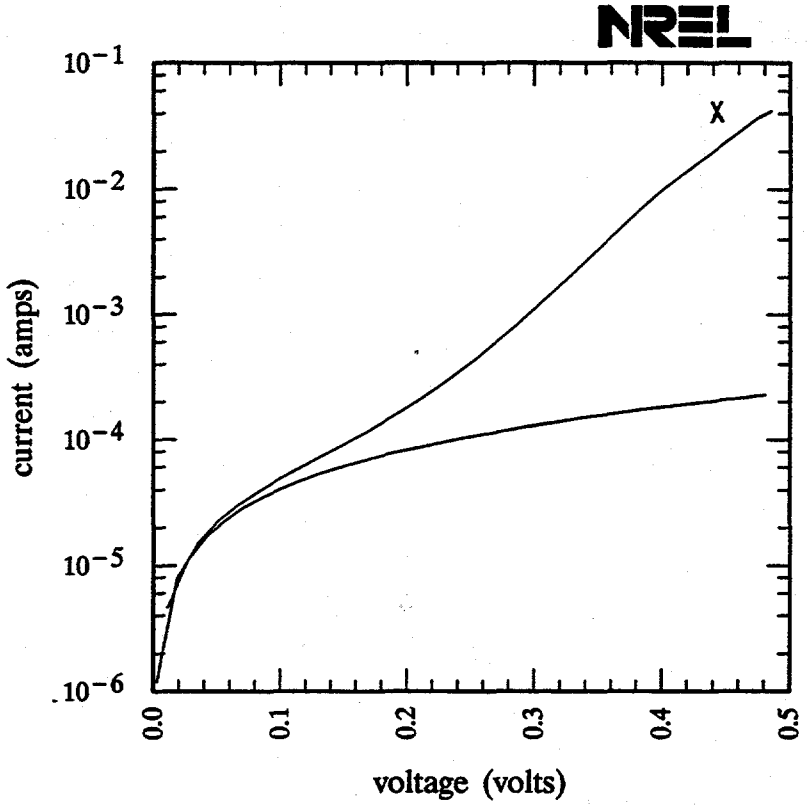
I-V measurements performed by NREL for one cell metallized using the new grid design showed a total area J_{sc} of 30.7 mA/cm² compared to the 26 - 27 mA/cm² normally obtained.

Note added in proof. Recent measurements have shown that the use of CBD CdS has increased the junction built-in voltage V_b from 1.00 eV (evaporated CdS, see section 3.2.2) to 1.07 eV (CBD CdS) thereby accounting for the improved V_{oc}.

Energy Photovoltaics, CIS/Glass

Sample: 11-11-164B Temperature = 25.0°C

Dec. 23, 1992 3:36 pm Area = 1.510 cm²



R_{shunt} = 1.78 Kohms

R_{series} = 4.23 ohms

Equivalent R_s = 0.999 ohms

Figure 3.11 Dark I-V data for a 1.5 cm² CIS cell

SECTION 4.0
MODULE DEVELOPMENT

4.1 SCALE-UP ISSUES AND ACTIVITIES

The development of 30 x 30 cm^2 modules has required scale up of several of the deposition processes, achievement of suitable patterning methods, and attention to the vitally important issue of layer uniformity. A cross-sectional view of a CIS module is shown in Figure 4.1. As described earlier, deposition of the metals (Mo, Cu, In) has always been conducted at the 30 x 30 cm^2 level, and this operation required no scale up. However, as described below, scale up was required for the CdS window layer and ZnO transparent conductor. Also, in order to overcome the point-source limitations of the existing selenization system a second selenization system has been constructed.

4.1.1 Scale up of CBD CdS

The initial set up for chemical bath depositions was designed for 5 x 10 cm^2 (2" x 4") substrates. A heated, uniform flow reaction vessel was later constructed so that CBD CdS films are now routinely deposited in a batch process onto two 30 x 30 cm^2 (1 ft^2) substrates. Top-to-bottom non-uniformities in the CdS have been eliminated by increased circulation. The design of the vessel minimizes the volume of waste from the process.

4.1.2 Scale up of sputtered ZnO

Zinc oxide films are deposited onto 30 x 30 cm^2 substrates by scanning the substrate back and forth across a 38 cm long sputtering target. The scan rate and deposition time have been optimized to produce the desired ZnO sheet resistance. Some non-uniformities exist at the corners of the substrate.

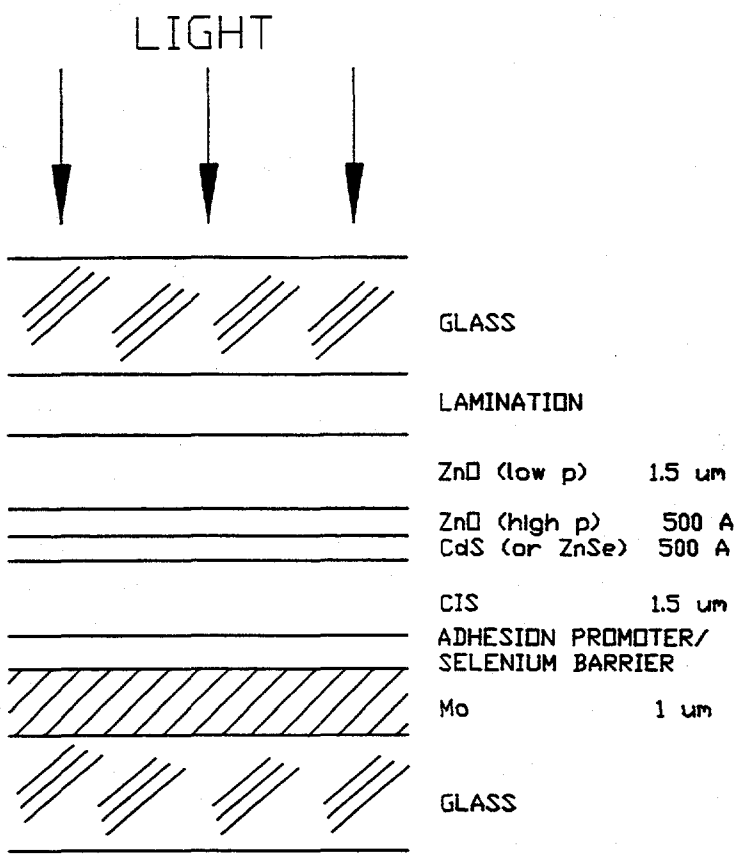


Figure 4.1 CIS module cross section

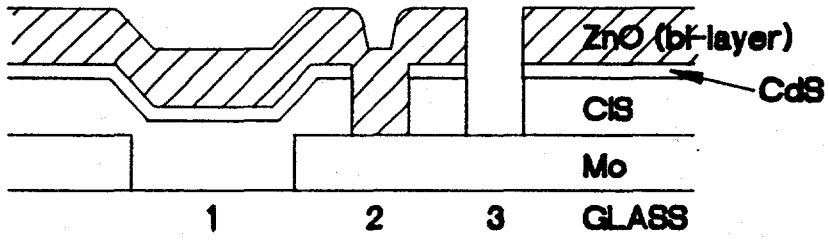


Figure 4.2 Schematic of module interconnect structure

4.1.3 New selenization system with linear source

An entirely new selenization system has been assembled and its components are being tested. The system features a distributed (linear) selenium source, provision for a second source (in order to prepare the quaternary $CuIn(Se,S)_2$), translation capability for 30 x 30 cm^2 substrates, and computer monitoring.

4.2 MODULE DESIGN

The interconnect scheme currently employed for the production of modules in shown in Figure 4.2. This scheme requires three patterning steps, the sequence of operations for module fabrication being:

1. clean glass
2. sputter deposit Mo
3. laser pattern Mo
4. sputter deposit $(Cu-In)_n$
5. heat and selenize
6. deposit CdS by CBD
7. mechanically pattern CdS/CIS
8. sputter deposit ZnO bilayer
9. mechanically pattern ZnO (including CIS)
10. encapsulate and test

An overall cell width of 0.5 cm (including interconnects) is currently employed. With this width fixed for the time being, the zinc oxide thickness must be increased over that employed for the fabrication of 1 cm^2 cells, the collection lengths in the two cases being about 0.45 cm and 0.2 cm, respectively.

In order to perform this calculation, the relationship between zinc oxide sheet resistance and transmission must be known as a function of thickness. These quantities were measured for ZnO films prepared over a wide range of thicknesses under the optimum conditions identified in section 3.3, and the results are shown in Figure 4.3. Numerical integrations were then performed to derive the terminal I-V characteristics of a distributed CIS solar cell of

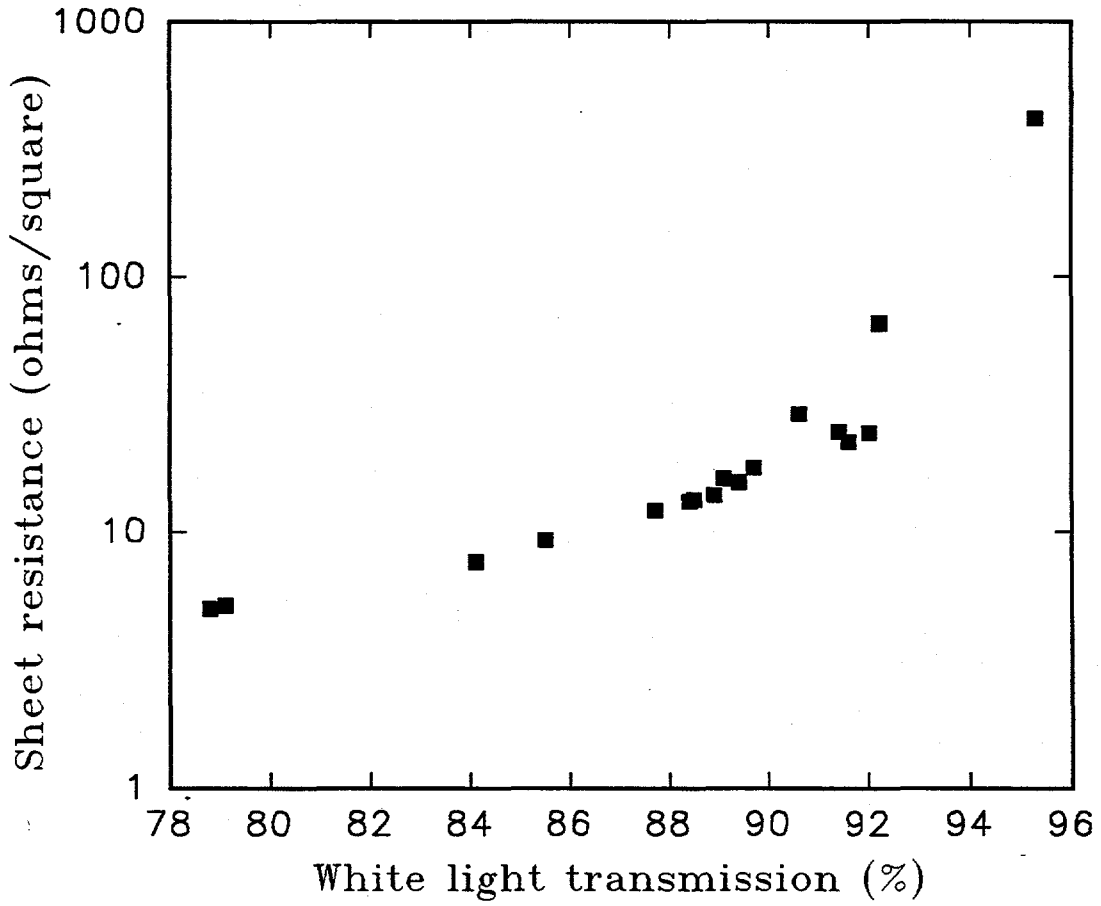


Figure 4.3 Relationship between ZnO:Al sheet resistance and white light transmission over a wide range of film thicknesses (for fixed sputtering conditions)

width 0.45 cm for given values of ZnO sheet resistance and transmission. The thickness of the ZnO was changed iteratively to maximize the power output of the distributed cell. The optimum ZnO thickness was found to be about 1.5 μm, and this thickness has been adopted for module fabrication.

4.3 PATTERNING METHODS

We start by discussing patterning of the Mo layer. The Mo layer can readily be cut and electrically isolated by laser blow off using a pulsed Nd-YAG laser operating at 1.06 μm. To pattern the entire 30 x 30 cm^2 plate the Mo-coated substrate is translated on an X-Y table under the focused beam of the YAG laser. However, serious problems were encountered with the quality of interconnects achieved using this process. Using a stylus profilometer it was discovered that the scribed region lying between the separated Mo films was enormously raised relative to the plane of the Mo. It was further realized that this resulted from extensive cracking and damage to the glass surface. This jagged raised region is shown in the profilometer trace of Figure 4.4.

Following the realization of this effect, a chemical etching method was developed and successfully used in the production of modules. The etching method involves screen-printing and curing of a resist, acid etching of the Mo, removal of the resist, and cleaning.

More recently, we have re-visited the Mo patterning problem. Three successful techniques are now at our disposal, including a laser process that does not result in damage to the glass. A line width of about 5 mils is currently employed in the laser process.

For the second and third patterning steps (CIS and ZnO cuts) mechanical scribing has been found satisfactory, although not without room for improvement in terms of area loss, definition, adhesion, and contact resistance (see Section 4.5).

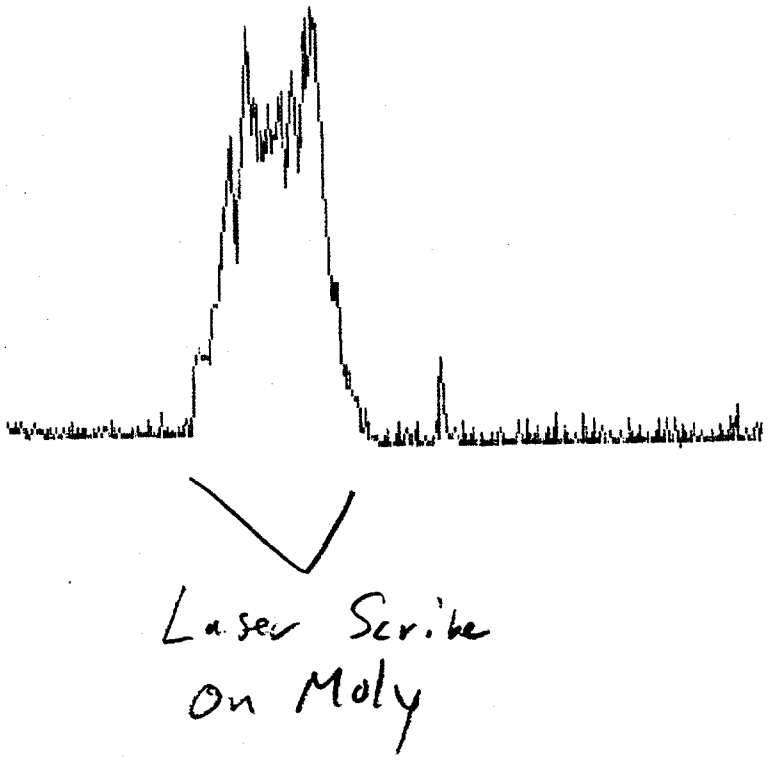


Figure 4.4 Profilometer trace of laser-scribed Mo on glass showing glass damage

4.4 MODULE FABRICATION

Full size (30 x 30 cm^2) CIS modules have been fabricated consisting of 55 interconnected subcells each 0.5 cm in width. After glass-glass encapsulation and framing, these modules have produced 14.5 volts and 0.17 amps in sunlight. These results clearly do not reflect the intrinsic small area cell efficiency, and diagnostic studies are underway to understand the various defects in these modules.

The performance of smaller modules is more satisfactory but interconnect problems have been shown to limit the fill factor. The I-V curve of a 15 cell module with 29.4 cm^2 total area is shown in Figure 4.5. (Data for this module is also tabulated in Table 3.3). The total area efficiency is 4.6%, corresponding to an

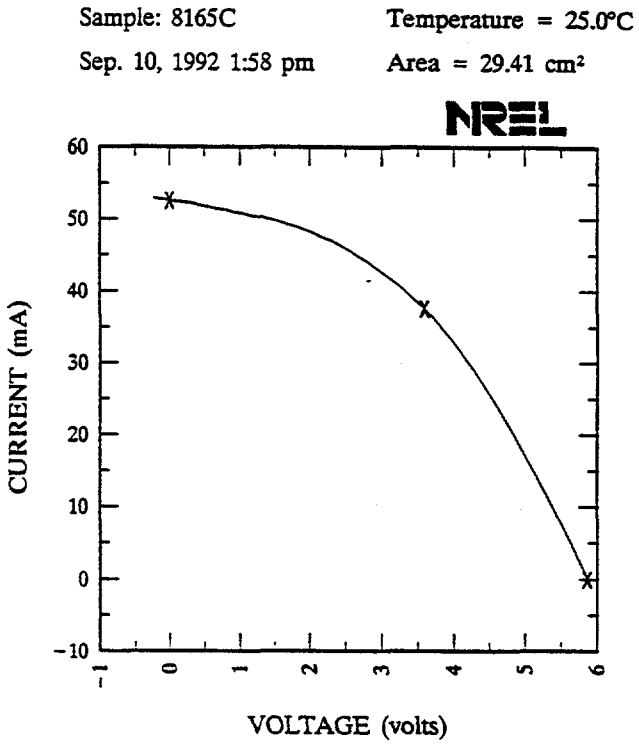


Figure 4.5 I-V curve for a 15 cell CIS module (total area efficiency 4.6%, active area efficiency 5.6%)

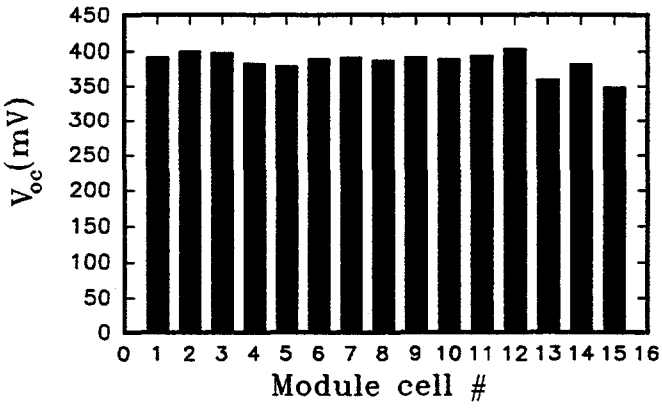


Figure 4.6 V_{oc} map at 1 sun illumination for the module of fig. 4.5

active area efficiency of 5.6%. A respectable average V_{oc} of 391 mV per cell was achieved, and all cells were active. A V_{oc} map (Figure 4.6) for all 15 cells in the module confirms that good uniformity of response was obtained, with the exception of slight shunting in two cells. J_{sc} was 32.8 mA/cm^2 (active area basis, no A/R coating). Fill factor, however, was limited by interconnect resistance to 43.8%.

4.5 INTERCONNECT RESISTANCE

Evidence that a substantial contact resistance can appear at the ZnO/Mo interface has been found from potential probe studies. Thus, with 30 mA passing through a test structure consisting of silver paint/ZnO contact pads on a strip of Mo-coated glass, the voltage obtained by probing at various positions is shown in Figure 4.7. A linear variation of potential with distance can be seen for the molybdenum, followed by abrupt drops at the Mo/ZnO and ZnO/silver paint interfaces. A drop of over 20mV at the ZnO/Mo cell interconnect would clearly reduce the fill factor of the module. The high resistivity ZnO layer may be responsible for this effect.

Another effect that we have observed is a difference in contact resistance for contacts made on freshly deposited Mo and Mo from which CIS has been removed by scraping. The latter Mo sometimes exhibits a variable and higher contact resistance that we believe is due to selenization of the Mo surface.

Work is underway to solve these problems and hence to obtain module fill factors representative of intrinsic material quality.

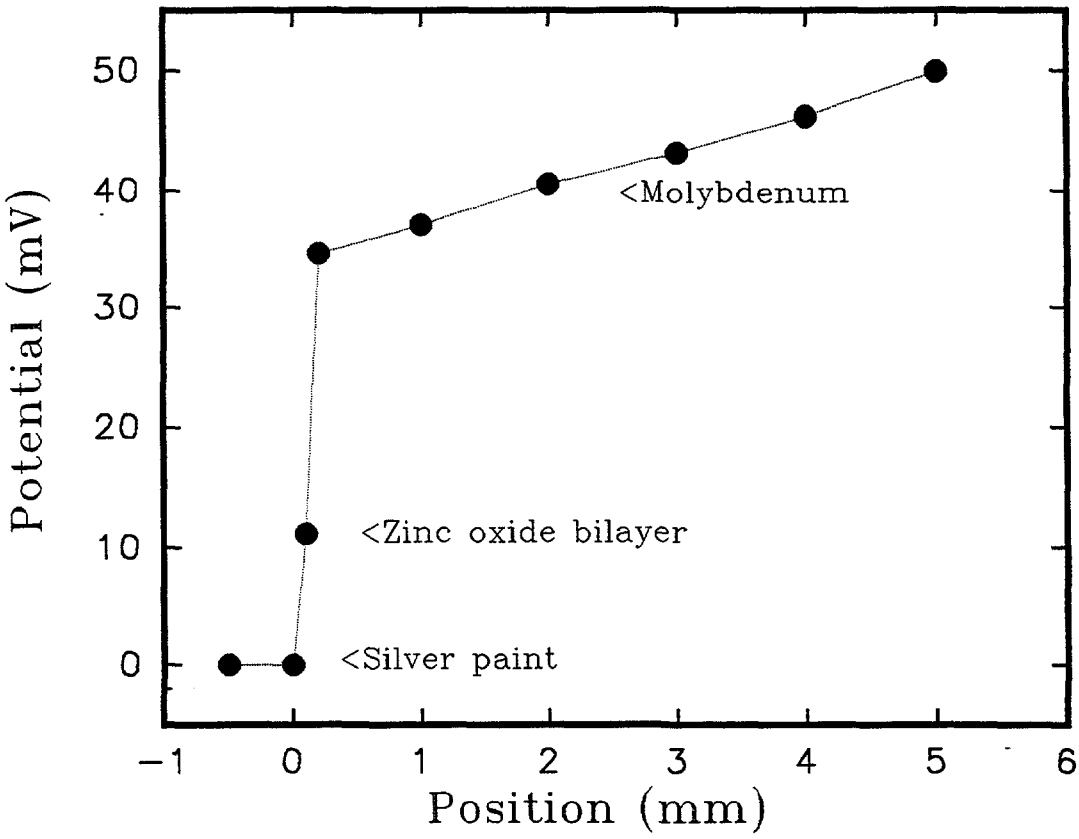


Figure 4.7 Potential as a function of distance in a test structure designed for examination of contact resistance at the ZnO/Mo interface

SECTION 5.0
CONCLUSIONS

Substantial progress in CIS technology was made during the first 8 months (Phase I) of this subcontract. The vacuum selenization process developed by EPV was shown to be self-stabilizing in that a) a $\pm$ 6% variation in precursor Cu/In ratio led to only a $\pm$ 3% variation in cell efficiency in the plateau region, and b) provided the amount of selenium evaporated exceeds a certain level, the exact amount is not critical. Environmental safety is ensured by the use of elemental selenium in the all-vacuum process compared to the hydrogen selenide (H_2Se) process which requires continuous monitoring and scrubbing.

After refinement of the rate/temperature/time profile for selenization an active area device efficiency of 10.5% was achieved for 1.10 cm^2 cell. These high efficiency cells employed a CdS window layer prepared by chemical bath deposition from acetate salts, and an AlF_3 anti-reflection coating. Three areas have been identified that should lead to further efficiency improvement. They are a) improvement of CIS quality leading to a longer minority carrier diffusion length and hence higher FF and J_{sc}, b) modification of the near-surface properties of the CIS and of the CBD CdS to further improve V_{oc}, and c) reduction of the ZnO optical absorption through the use of thinner films, optimization of the doping level, and choice of dopant (trading reduced carrier concentration for increased mobility) to improve J_{sc}.

The fabrication of 30.5 x 30.5 cm^2 (1 ft^2) modules was accomplished following scale up activities for the CBD CdS and ZnO, and the development of a laser patterning process for the molybdenum back contact. Active area efficiencies of 5.6% were achieved for 30 cm^2 modules. Diagnostics indicated the existence of substantial ZnO/Mo interconnect resistance in some modules, and work is under way to test various methods of minimizing the contact resistance.

SECTION 6.0
FUTURE PLANS

Our plans for Phase II fall into three main areas: further improvement of cell efficiency, the production of well-engineered modules, and scale up of the CIS to allow coating of 0.5 x 1.25 m^2 substrates. The route to higher cell efficiency has already been outlined in Section 5.0 above, and in this context we will further document the effect of CIS thickness. To achieve high module efficiencies, we intend to pay careful attention to issues such as layer thickness, uniformity, and reproducibility. In particular, we will strive for more accurate monitoring of substrate temperature during selenization, and a more uniform temperature distribution. Widening of the CIS band gap would be particularly advantageous for modules in order to reduce sheet resistance losses by trading lower currents for higher voltages. This we will seek to achieve through the use of $CuIn(Se,S)_2$. Finally, equipment will be designed, procured and assembled for metal deposition (Mo, Cu, In) and selenization on 0.5 x 1.25 m^2 substrates.

SECTION 7.0
ACKNOWLEDGEMENTS

The authors would like to thank A. Mason and D. Albin of the National Renewable Energy Laboratory for the EPMA and SEM analyses, respectively, A. Duda of the Colorado School of Mines for the x-ray diffraction of CIS, and D. Albin for coordinating these measurements. Thanks are due also to A. Nelson for ZnO transmission vs. wavelength, A. Franz for Auger analyses, and K. Emery's group for I-V and spectral response measurements. The x-ray diffraction of precursors was performed by H. Weakliem at Princeton University. At EPV, the other main contributors to this work were G. Butler, F. Faras, A. Sizemore, and F. Ziobro. We further acknowledge helpful discussions with K. Zweibel, R. Noufi, J. Tuttle, D. Albin, U. Choudary and R. Birkmire.

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Document Control Page	1. NREL Report No. NREL/TP-413-5334	2. NTIS Accession No. DE93000078	3. Recipient's Accession No.

4. Title and Subtitle

Non-H_2Se, Ultra-Thin CIS Devices

5. Publication Date
February1993

6.

7. Author(s)
A.E. Delahoy, J. Britt, and Z. Kiss

8. Performing Organization Rept. No.

9. Performing Organization Name and Address

Energy Photovoltaics, Inc. (EPV)
P.O. Box 7456
Princeton, New Jersey 08543

10. Project/Task/Work Unit No.
PV331101

11. Contract (C) or Grant (G) No.

(C) XG-2-12051-1

(G)

12. Sponsoring Organization Name and Address
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

13. Type of Report & Period Covered

Technical Report
10 March 1992 - 9 November 1992

14.

15. Supplementary Notes
NREL technical monitor: H. S. Ullal

16. Abstract (Limit: 200 words)

This report describes work done during Phase I of a 3-phase, cost-shared contract. The objective of the subcontract is to demonstrate 12% total-area efficiency copper indium diselenide (CIS) solar cells and 50-W CIS modules averaging at least 8 W/ft^2 in the third year. At the end of Phase I, EPV delivered to NREL a 1.1 cm^2 CIS cell with an active area efficiency of 10.5%. The correspondong total-area efficiency is 7.9%.

17. Document Analysis
a. Descriptors
copper indium diselenide ; thin devices ; photovoltaics ; solar cells

b. Identifiers/Open-Ended Terms

c. UC Categories
273

18. Availability Statement
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

19. No. of Pages
71

20. Price
A04

Form No. 0069E (6-30-87)