NREL/TP-451-5353 • UC Category: 272 • DE93000096

Low-Cost, High-Efficiency Solar Cells Utilizing GaAs-on-Si Technology

Annual Subcontract Report
1 August 1991 – 31 July 1992

NREL/TP--451-5353

DE93 000096

S. M. Vernon
Spire Corporation
Bedford, Massachusetts

NREL technical monitor: J. Benner

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
Operated by Midwest Research Institute
for the U.S. Department of Energy
under Contract No. DE-AC02-83CH10093

Prepared under Subcontract No. XM-0-19142-7

April 1993

MASTER

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

This publication was reproduced from the best available camera-ready copy
submitted by the subcontractor and received no editorial review at NREL.

NOTICE

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Printed in the United States of America
Available from:
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

Price: Microfiche A01
Printed Copy A03

Codes are used for pricing all publications. The code is determined by the number of pages in the publication. Information pertaining to the pricing codes can be found in the current issue of the following publications which are generally available in most libraries: *Energy Research Abstracts (ERA)*; *Government Reports Announcements* and Index (*GRA* and I); *Scientific and Technical Abstract Reports (STAR)*; and publication NTIS-PR-360 available from NTIS at the above address.

DISCLAIMER

Portions of this document may be illegible electronic image products. Images are produced from the best available original document.

TABLE OF CONTENTS

		Page
1	INTRODUCTION	1
2	GaAs-ON-Si USING ALE NUCLEATION	1
2.1	ALE of GaAs on GaAs	1
2.2	ALE of AlAs on GaAs	2
2.3	GaAs on Si with GaAs and AlAs ALE Nucleation Layers	4
2.4	Characterization of GaAs on Si grown with ALE Nucleation	6
3	GaAs ON SAWTOOTH-PATTERNED Si	11
3.1	Patterning by Holographic Lithography	11
3.2	Deposition of GaAs on Si	16
4	GaAs-ON-Si SOLAR CELLS	23

LIST OF ILLUSTRATIONS

Page

1 AlGaAs/GaAs/AlGaAs sandwich test structure for reflectance measurements 2

2 Sample output from REFIT(c) program 3

3 Summary of calibration runs made to determine GaAs monolayer per cycle growth conditions 3

4 Results of Calibration runs for ALE of AlAs 4

5 GaAs on Si by ALE nucleation test structure 4

6 X-ray FWHM vs. ALE nucleation layer thickness 6

7 D-H Structure used for minority carrier lifetime measurement experiments 7

8 X-ray FWHM for GaAs on Si vs. GaAs ALE nucleation film thickness before and after TCG 9

9 X-ray FWHM for GaAs on Si vs. AlAs ALE nucleation film thickness before and after TCG 9

10 Cross sectional TEM image of as-deposited ALE GaAs on Si film 10

11 Cross sectional TEM image of the as-deposited GaAs on Si film with a 15 minute anneal at 800°C 11

12 A schematic diagram of the holographic lithography set-up 12

13 A schematic diagram of the grating pattern transfer sequence 12

14a Cross sectional SEM of PR/ARC after RIE 14

14b Cross sectional SEM of Si_3N_4 grating mask after the removal of the PR and ARC 14

14c Si_3N_4 masked Si wafer after KOH etching 15

15 Cross sectional SEM of a sawtooth patterned, three-inch diameter Si substrate (0.2 μm period) at low magnification 15

16 Cross sectional SEM of GaAs on sawtooth patterned Si deposited using: a) a fifteen minute bake-out at 1000°C, and b) seven minute bake-out at 1000°C 17

LIST OF ILLUSTRATIONS (Concluded)

Page

17 Lifetime vs. FWHM of double heterostructure on Si 20

18 Lifetime vs. FWHM of post-thermal-cycle growth (TCG) layer on Si 20

19 Lifetime vs. FWHM of pre-thermal-cycle growth (TCG) layer on Si 21

20 Minority-carrier lifetime values for $Al_xGa_{1-x}As$-GaAs double heterostructures on Si vs. dislocation density measured by TEM 22

21 Design of the layers to be processed into solar cells 23

22 Cross-sectional transmission electron micrograph of GaAs film grown on sawtooth-patterned Si by a TCG process (wafer #M6-1167-3) 24

LIST OF TABLES

Page

I GaAs/Si: nucleation by GaAs ALE 5

II GaAs on Si samples for minority carrier lifetime measurements 8

III GaAs on patterned Si structures 17

IV GaAs on STP Si samples for minority carrier lifetime measurements 18

V Lifetime results for $Al_xGa_{1-x}As$-GaAs double heterostructures on Si 19

VI Dislocation densities (cm^{-2}) measured by planview TEM, and minority-carrier lifetimes measured by photoluminescence decay 22

1 INTRODUCTION

The overall goal of this research is to establish a technology to produce very-high-efficiency solar cells for terrestrial photovoltaic applications, using either multijunction or single-junction concepts. The approach pursued in this program involves the growth of GaAs and/or $GaInP_2$ materials onto Si substrates by the metalorganic chemical vapor deposition (MOCVD) technique. Efforts of our prior NREL contracts have resulted in the achievement of a GaAs-on-Si solar cell having a terrestrial efficiency of 21.3% at 200 suns.

This report covers the program year of October 1991 through September 1992. During this year we developed technology to deposit GaAs on Si using a nucleation layer of atomic-layer-epitaxy (ALE)-grown GaAs or AlAs on Si. This ensures two-dimensional nucleation, and should lead to less defects in the final GaAs layer. As an alternative, we also developed technology for depositing GaAs on sawtooth-patterned Si. Preliminary studies showed that this material can have a very low defect density ($\approx 1 \times 10^5$ cm^{-2}), as opposed to our conventionally grown GaAs on Si, which has a typical defect density of over 1×10^7 cm^{-2}. Using these two new methods of GaAs-on-Si material growth, we have made solar cells which are expected to show higher efficiencies than previous cells.

2 GaAs-ON-Si USING ALE NUCLEATION

2.1 ALE of GaAs on GaAs

The first task was to calibrate the conditions for depositing GaAs and AlAs by ALE; this was done on GaAs substrates. Twenty seven experiments on ALE growth of GaAs on GaAs, all in a SPIRE 450 low pressure MOCVD reactor, have been performed. The metalorganic precursors have been TMG, AsH_3 and TMA for Ga, As, and Al respectively. The films have been grown as sandwich structures consisting of a GaAs by ALE layer clad by AlGaAs (40%) deposited via standard MOCVD at 720°C as shown in Figure 1. The experiments were conducted at a baseline ALE cycle of 5 sec, 5 sec, 5 sec, 10 sec (TMGa, H_2 purge, AsH_3, H_2 purge). 106 cycles were used for the experiments. At the one monolayer per cycle conditions this corresponds to 300Å. N^+ GaAs wafers served as the growth substrates and were rotated at 20 rpm during deposition.

The films were characterized for thickness and composition by optical reflectance measurements using Spire REFIT(c) software. This is a powerful non-contact, non-destructive test for accurate characterization of AlGaAs/GaAs structures. The technique, based on near normal incidence specular reflectance, can provide both thickness and composition data required for process control and analysis. REFIT(c), developed at Spire, analyses the measured reflectance data and varies the thickness and composition parameters in a thin-film optical model of the wafer layer structure to fit the observed reflectance spectrum.

In order to confirm the accuracy of this technique, a AlGaAs/GaAs(ALE) sandwich structure was deposited with a GaAs thickness of 1000Å. The thickness of the ALE film was then determined by selectively etching a step on a photolithographically masked wafer. The selective etchant (NH_3OH:H_2O_2, PH=7) only etches GaAs. The thickness of the ALE layer was then measured using a Dektak stylus profilometer as well as the optical reflectance technique.

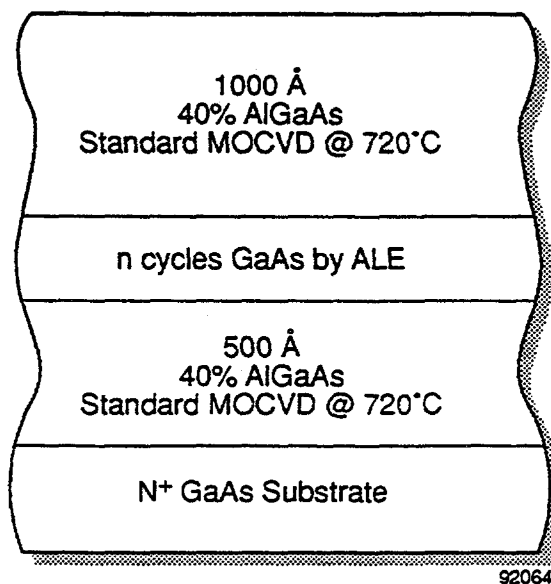


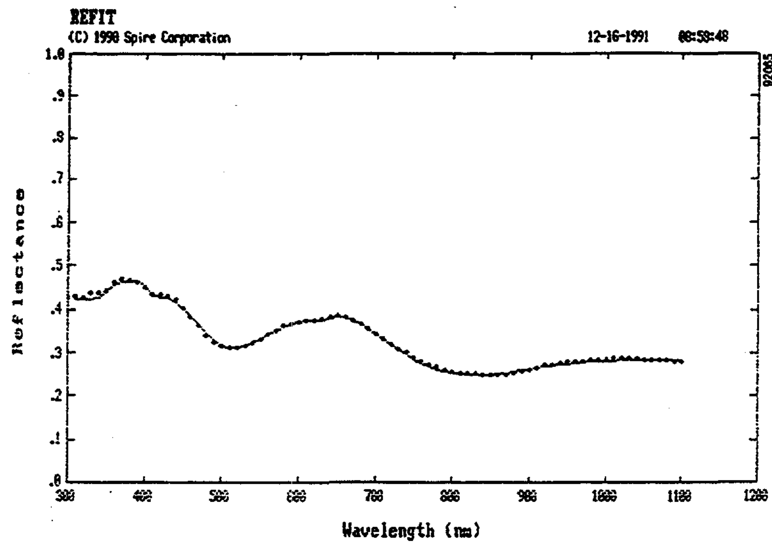
Figure 1 *AlGaAs/GaAs/AlGaAs sandwich test structure for reflectance measurements.*

Excellent agreement was achieved for the two methods. Optical reflectance has been used on the reported experiments because it is non-destructive, accurate and can quickly map a wafer for uniformity. The test structure used for the ALE experiments was designed to maximize optical interference hence resulting in very accurate thickness measurements. A sample reflectance spectrum and calculated fit from the REFIT program taken on a current AlGaAs/GaAs (ALE) sample appears in Figure 2.

Figure 3 shows the results of these runs. It can be seen that the one mono-layer per cycle condition for GaAs has been established at 450°C. The plot shows the maximum, minimum and average thickness measured on the samples.

2.2 ALE of AlAs on GaAs

These experiments were conducted in a similar manner to the ALE of GaAs. We chose to continue with the same ALE cycle (5,5,5,10) as used for the GaAs work. The AlAs layer thicknesses were measured by fitting the reflectance data from the sandwich structures to an optical model of the layers using Spire's REFIT[(c)] software as described last period. We grew the initial calibration runs on GaAs substrates for target thicknesses of 1000Å to help minimize any error in the reflectance data. Once the monolayer per cycle conditions were established, 300Å thick layers were grown to confirm the growth conditions prior to beginning work on Si. During the course of the experiments, the metal organic aluminum source was exhausted and a number of experiments had to be repeated. Figure 4 shows the results of the calibration runs. It can be seen that the monolayer per cycle condition is located at 470°C.



Input File Name: A:1070-2.REF Output File Name: NUL
Sample ID: MG-1070-2
Measurement Date: 12-16-1991 Time: 08:19:07 Data Points: 60 Wavelength Range: 310-1100 nm

File No.	F/A	File Name	N6328	Results X	90%CI	Thick	90%CI	Initial Values X	Step	Tol	Thick	Step	Tol
1	F	GASDKINK.DAT	.000	.000	(.000)	0	(5)	.000	.00	.001	0	.50	1
2	A	NUL	.000	.392	(.010)	921	(12)	.400	.10	.001	1000	.10	1
3	F	GAASNK.DAT	.000	.000	(.000)	220	(24)	.000	.00	.001	300	.10	1
4	A	NUL	.000	.399	(.015)	398	(33)	.400	.10	.001	500	.10	1
5	F	NUL	.000	.000	(.000)	0	(0)	.000	.05	.001	0	.00	1
6	F	NUL	.000	.000	(.000)	0	(0)	.000	.06	.001	0	.00	1
S	F	GAASNK.DAT	.000	.000	(.000)			.000	.06	.001			

Figure 2 *Sample output from REFIT(c) program.*

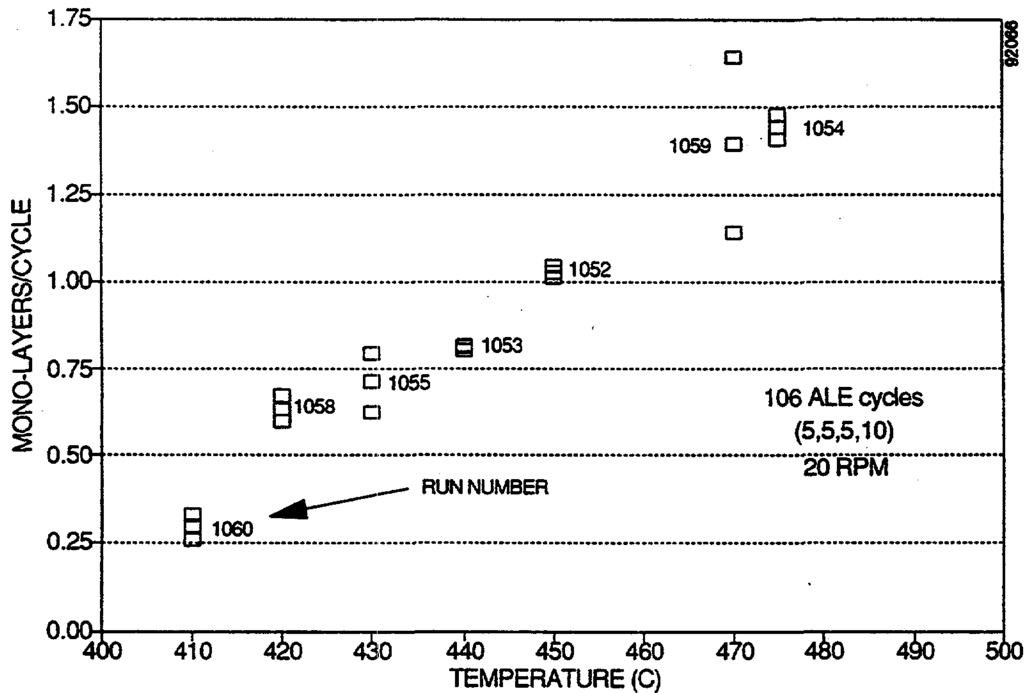


Figure 3 *Summary of calibration runs made to determine GaAs monolayer per cycle growth conditions.*

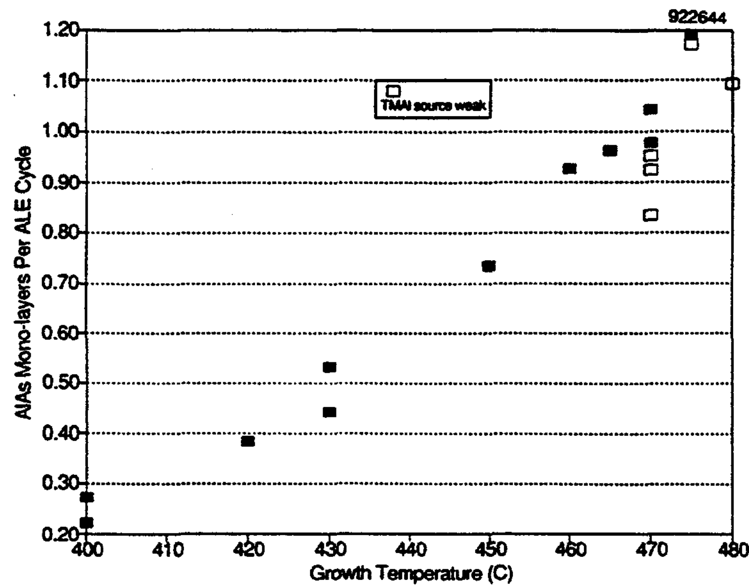


Figure 4 *Results of Calibration runs for ALE of AlAs.*

2.3 GaAs on Si with GaAs and AlAs ALE Nucleation Layers

With the monolayer per cycle conditions determined for both GaAs and AlAs, a matrix was established to grow nucleation layers by ALE, on Si substrates. The target thicknesses ranged from 25Å to approximately 300Å. A one micron GaAs cap was grown by conventional MOCVD on the ALE layers for X-ray measurements. Silicon substrates oriented at 2 degrees off and 4 degrees off the (100) towards the [110] were used. Figure 5 shows the structure.

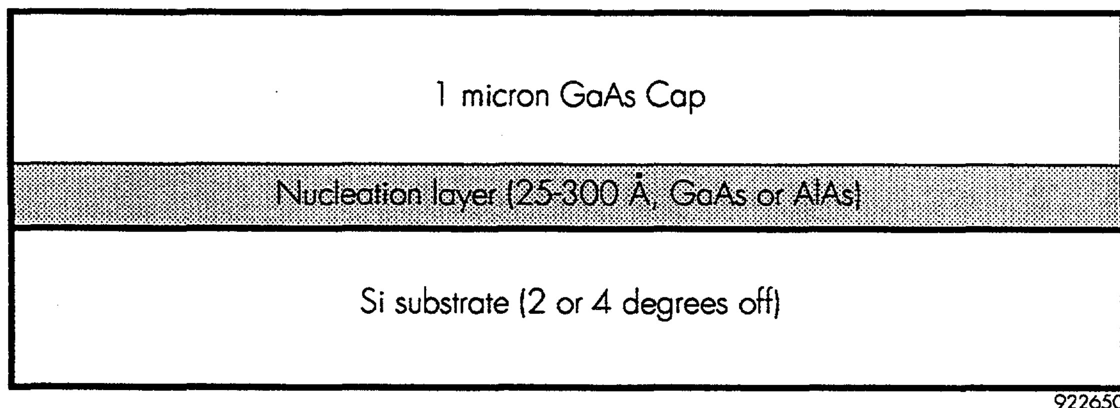


Figure 5 *GaAs on Si by ALE nucleation test structure.*

A programming error resulted in growth of a number of GaAs nucleation layers at 470°C (instead of 450°C). ALE of GaAs at 470°C has been calibrated at 1.4 monolayers per cycle therefore we have included these runs in our data. All samples were examined under bright light, photographed at 400X using Nomarski objectives and characterized using X-ray double crystal diffraction. Table I summarizes the structures and measured X-ray FWHM on the sample wafers. For these experiments, the layer thickness has been defined as the number of ALE cycles times the monolayer thickness (2.83Å). The average measured FWHM for both AlAs and GaAs ALE nucleation layers is plotted against nucleation layer thickness in Figure 6. As expected, the FWHM is reduced as the layer thickness is increased. Our results show that the AlAs layers have better overall X-ray characteristics as compared to the GaAs films.

Table I *GaAs/Si: nucleation by GaAs ALE.*

Run #	Thickness (Å)	Average (arcsec)	4° off (arcsec)	2° off (arcsec)	Temp. °C
1090	200	563	480	645	450
1095	25	770	840	700	450
1096	100	567	500	633	450
1097	50	717	733	700	450
1101	200	550	550	550	450
1113	280	492	440	544	470
1115	208	493	486	500	470
1117	142	542	537	547	470
1118	71	520	500	539	470
GaAs/Si: Nucleation by AlAs ALE					
1119	25	508	511	505	470
1120	200	441	463	419	470
1121	150	453	463	442	470
1122	100	453	442	463	470
1123	50	461	474	447	470

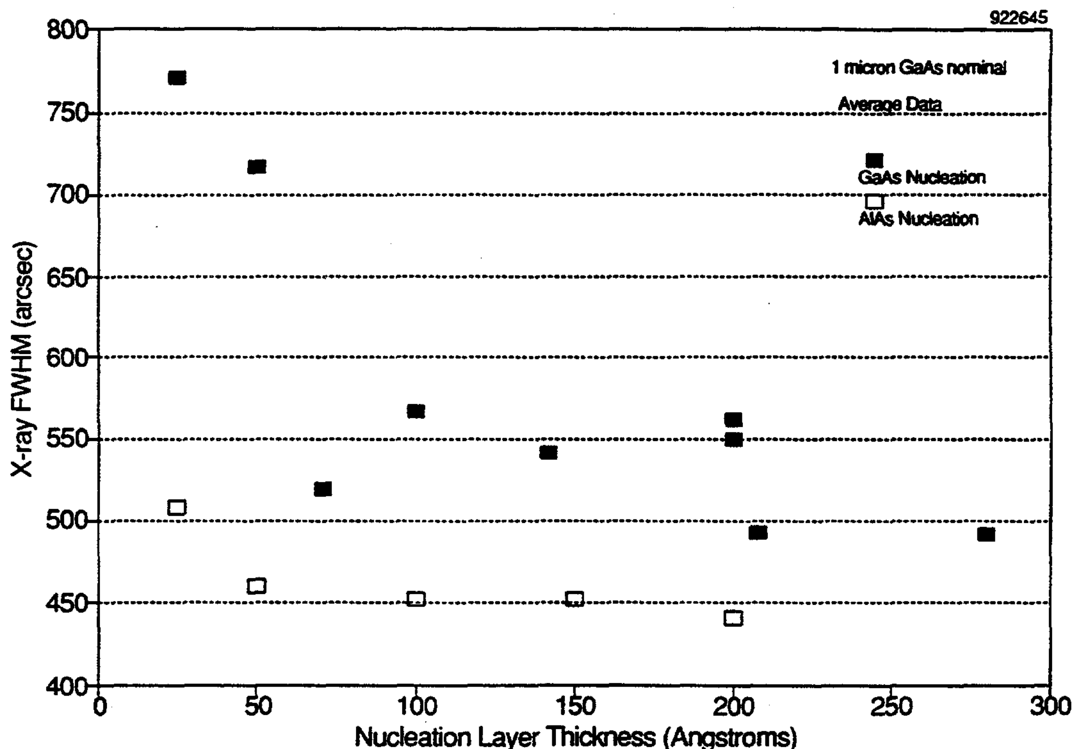


Figure 6 *X-ray FWHM vs. ALE nucleation layer thickness.*

2.4 Characterization of GaAs on Si grown with ALE Nucleation

GaAs on Si films have been deposited using ALE, for the deposition of the initial "nucleation" film, followed by conventional MOCVD. Both GaAs and AlAs nucleation films were used. A matrix of experiments was conducted in order to optimize the ALE nucleation film thickness on (100) Si substrates with 2° and 4° misorientation towards the <111> direction. nucleation film thicknesses in the range of 25-300Å were used. Thermal cycle growth (TCG) was employed to a number of most promising samples which were selected based on the surface morphology by Nomarski optical microscopy and the X-ray line width. We have compared the minimum ALE nucleation thickness successful in producing good surface morphology (18 ALE cycles = 50Å) to the typical ALE nucleation thickness used to produce high quality GaAs on Si (71 cycles = 200Å). AlGaAs/GaAs/AlGaAs double heterostructures (DH) were subsequently deposited on the TCG samples for minority carrier lifetime measurements. For each deposition condition, the DH structure was grown with two GaAs active region thicknesses (0.2 and 2 µm) for accurate minority carrier lifetime measurement. A schematic of these structures is shown in Figure 7.

A total of 20 samples (listed in Table II) were sent to NREL for minority carrier lifetime measurements and transmission electron microscopy. The first 20 samples deal with the GaAs and AlAs ALE nucleation. Table II also shows double crystal X-ray diffraction spectra for the 400 reflection full width at half maximum (FWHM) which is indicative of the crystalline perfection and can be correlated to a rough estimate of the defect density in the films. Figure 8 shows the X-ray FWHM for GaAs on Si as a function of the GaAs ALE "nucleation" film thickness and substrate orientation for as-deposited (1 µm thick) films and TCG films, 2.5 µm thick. For the

922646

30% AlGaAs, 0.3 microns, N-type 1e17 cm^{-3}
GaAs, 0.2 or 2 microns, N-type 1e17 cm^{-3}
30% AlGaAs, 0.3 microns, N-type 1e17 cm^{-3}
TCG GaAs (2.5 μm) on Si Substrate or GaAs Control

Figure 7 *D-H Structure used for minority carrier lifetime measurement experiments.*

as-deposited films, on the average the 4° off substrates seem to exhibit better surface morphology (compared to 2° off substrates) and narrower X-ray line widths which improve with increased nucleation film thickness. The surface morphology is very good for films with GaAs ALE nucleation thickness greater than 50Å (18 cycles). After TCG the surface morphology is improved and the X-ray line width drops to the range of 100-150 arcsec. The effects of substrate orientation become insignificant after TCG. Figure 9 shows a similar comparison as Figure 8, except that the initial ALE "nucleation" film is AlAs. In general, the GaAs on Si films with AlAs nucleation typically show improved surface morphology compared to GaAs nucleation. The X-ray line widths are typically 20-200 arcsec narrower for the as-deposited films and is independent of the substrate orientation. After TCG the X-ray FWHM improves, however the difference between the GaAs and AlAs nucleated GaAs on Si films becomes insignificant (5-10 arcsec).

We reported the deposition of GaAs on Si using a thin GaAs or AlAs (5-20 nm) atomic layer epitaxy (ALE) seed layer. We also grew a 300 nm thick GaAs film entirely by ALE at low temperature. In these experiments the wafers were first exposed to a high temperature bake out at 1150°C for 15 minutes followed by an arsenic initial monolayer; then the temperature was lowered to 450°C or 470°C where 1000 GaAs or AlAs ALE cycles were deposited. The ALE AlAs was subsequently capped with 10 nm of GaAs to prevent oxidation. The films were deposited on 2 and 4 degrees off substrates for comparison. Some of the wafers were subsequently exposed to post-growth annealing. The wafers were characterized using Nomarski optical microscopy and cross-sectional-transmission-electron microscopy (XTEM).

Table II *GaAs on Si samples for minority carrier lifetime measurements.*

DH RUN ID	SUBSTRATE ID						PRE-TCG	POST-TCG	POST-DH
0.2 µm GaAs	TCG RUN ID	NUCL RUN ID	ORIENTATION	NUCL TYPE	ALE TEMP	# ALE CYCLES	(arcsec) 1.0 µm GaAs	(arcsec) 2.5 µm GaAs	(arcsec) 1 µ/sec
M6-1162-1	M6-1158-2	M6-1097	2 DEG OFF	GaAs ALE	450°C	18 CYCLES	700	144.0	161.6
M6-1162-2	M6-1158-3	M6-1118	4 DEG OFF	GaAs ALE	470°C	18 CYCLES	500	159.3	156.2
M6-1162-3	M6-1158-4	M6-1123	2 DEG OFF	AlAs ALE	470°C	18 CYCLES	447	137.1	148.4
M6-1162-4	M6-1158-5	M6-1123	4 DEG OFF	AlAs ALE	470°C	18 CYCLES	474	133.4	145.6
M6-1162-5	GaAs control								
2.0 µm GaAs									
M6-1163-1	M6-1158-2	M6-1097	2 DEG OFF	GaAs ALE	450°C	18 CYCLES	700	144.0	97.9
M6-1163-2	M6-1158-3	M6-1118	4 DEG OFF	GaAs ALE	470°C	18 CYCLES	500	159.3	172.8
M6-1163-3	M6-1158-4	M6-1123	2 DEG OFF	AlAs ALE	470°C	18 CYCLES	447	137.1	123.3
M6-1163-4	M6-1158-5	M6-1123	4 DEG OFF	AlAs ALE	470°C	18 CYCLES	474	133.4	106.9
M6-1163-5	GaAs Control								
0.2 µm GaAs									
M6-1164-1	M6-1160-5	M6-1120	4 DEG OFF	AlAs ALE	470°C	71 CYCLES	463	137.7	226.9
M6-1164-2	M6-1160-2	M6-1090-1	2 DEG OFF	GaAs ALE	450°C	71 CYCLES	645	152.9	239.9
M6-1164-3	M6-1160-3	M6-1090-2	4 DEG OFF	GaAs ALE	450°C	71 CYCLES	480	139.5	167.8
M6-1164-4	M6-1160-4	M6-1120	2 DEG OFF	AlAs ALE	470°C	71 CYCLES	419	138.3	149.9
M6-1164-5	GaAs Control								
2.0 µm GaAs									
M6-1165-1	M6-1160-2	M6-1090-1	2 DEG OFF	GaAs ALE	450°C	71 CYCLES	645	152.9	117.8
M6-1165-2	M6-1160-3	M6-1090-2	4 DEG OFF	GaAs ALE	450°C	71 CYCLES	480	139.5	117.2
M6-1165-3	M6-1160-4	M6-1120	2 DEG OFF	AlAs ALE	470°C	71 CYCLES	419	138.3	118.1
M6-1165-4	M6-1160-5	M6-1120	4 DEG OFF	AlAs ALE	470°C	71 CYCLES	463	137.7	121.3
M6-1165-5	GaAs Control								

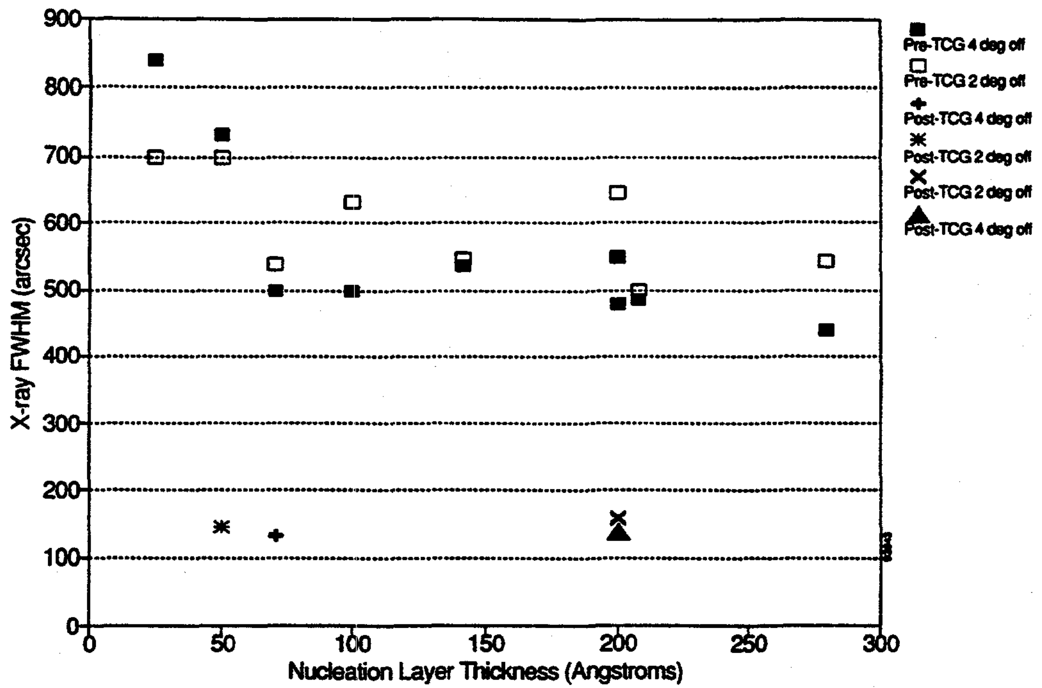


Figure 8 *X-ray FWHM for GaAs on Si vs. GaAs ALE nucleation film thickness before and after TCG.*

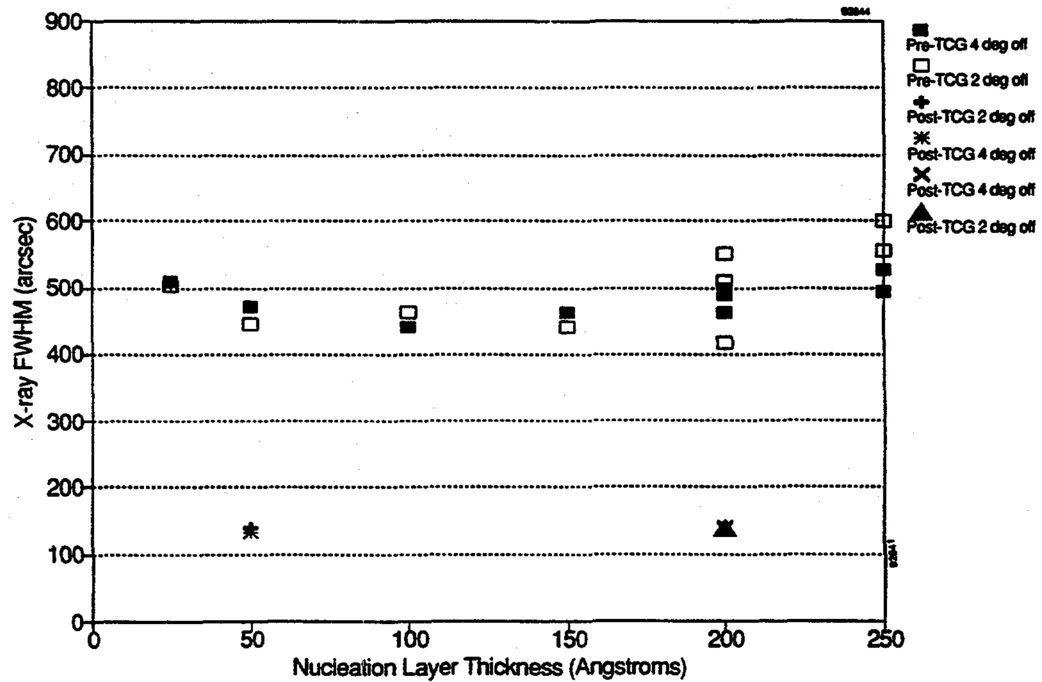


Figure 9 *X-ray FWHM for GaAs on Si vs. AlAs ALE nucleation film thickness before and after TCG.*

The surface morphology of the as deposited ALE films was found to be of exceptional quality for both GaAs and AlAs films. Most certainly it was superior to the best GaAs on Si deposited in our laboratory by conventional MOCVD. This is expected since the film is deposited at low temperature, therefore reducing the effects of the thermal-expansion-coefficient (TEC) mismatch between GaAs and Si. In fact a simple calculation can show that if the film is deposited around 400°C the GaAs film can be almost stress free at room temperature. Moreover, the strain in films deposited at around 450°C can be elastically accommodated. Figure 10 shows XTEM image of the as-deposited GaAs ALE film which is a high quality single crystalline film. To the best of our knowledge this is the lowest deposition temperature reported for GaAs on Si and the first report of ALE bulk film deposition on Si. No planar defects were observed, indicative of the two-dimensional nature of the ALE deposition process. Also a uniform array of misfit dislocations is observed at the GaAs/Si interface; such a feature is typically observed in annealed or TCG-deposited films. The thickness of the ALE film was measured using XTEM and found to be approximately 0.28 microns, corresponding to 1000 ALE cycles. Figure 11 shows a XTEM image of the same sample after a 15 minute anneal at 800°C in an arsine over-pressure. A high density of planar and threading dislocations was observed which may be due to the GaAs/Si TEC mismatch actually deforming the film during the high temperature anneal.

Figure 10 *Cross sectional TEM image of as-deposited ALE GaAs on Si film.*

Figure 11 *Cross sectional TEM image of the as-deposited GaAs on Si film with a 15 minute anneal at 800°C.*

The ALE AlAs/GaAs films also had excellent surface morphology, however the GaAs cap was not sufficient to protect the AlAs from oxidation. Utilization of thicker ALE GaAs caps will prevent oxidation. It is believed that if the epitaxial GaAs on Si films are deposited at sufficiently low temperatures, high crystalline perfection films can be achieved without resorting to thermal annealing approaches. Interestingly, GaAs on Si films deposited with conditions identical to those above, except that the films were deposited with conventional MOCVD instead of ALE, resulted in polycrystalline films. Details of these experiments will be reported later.

3 GaAs ON SAWTOOTH-PATTERNED Si

This report discusses GaAs on sawtooth patterned (STP) Si. The aim is to understand the mechanism of defect reduction/elimination and the role of the interfacial oxide in the GaAs on STP Si. Another important objective is to establish a reproducible deposition process that will preserve the STP and result in low defect density GaAs on large area Si (three-inch diameter) substrates.

3.1 Patterning by Holographic Lithography

The sawtooth patterning of three-inch and two-inch diameter silicon substrates with direct (100) orientation and 2-4° off the (100) towards the [111] has been achieved using a combination of holographic lithography and wet chemical etching. Figure 12 shows a schematic diagram of the holographic lithography set-up used for the present experiments, and Figure 13 shows the grating pattern transfer sequence used to form a Si_3N_4 mask with a 0.2 μm period on the Si substrate. The steps employed for sawtooth patterning of the Si substrate are outlined below.

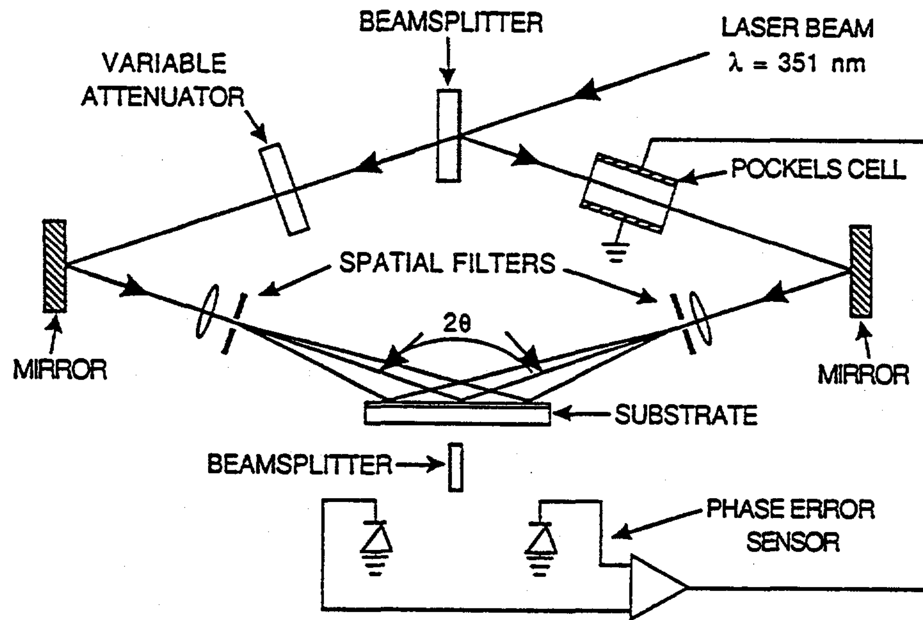


Figure 12 *A schematic diagram of the holographic lithography set-up.*

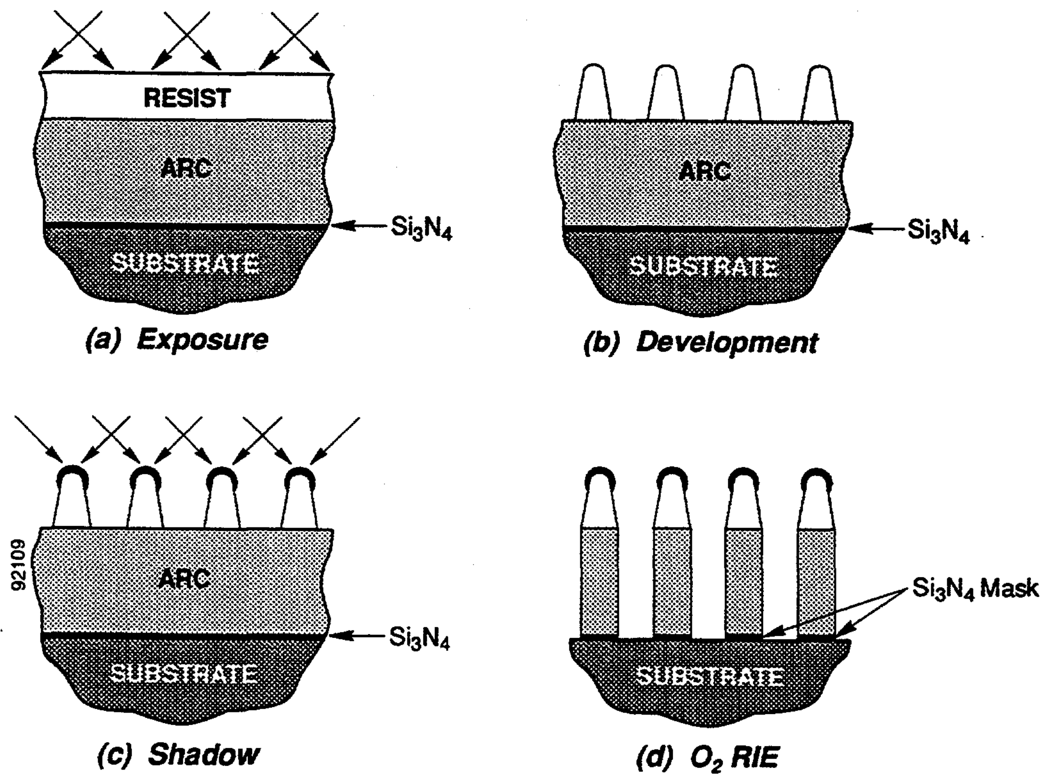


Figure 13 *A schematic diagram of the grating pattern transfer sequence.*

- 30-50 nm thick Si_3N_4 is deposited on the Si substrate using LP-CVD;

- Antireflection coating (ARC) and photoresist (PR) are then spun on the nitride layer;

- Holographic lithography is used to expose a 200 nm period grating into the PR (Figure 13a);

- After the PR development (Figure 13b), SiO_x is shadow evaporated from both sides at a 40° angle to act as a mask to the PR during subsequent etching steps (Figure 13c);

- Reactive ion etching (RIE) is used to etch the ARC (using O_2 as a gas) and the Si_3N_4 (using CF_4 as a gas) (Figure 13d). Figure 14a is a cross sectional scanning electron microscope (SEM) image showing the PR/ARC profiles after RIE;

- The substrate is subsequently cleaned in NH_4OH: H_2O_2: H_2O to remove the PR and the ARC;

- The remaining Si_3N_4 grating acts as a mask during KOH etching of the Si substrate, which anisotropically etches Si, exposing the (111) surfaces hence, generating a sawtooth pattern with a period of 200 nm. Figure 14b shows a cross sectional SEM image illustrating the Si_3N_4 grating mask after the removal of the PR and ARC. The grating has a period of 200 nm and acts as an effective mask for subsequent KOH etching. Wafers are then etched for 30 seconds in 4:1 H_20:HF to remove any oxide from the Si surface. This is immediately followed by a 2-3 minute etch in 2 molar KOH solution saturated with isopropyl alcohol, at 40°C. Figure 14c shows a cross sectional SEM of the Si_3N_4 masked Si wafer after KOH etching. The Si (100) plane is etched at a much faster rate compared to the (111) plane resulting a V-groove profile with (111) sidewalls. Lateral etching also results in undercutting the Si_3N_4 mask forming a sharp sawtooth pattern as shown in Figure 14c. Excessively long etching has been found to lift off the Si_3N_4 mask and planarize (destroy) the sawtooth pattern. The etching process if reproducible and is well behaved, independent of the wafer size.

- The wafers are then dipped in HF for two minutes to strip the nitride mask followed by a DI water rinse. Figure 15 shows a typical cross sectional SEM of the sawtooth patterned (100) Si substrate after nitride removal. It is clear from the SEM micrograph that the sawtooth pattern is very uniform, and since the pattern period is 200 nm, the wafers appear perfectly smooth and shiny under optical microscopy with a comparable appearance to unpatterned Si wafers.

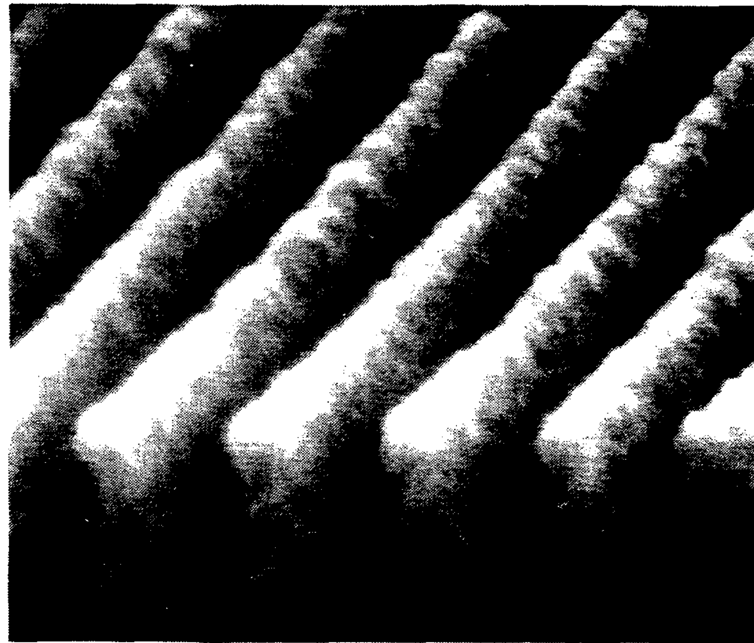


Figure 14a *Cross sectional SEM of PR/ARC after RIE.*

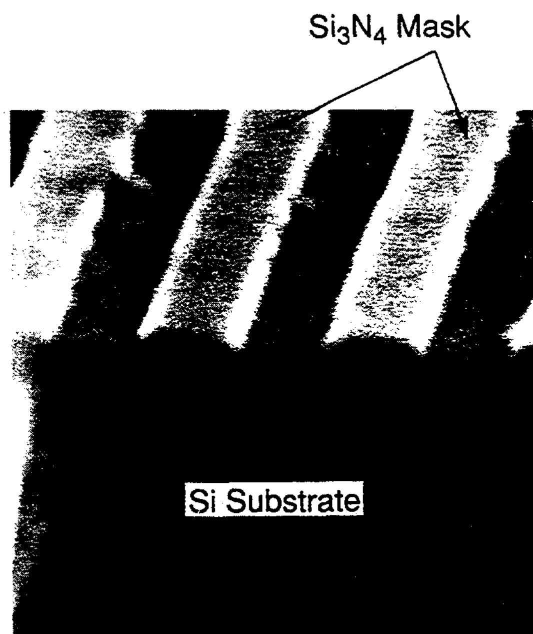


Figure 14b *Cross sectional SEM of Si_3N_4 grating mask after the removal of the PR and ARC.*

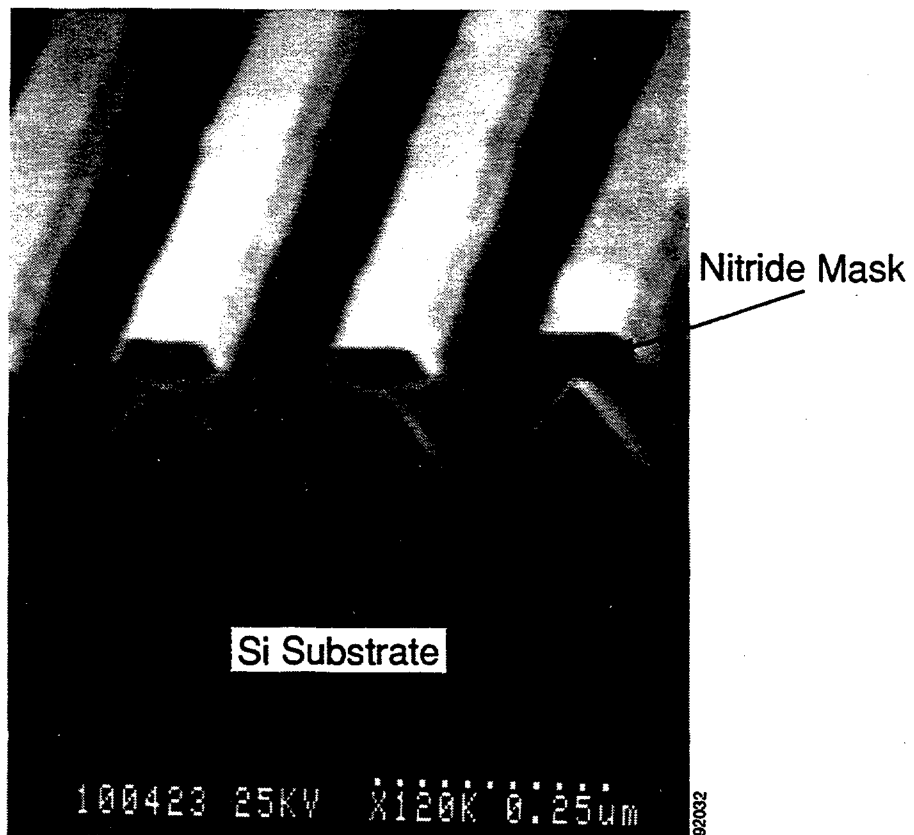


Figure 14c *Si_3N_4 masked Si wafer after KOH etching.*

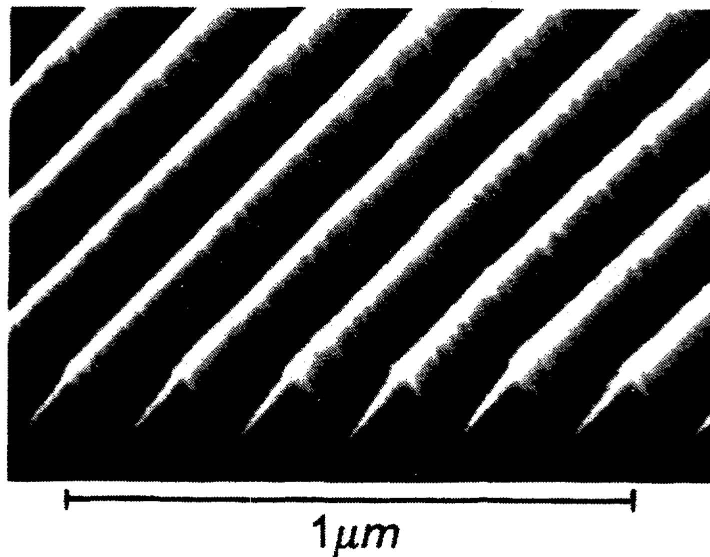


Figure 15 *Cross sectional SEM of a sawtooth patterned, three-inch diameter Si substrate (0.2 μm period) at low magnification.*

3.2 Deposition of GaAs on Si

The deposition of GaAs on STP Si was preceded by an *ex-situ* chemical clean of the wafers followed by a two-step deposition process. An *in-situ* high temperature bake-out (up to 15 minutes) was also used in some of the experiments for better cleaning of the substrate prior to the growth.

Wafer Chemical Clean - In order to prepare the patterned Si wafers for MOCVD growth, the wafers first go through a standard cleaning procedure including RCA clean, followed by a short etch with HF to ensure the formation of a reproducibly thin native oxide. The HF efficiently passivates the Si surface for 30 to 60 minutes, then a thin oxide (typically < 20Å, measured by ellipsometry) will grow on the sawtooth patterned surface. In all the experiments reported here, the wafers were loaded in the MOCVD immediately after the chemical clean to minimize the thickness of the native oxide.

High Temperature Clean - In conventional GaAs on planar Si wafers the Si is typically cleaned using a high temperature (1000°C) bake for a long time (typically 30 minutes) to remove the persistent native oxide. This high temperature step in H_2 was found to completely planarize the sawtooth-patterned surface possibly due to the much faster etch rate of the (100) Si compared to (111) planes, and/or the strong driving force to minimize the exposed surface area which is enhanced by the high surface mobility of Si at these high temperatures. The bake out temperature and time should be calibrated to remove the weakly bonded oxide from the (100 planes, yet prevent its removal from the (111) planes and/or the destruction of the patterned structure. A number of experiments were conducted to determine the bake-out conditions for the GaAs on patterned Si. Figure 16 shows cross sectional SEM of GaAs on sawtooth patterned Si deposited using a seven minute bake (Figure 16b) and a 15 minute bake-out at 1000°C (Figure 16a) in H_2. It is clear from Figure 16 that the longer bake-out time results in a diffused sawtooth pattern, while a short 7 minute bake preserved the pattern. By comparing Figures 15 and 16, it is clear that the seven minute bake is not optimal since the sawtooth pattern in Figure 16b is not as sharp as the as patterned wafer (Figure 15). A reproducible process was developed for GaAs on chemically cleaned STP Si without a high temperature bake-out.

GaAs on STP Si - A matrix of experiments was conducted where the deposition conditions for GaAs on STP on chemically cleaned Si were established with no bake-out in comparison to a short bake. Si wafers with two STP periods (0.2 and 0.35 µm) were used. The orientation of the STP grating was chosen to be normal to the major flat. The effect of the STP orientation will be reported later. Table III shows a list of GaAs-on-Si samples that were sent to NREL for TEM characterization. In general the as-deposited GaAs on STP Si samples are planar and have a mirror like surface morphology. The high temperature bake-out did not improve the surface morphology. For example, samples 1 and 2 (no bake) had similar surface morphology to samples 3 and 4 (7 min bake). Interestingly, the growth conditions developed for GaAs on STP Si result in polycrystalline film growth on unpatterned Si wafers. An AlGaAs/ GaAs superlattice (sample 2) was used to investigate the propagation of the growth front and planarization. Samples 5, 6, and 7 employed thermal cycle growth (TCG), to bring the total film thickness to 1.8 µm and for defect reduction purposes. Sample number 8 is intended to study the nature of the initial nucleation film (< 200 Å) without an interfacial oxide.

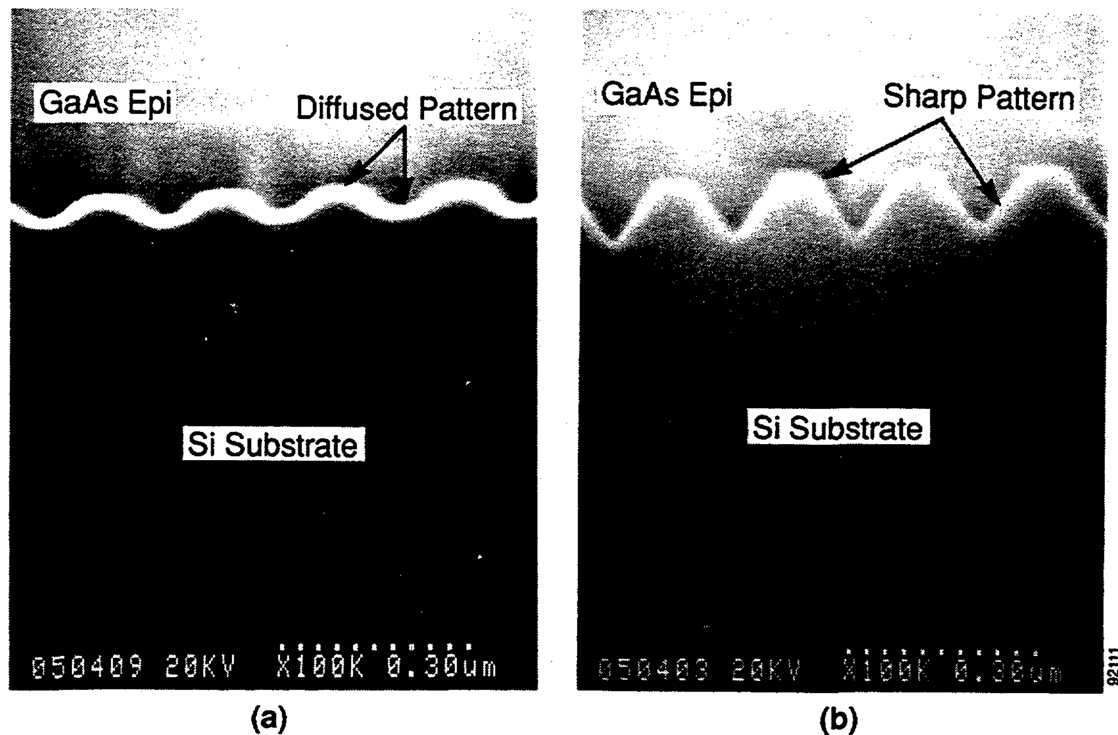


Figure 16 *Cross sectional SEM of GaAs on sawtooth patterned Si deposited using: a) a fifteen minute bake-out at 1000°C, and b) seven minute bake-out at 1000°C.*

Table III *GaAs on patterned Si structures.*

#	Run #	Wafer ID	Structure
1	M6-1031-3	0.2P1.1	GaAs on Patterned Si
2	M6-1032-3	0.2P2.4	SL-AlGaAs-GaAs/Si
3	M6-1033 #16	0.2P2.2	GaAs on Patterned Si+Bake
4	M6-1033	0.3P1.2	GaAs on Patterned Si+Bake
5	M6-1034	0.3P3.2	TCG SL-AlGaAs-GaAs/Si
6	M6-1034	0.2P1.3	TCG SL-AlGaAs-GaAs/Si
7	M6-1035	0.2P2.1	TCG GaAs on Patterned Si
8	M6-1047	0.2P3.4	GaAs Nucleation
9	M4-2068-1	A3-ST.2P1000	TCG GaAs on STP Si

A matrix of experiments was conducted for comparison of GaAs on STP Si, with the STP oriented parallel and normal to the substrate major flat direction (011). The wafers were all chemically cleaned using a HF etch as a final step and immediately loaded in the MOCVD reactor where a 1 µm thick film was grown using a two step deposition process with no bakeout. TCG was also performed to bring the total thickness of the film to approximately 2.0 µm. An $Al_xGa_{1-x}As$-GaAs double heterostructure structure was subsequently deposited. Table IV shows details of the deposited films and the X-ray data.

Table IV *GaAs on STP Si samples for minority carrier lifetime measurements.*

DH RUN ID	SUBSTRATE ID						PRE-TCG	POST-TCG	POST-DH
0.2 µm GaAs	TCG RUN ID	NUCL RUN ID	ORIENTATION	NUCL TYPE	ALE TEMP	# ALE CYCLES	(arcsec) 1.0 µm GaAs	(arcsec) 1.8 µm GaAs	(arcsec) 1 pt/sec
M6-1167-3	M6-1046-4	0.2 µm PERIOD PARALLEL TO FLAT						157.6	128.6
M6-1167-4	M6-1046-3	0.2 µm PERIOD PERPENDICULAR TO FLAT						118.1	170.2
M6-1167-1	GaAs Control								
2.0 µm GaAs									
M6-1168-3	M6-1046-4	0.2 µm PERIOD PARALLEL TO FLAT						157.6	149.0
M6-1168-4	M6-1046-3	0.2 µm PERIOD PERPENDICULAR TO FLAT						118.1	98.1
M6-1168-1	GaAs Control								

The 30 $Al_xGa_{1-x}As$-GaAs double heterostructure sample sent to NREL have been analyzed by Dick Ahrenkiel and Brian Keyes to determine the minority-carrier lifetime. The results are presented in Table V, along with the sample descriptions and the X-ray FWHM data measured at Spire. These lifetime values, up to ≈ 3 nsec, are the best we have ever achieved for GaAs on Si; our previous best results have been ≈ 2 nsec. In fact, these are the best ever measured at NREL for any GaAs on Si. We see from the data that the best lifetime values can be achieved using either the ALE-nucleation or the sawtooth-patterned-Si method. Further experiments, including making GaAs-on-Si solar cells, will decide which growth procedure is the better to pursue.

It appears that the X-ray values do not correlate with the measured lifetimes. These data are plotted in Figures 17 through 19, along with a linear-regression fit to the data points. It is interesting to note that the X-ray FWHM values of 98 arcsec achieved here are the best to date grown at Spire, and are among the best reported in the literature. No meaningful correspondence of lifetime to X-ray FWHM, measured either before or after the growth of the $Al_xGa_{1-x}As$-GaAs double heterostructure, can be seen. Looking at the table we note that the best lifetimes seem to occur in the thinner active layer samples. The substrate orientation, the nucleation type (GaAs or AlAs), and the number of ALE cycles in the nucleation layer appear to have no significant influence on the lifetime results.

Table V *Lifetime results for $Al_xGa_{1-x}As$-GaAs double heterostructures on Si.*

DH run # M6-	Orientation	NUCL type	ALE cycles	Life-time nsec
1162-1	2°	GaAs ALE	18	2.29
1162-2	4°	GaAs ALE	18	2.37
1162-3	2°	AlAs ALE	18	1.84
1162-4	4°	AlAs ALE	18	1.95
62-5				22.2
1163-1	2°	GaAs ALE	18	1.64
1163-2	4°	GaAs ALE	18	2.02
1163-3	2°	AlAs ALE	18	1.55
1163-4	4°	AlAs ALE	18	1.94
63-5				33.5
1164-1	4°	AlAs ALE	71	2.74
1164-2	2°	GaAs ALE	71	2.87
1164-3	4°	GaAs ALE	71	1.47
1164-4	2°	AlAs ALE	71	1.47
64-5				14.1
DH run # M6-	Orientation	NUCL type	ALE cycles	2.13
1165-1	2°	GaAs ALE	71	2.21
1165-2	4°	GaAs ALE	71	1.51
1165-3	2°	AlAs ALE	47710	1.46
1165-4	4°	AlAs ALE	47071	26.0
65-5				
1167-2	2°	GaAs ALE	1000	2.15
1167-3				2.59
1167-4				2.93
1167-5	4°	GaAs ALE	1000	1.97
67-1				13.8
1168-2	2°	GaAs ALE	1000	1.61
1168-3				2.32
1168-4				2.04
1168-5	4°	GaAs ALE	1000	1.88
1168-1				30.2

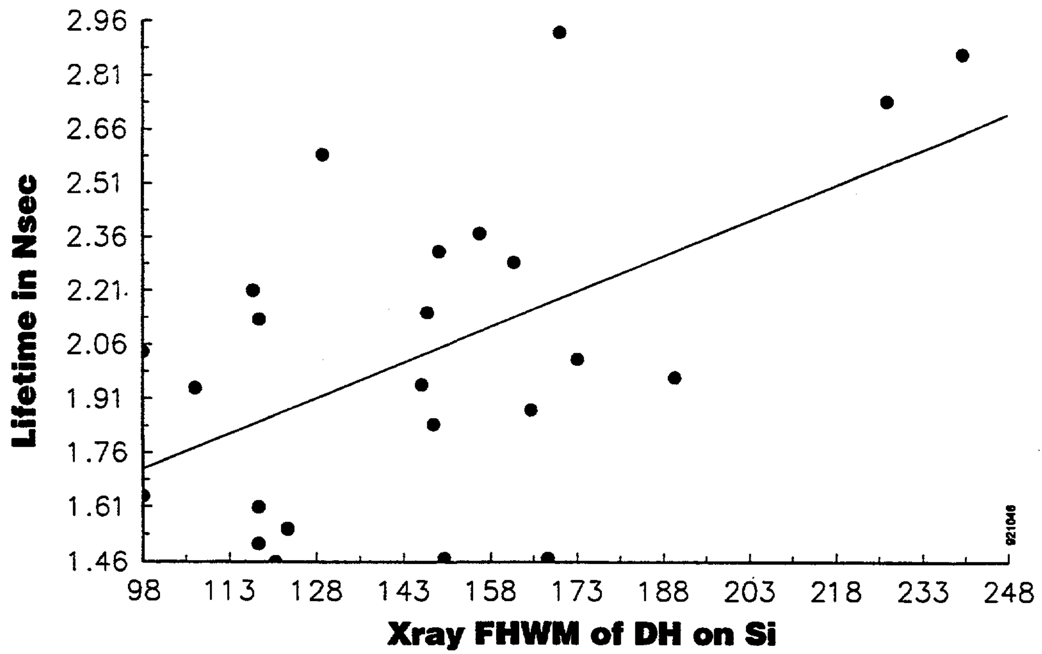


Figure 17 *Lifetime vs. FWHM of double heterostructure on Si.*

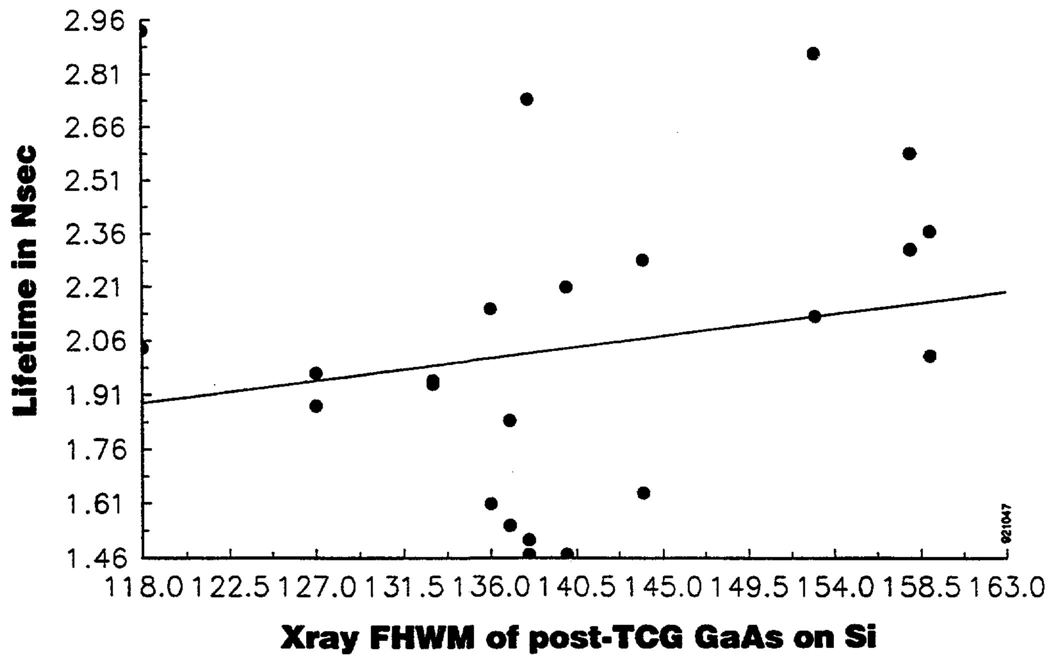


Figure 18 *Lifetime vs. FWHM of post-thermal-cycle growth (TCG) layer on Si.*

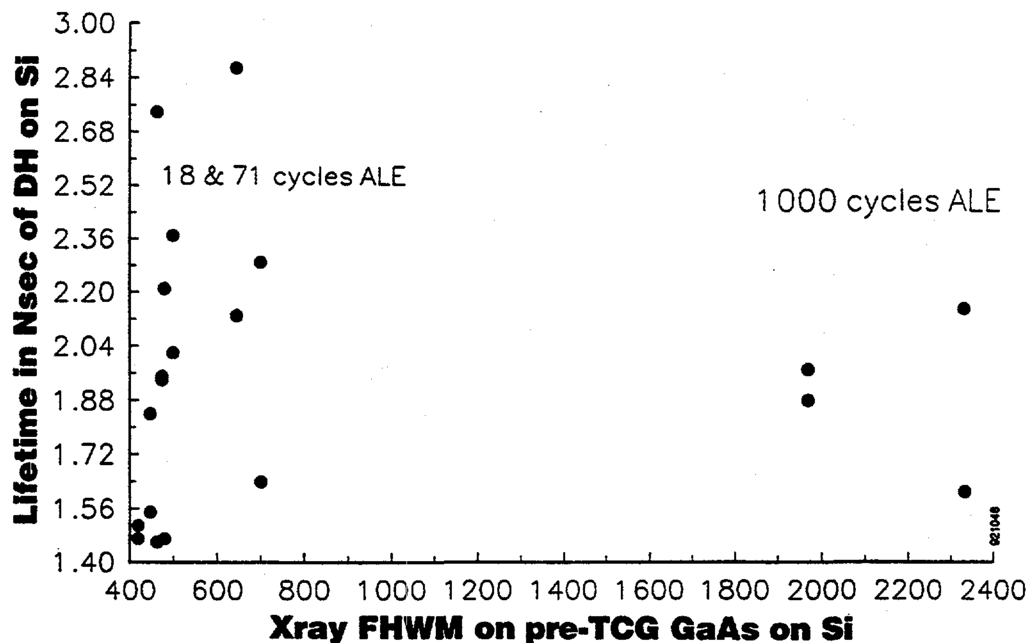


Figure 19 *Lifetime vs. FWHM of pre-thermal-cycle growth (TCG) layer on Si.*

- Run numbers M6-1162, 1164, and 1167 (see first column in table) have an $Al_xGa_{1-x}As$-GaAs double heterostructure with the GaAs layer being 2000Å thick; numbers 1163, 1165, and 1168 use a GaAs active-layer thickness of 2.0 µm in the DH.

The most interesting samples of $Al_xGa_{1-x}As$-GaAs double heterostructures grown on Si, as described above have been examined by planview transmission electron microscopy at NREL, in the laboratory of Dr. M.M. Al-Jassim. The dislocation densities determined are shown in Table VI, along with the minority-carrier lifetime values measured by Dr. R.K. Ahrenkiel at NREL. Excellent correlation between TEM and lifetime results is found, as shown in Figure 20.

Table VI *Dislocation densities (cm^{-2}) measured by planview TEM, and minority-carrier lifetimes measured by photoluminescence decay.*

Sample	Nucleation. Layer	Lifetime	Active DH Thickness	Dislocation Density (cm^{-2})
M6-1167-4	Sawtooth	2.93 nsec	0.2 μm	1-2 E7
M6-1164-2	71 cycle GaAs ALE	2.87 nsec	0.2 μm	1-2 E7
M6-1164-1	71 cycle AlAs ALE	2.74 nsec	0.2 μm	1-2 E7
M6-1168-4	Sawtooth	2.04 nsec	2.0 μm	≈ 3 E7
M6-1163-1	18 cycle GaAs ALE	1.64 nsec	2.0 μm	≈ 5 E7
M6-1164-3	71 cycle GaAs ALE	1.47 nsec	0.2 μm	≈ 5 E7

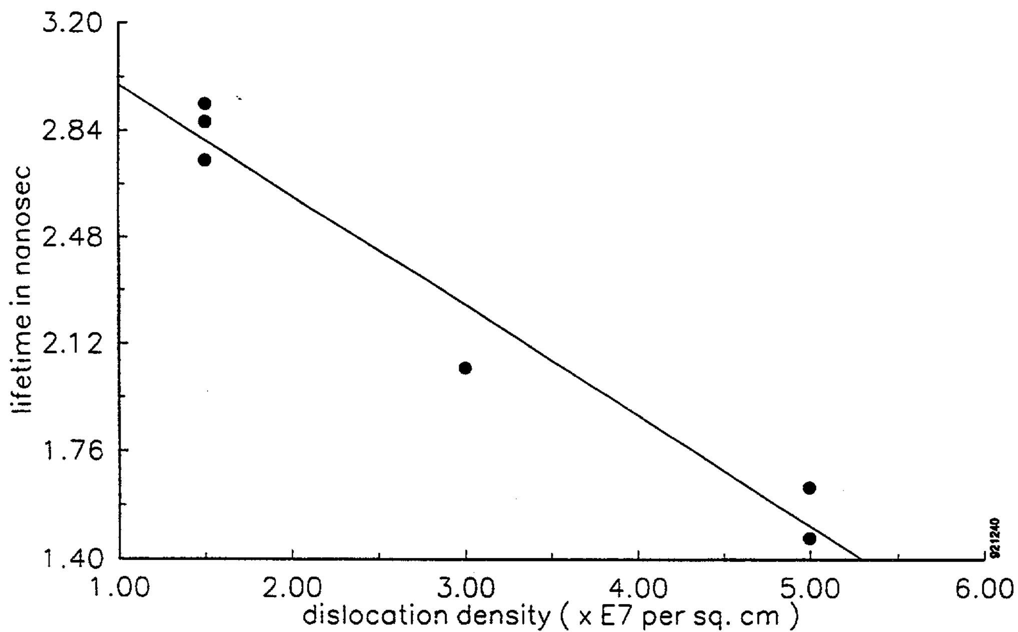


Figure 20 *Minority-carrier lifetime values for $Al_xGa_{1-x}As$-GaAs double heterostructures on Si vs. dislocation density measured by TEM.*

We received from NREL 34 cross-sectional transmission electron micrographs, detailing the structure of 18 samples of GaAs on Si. These samples cover a wide array of growth recipes, including both the sawtooth-patterned-Si and atomic-layer-epitaxy-nucleation techniques. These XTEM data are critical for understanding how to proceed with experiments aimed at reducing the dislocation density in GaAs on Si. One representative XTEM (GaAs on sawtooth-patterned Si) is shown in Figure 21; clearly visible is how the dislocations interact near the Si surface to quickly annihilate themselves, with only relatively few dislocations surviving to propagate through the upper GaAs regions. The beneficial interactions of dislocations near the GaAs-Si interface is a result of the sawtooth pattern and the thermal-cycle growth (TCG) process. This particular sample was measured to have a high minority-carrier lifetime value of 2.6 nanosecond. The high-quality XTEM work at NREL was conducted by M.M. Al-Jassim and Jane Zhu.

922647

Layer	Doping	Thickness
GaAs CONTACT P	$= 5x10^{19}$	3000 Å
GaAs CAP P	$= 1x10^{19}$	100 Å
$Al_{0.8}Ga_{0.2}As$ WINDOW P	$= 2x10^{18}$	300 Å
GaAs EMITTER P	$= 3x10^{18}$	2500 Å
GaAs BASE N	$= 2x10^{17}$	3 µm
$Al_{0.3}Ga0_{.7}As$ BSF N	$= 2x10^{18}$	1 µm
GaAs BUFFER N	$= 2x10^{18}$	1 µm
N+ "SUBSTRATES" (Various structures)		

Figure 21 *Design of the layers to be processed into solar cells.*

4 GaAs-ON-Si SOLAR CELLS

We have produced GaAs solar cells for study; this experiment compares many growth processes, in a side-by-side device comparison. The substrate types being used represent our state of the art in GaAs on Si, and include wafers with ALE AlAs nucleation layers, wafers with GaAs nucleation layers, GaAs on sawtooth-patterned Si (with several different surface preparation recipes), GaAs on Si grown by our conventional, standard process, and bulk GaAs wafers as control samples. All structures use the thermal-cycle growth (TCG) annealing process to minimize dislocation density. The solar-cell epitaxial layer structure to be used on all wafers is shown in Figure 22; GaAs-on-Si growth variations are in the region labelled as "substrate." From many prior experiments, approximately fifteen wafers of various GaAs-on-Si designs have been selected, and have been used for cell fabrication and testing.

Figure 22 *Cross-sectional transmission electron micrograph of GaAs film grown on sawtooth-patterned Si by a TCG process (wafer #M6-1167-3). Most dislocations are entangled within 5000Å of the GaAs-Si interface, with only a few surviving to thread upwards through the GaAs.*

We have completed fabrication of this batch of GaAs cells for study; 20 wafers of GaAs-on-Si and GaAs-on-GaAs structures have been processed into solar cells. All process steps went well, with apparently no wafers lost to breakage or process errors. Test results will be available soon; these will provide valuable insight in determining the growth conditions which yield the best cell efficiencies, and also in revealing which characterization methods can best be correlated with cell results. We are hopeful, based on the high values of minority-carrier lifetime achieved this year, that our best GaAs-on-Si solar cell will exceed previous attempts by several efficiency percentage points.

Document Control Page	1. NREL Report No.	2. NTIS Accession No.	3. Recipient's Accession No.
	NREL/TP-451-5353	DE93000096	

4. Title and Subtitle

Low-Cost, High-Efficiency Solar Cells Utilizing GaAs-on-Si Technology

5. Publication Date
April 1993

6.

7. Author(s)
S.M. Vernon

8. Performing Organization Rept. No.

9. Performing Organization Name and Address

Spire Corporation
One Patriots Park
Bedford, MA 01730-2396

10. Project/Task/Work Unit No.
PV321101

11. Contract (C) or Grant (G) No.

(C) XM-0-19142-7

(G)

12. Sponsoring Organization Name and Address
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

13. Type of Report & Period Covered

Technical Report
1 August 1991 - 31 July 1992

14.

15. Supplementary Notes
NREL technical monitor: J. Benner

16. Abstract (Limit: 200 words)

This report describes work to develop technology to deposit GaAs on Si using a nucleation layer of atomic-layer-epitaxy-grown GaAs or AlAs on Si. This ensures two-dimensional nucleation and should lead to fewer defects in the final GaAs layer. As an alternative, we also developed technology for depositing GaAs on sawtooth-patterned Si. Preliminary studies showed that this material can have a very low defect density, $\approx 1 \times 10^5$ cm^{-2}, as opposed to our conventionally grown GaAs on Si, which has a typical defect density of over 1×10^7 cm^{-2}. Using these two new methods of GaAs-on-Si material growth, we made solar cells that are expected to show higher efficiencies than those of previous cells.

17. Document Analysis

a. Descriptors
low-cost ; high efficiency ; gallium arsenide ; silicon ; photovoltaics ; solar cells

b. Identifiers/Open-Ended Terms

c. UC Categories
272

18. Availability Statement
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

19. No. of Pages

31

20. Price

A03

Form No. 0069E (6-30-87)