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Development of Large-Area Monolithically Integrated Silicon-Film Photovoltaic Modules

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Abstract

The objective of this program is to develop Silicon-Film™ Product III into a low-cost, stable solar cell for large-scale terrestrial power applications. The Product III structure is a thin (<100 μm) polycrystalline layer of silicon on a durable, insulating, ceramic substrate. The insulating substrate allows the silicon layer to be isolated and metallized to form a monolithically interconnected array of solar cells (see Figure 1). High efficiency is achievable with the use of light trapping and a passivated back surface. The long term goal for the product is a 1200 cm^2, 18% efficient monolithic array. The short term objectives are improving material quality and fabricating 100 cm^2 monolithically interconnected solar cell arrays. Low minority carrier diffusion length in the silicon film and series resistance in the interconnected device structure are presently limiting device performance. Material quality is continually improving through reduced impurity contamination. Metallization schemes, such as a solder dipped interconnection process, have been developed that will allow low-cost production processing and minimize Rs effects. Test data for a 9 cell device (16 cm^2) have indicated a V_{OC} of 3.72 V. These first reported monolithically interconnected multicrystalline silicon on ceramic devices show low shunt conductance (< 0.1 mS/cm^2) due to limited conduction through the ceramic and no process related metallization shunts.

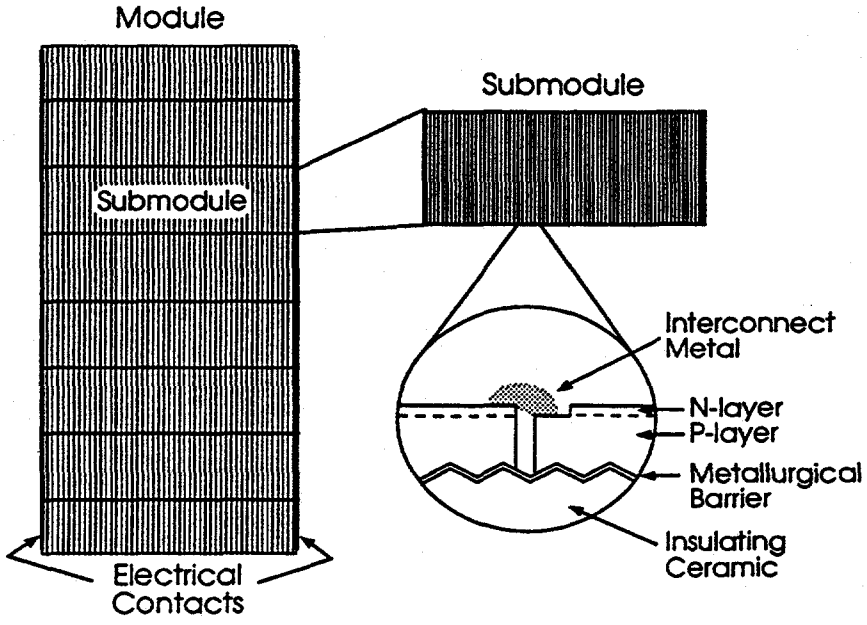


Figure 1. Silicon-Film™ Product III

1. Introduction and Objectives

Material quality has been the key issue in the development of Product III over the past year. Thin, large-grain polysilicon layers can be grown routinely on ceramic substrates using the Silicon-Film process. Minority carrier diffusion lengths, however, have been limited to less than 10 μm. Metallic impurities and dislocations are two potential causes being investigated in detail. Isolating impurity sources has resulted in recent improvements in L_n. Impurity sources have been identified in the bulk materials (both ceramic and silicon layer precursors) as well as in the silicon deposition process. Impurity segregation effects have been verified to have a significant impact in removing many metallic impurities.

The processing required to transform the thin silicon layers into integrated arrays is also being developed as part of this program. Issues for the monolithic integration process are: 1) developing a process sequence that does not introduce conduction paths through the ceramic and leaves the ceramic mechanically durable, and 2) developing low-cost metallization and array interconnection techniques. Significant progress has been made in each area.

1.1 Materials Development

Conductive ceramic substrates had been developed for the pre-existing Silicon-Film Product II effort [1]. They were developed, and are fabricated, in-house at AstroPower. That process has been adapted to the fabrication of insulating ceramics for the present Product III effort. The present fabrication sequence involves formulating the ceramic composition, tape casting into substrates (10 cm X 50 cm X 0.05 cm), sizing to 100 cm^2, and high temperature sintering. Ceramics are formulated from a proprietary mixture of readily available, low cost materials.

Through the development of the ceramic at AstroPower, significant expertise has evolved. This expertise has lead to the ability to control ceramic properties such as; thickness, uniformity, thermal properties, electrical conductivity, and surface texture. The conductivity of the ceramic was initially designed to be 0.5 to 2.0 Ωcm to provide electrical back contact on the single junction Product II structure. The Product III structure requires an insulating ceramic. The development of that insulating ceramic has led to the ability to control bulk electrical properties over a wide range by altering ceramic materials but leaving the fabrication process essentially identical. The ceramic development work is reviewed in section 3. This development work has included demonstrating increased ceramic size from 100 cm^2 to 500 cm^2. Increases to areas above 600 cm^2 will require upgrades to the equipment used for ceramic fabrication. Target resistivity for the Product III insulating ceramic is 40kΩcm.

As part of the Silicon-Film device, a metallurgical barrier (MB) is incorporated between the ceramic and active silicon layer. The barrier must play a number of critical roles in the physical and electrical nature of the device. Physically, the barrier must protect the active layer from impurities within the ceramic and be reflective to long wavelength light trapped in the active layer. Electrically, the barrier must provide a low recombination back surface to the active layer.

To increase absorption of long wavelength light in thin silicon layers, light trapping will be used. Detailed analysis of light trapping structures has been undertaken [2]. The general light trapping structures required for Product III will be similar to those developed for Product II. Through the use of back surface texturing (either random or regular) and metallurgical barriers of carefully designed reflective properties, high levels of light trapping have been achieved. The level of light trapping can be quantified by Z, the optical path length of the light given as a multiple of the device thickness. Optical properties have been measured in the present Product II structure to show a Z=9 has been achieved [3].

Silicon active layers are grown from a liquid in a controlled thermal environment. The precursors of the film are deposited on the ceramic in a separate process. Strict control of the ambient and thermal profile are required in this proprietary process.

1.2 Device Development

The ability to process continuous thin silicon layers, supported on an insulating substrate, into an integrated array is being developed. A key element in achieving such a structure is the ability to electrically isolate areas of the Silicon-Film wafer. The fact that the active device is only 100 microns thick and is supported by an insulating barrier-ceramic substrate allows this to occur. A contacting scheme has been designed to retrieve the generated power in any I-V configuration required. All electrical contacts are applied on the top of the device. Figure 1 shows one possible interconnection scheme. The cell size will be limited by resistive losses within the cell. Higher cell conduction in the n-layer can be achieved by the use of grids on the front surface. Increased p-layer conduction can be achieved by the use of back plane conductor. The development of a back plane conductor will require altering the barrier system to allow for the addition of a conducting plane beneath each cell. Care must be taken in the interconnection scheme to eliminate the possibility of shunting. The present process sequence is reviewed in detail in Section 4, Device Processing and Results.

2. Materials Processing Results

2.1 Material Quality

Minority carrier diffusion length (L_n) has been low (<10 μm) on grown silicon films. These multicrystalline films have grain sizes in the millimeter range, therefore minimizing the role of grain boundary recombination. The role of dislocations and impurities are being investigated in detail. That work is reviewed below.

2.1.1 Dislocation Density

Efforts have focused on understanding the role of dislocations in limiting device performance. The goal of the effort is to correlate dislocations measured by etch pit density (EPD) to device performance. The study is utilizing Silicon-Film layers on ceramic substrates and thermally-stressed float zone wafers. The single crystal wafers are heat treated by the same thermal schedule utilized to form silicon film layers.

Secco and Sopori etches are being used to delineate etch pits. Dislocations generated during the growth of the layers (during thermal cycling) and dislocations propagating from the ceramic substrate have been identified as two possible dislocation sources. Etch pit densities on controls (thermally cycled, no ceramic) range from 10^4 to 10^6 cm^{-2}. Diffusion lengths of these samples measured between 25 and 105 microns. Etch pit densities of silicon film-on-ceramic samples averaged $1.5x10^5$ cm^{-2} with high levels of clustering. Diffusion lengths typically average 5 microns, indicating that the poor material quality is not due to dislocations. This result is supported by the LBIC and EBIC data showing uniform intragrain response (see Section 2.1.3).

A summary of the data taken to date is shown in Figure 2. Included in the attached plot are data taken from the literature for similar studies. The AstroPower control data consist of over 100 mesa devices. The downward trend shows a slight dependence of Ln on dislocation density. It is interesting to note that data published by Ghitani and Martinuzzi [4] and Sopori [5] show a much stronger dependence of the diffusion length on the dislocation density than observed in the thermally stressed FZ silicon wafers. This may be due to the interaction of the dislocations with other lattice defects or metallic impurities which may result in a difference in the activity of the dislocations. Device size in this initial experimental sequence was 7×10^{-2} cm^2. The diffusion length was calculated from quantum efficiency curves. After determining the diffusion length of each mesa, the etch pit density was calculated by counting the delineated etch pits divided by the count area.

Silicon-Film results indicate high levels of dislocation clustering making numerical averaging difficult. The range of data measured is noted in Figure 2. The position of the Silicon-Film data, far below the results of the other material systems, indicates that low performance is not limited by dislocations alone.

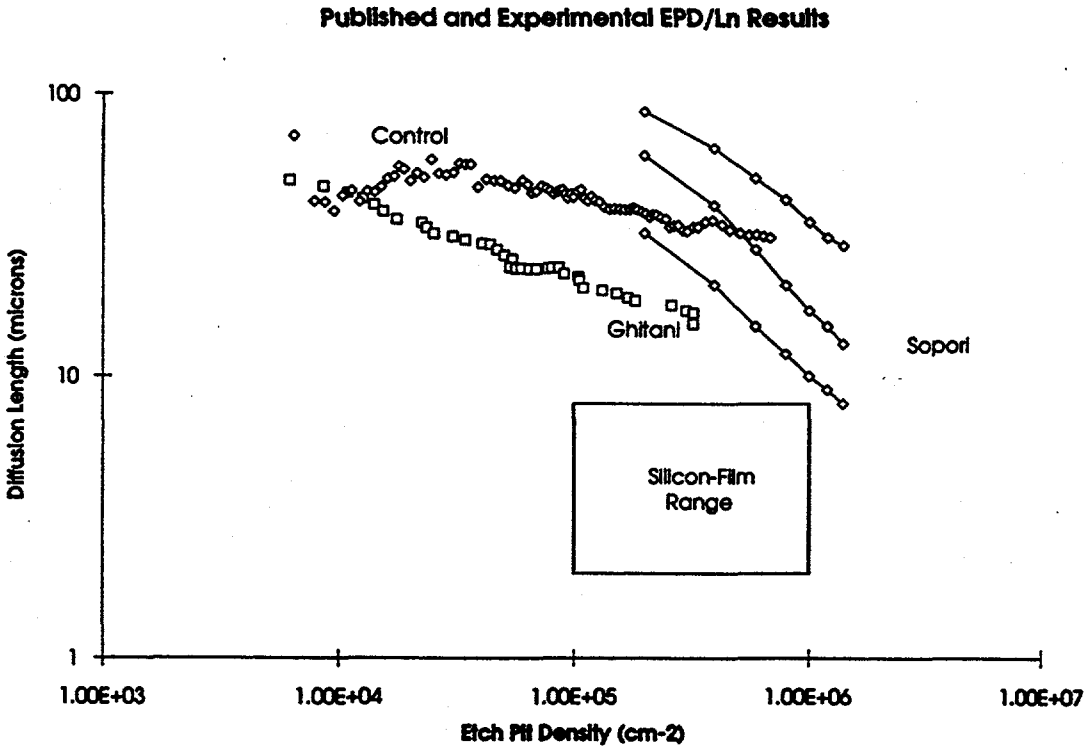


Figure 2. Published [4,5] and experimental dislocation density data.

2.1.2 Impurities and Concentrations

In order to track impurity contamination effects, silicon feedstock and finished layers have been evaluated by inductively coupled plasma - mass spectroscopy (ICP-MS). Using this chemical analysis technique, a number of contamination sources in the process sequence were identified. The silicon feedstock contains on the order of 4 ppm iron, introduced through particle size classification procedures.

Impurity levels were also determined for grown films. These data were obtained by selectively etching the silicon from the ceramic substrate and analyzing the resulting solution. Figure 3 summarizes the ICP-MS results for the substrate and the silicon film layer. The silicon deposition process has added aluminum, chromium, copper, and tungsten at the ppm level. All of the transition metals are known to have large segregation coefficients. After impurity segregation effects, all impurities except aluminum are below ICP-MS detection limits (typically 1 ppm). However, impurities such as tungsten could continue to have a significant adverse effect on L_n at such levels. Silicon-Film layers are approximately 100 μm thick with aspect ratios (grain width to height) on the order of 10 to 1. With these impurities present, diffusion lengths have been limited to 5 to 8 μm, and gettering processes have had no appreciable effect.

The sensitivity of the ICP-MS technique is approximately 1 ppm. This limits its usefulness for analysis of the grown films. SIMS analysis at NREL is planned.

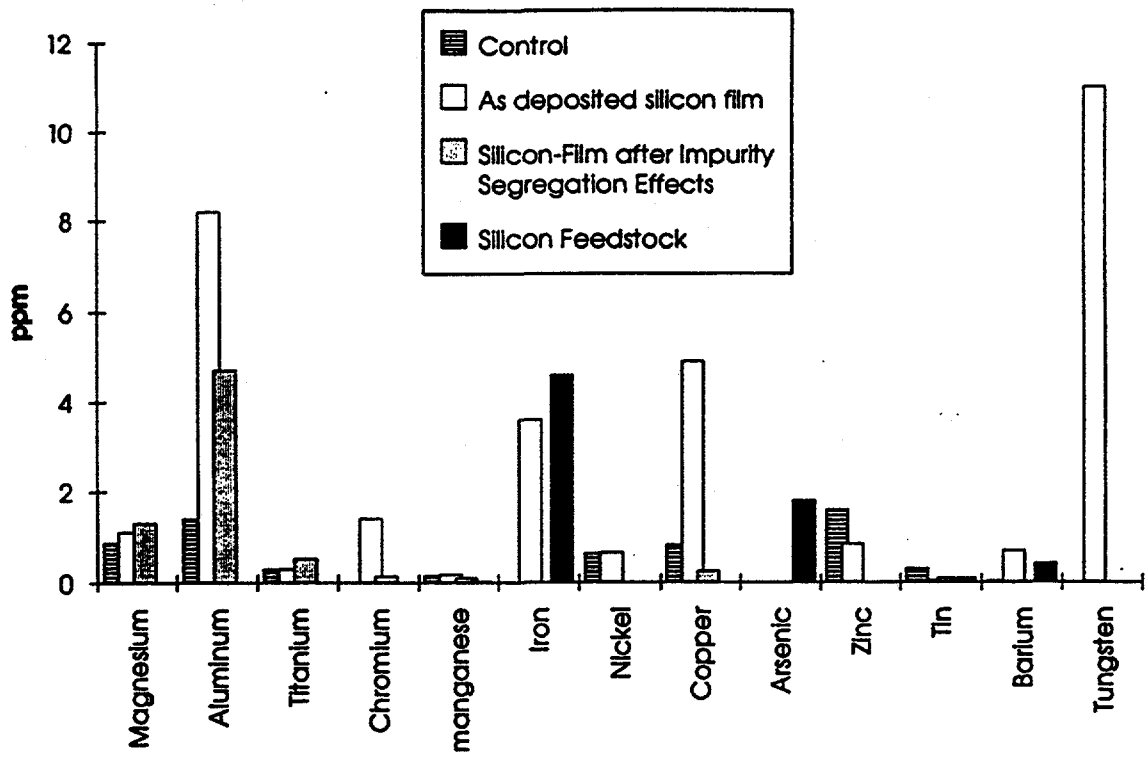


Figure 3. Broad based ICP-MS data

2.1.3 EBIC and LBIC Results

To further understand the impact of grain boundaries, dislocations or stacking faults, electron-beam induced current (EBIC) line scans and micrographs were generated by Rick Matson at NREL. A light beam inducted current (LBIC) has also been developed at AstroPower. The LBIC technique uses a 633 nm laser, and a probe size of approximately 100 μm. Initial results from these measurements indicate that photo-response is not limited by grain boundaries or other structural defects, but by a bulk effect.

To compare the EBIC and LBIC techniques, Silicon-Film samples were evaluated successively by both methods. The results for one mesa is shown in Figure 4. The EBIC image (Figure 4(a)) highlights the total active area. An aberration caused by probe shading can be seen in the middle of the device. Distinct lines of reduced response relating to grain boundaries can be seen running vertically through the device. A linescan is superimposed on the device. The zero reference is also shown, corresponding with the position of the line scan on the device. The magnitude of the intergrain response is very uniform. Grain boundary recombination is at small levels compared to total response. No significant intra-grain recombination centers are seen.

LBIC results for the same device are shown in Figure 4(b). The LBIC spot size (100 μm) and step size (75 μm) are far greater than that used in EBIC, therefore the resolution of the LBIC scan is much lower that the EBIC image. However, major

recombination features can be seen in both. Directly above the LBIC image is a line scan taken approximately through the center of the device (to correspond to the EBIC line scan). Both line scans indicate that grain boundary recombination is not a major photocurrent detractor.

2.2 Deliverables

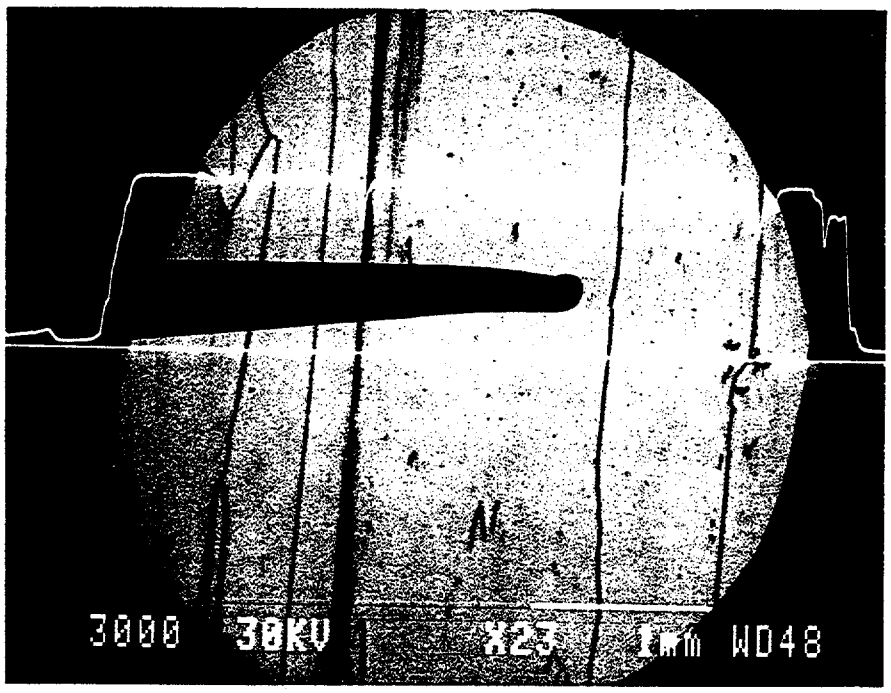
To demonstrate progress the following samples were delivered to NREL on January 8,1993;

1. 100 cm^2 conducting ceramic substrate.
2. 100 cm^2 insulating ceramic substrate.
3. 100 cm^2 conducting ceramic with metallurgical barrier attached.
4. 25 cm^2 Silicon-Film on ceramic sample demonstrating a thin silicon layer and high aspect ratio.
5. 16.1 cm^2 Silicon-Film on ceramic sample fabricated into a monolithic array. Our testing indicates a Voc = 3.72 V, Isc = 21.6 mA, and FF=0.512. The device has no anti-reflection coating. See "Process Development Below".

Deliverables 1 - 4 reflect the present state of development in terms of materials. Ceramic substrate formation is demonstrated with excellent dimensional control, as well as the ability to tailor ceramic resistivity over a large range (<500 Ω cm to >40 KΩ cm). The barrier layer is also demonstrated. Deliverable 4 demonstrates that aspect ratios (grain width/ film thickness) exceeding 10 are achieved in Silicon-Film material.

Deliverable #5 represents advances in monolithic interconnection and the resolution of many processing and metallization issues. Those issues will be discussed in Section 4, Device Processing and Results.

(a)



(b)

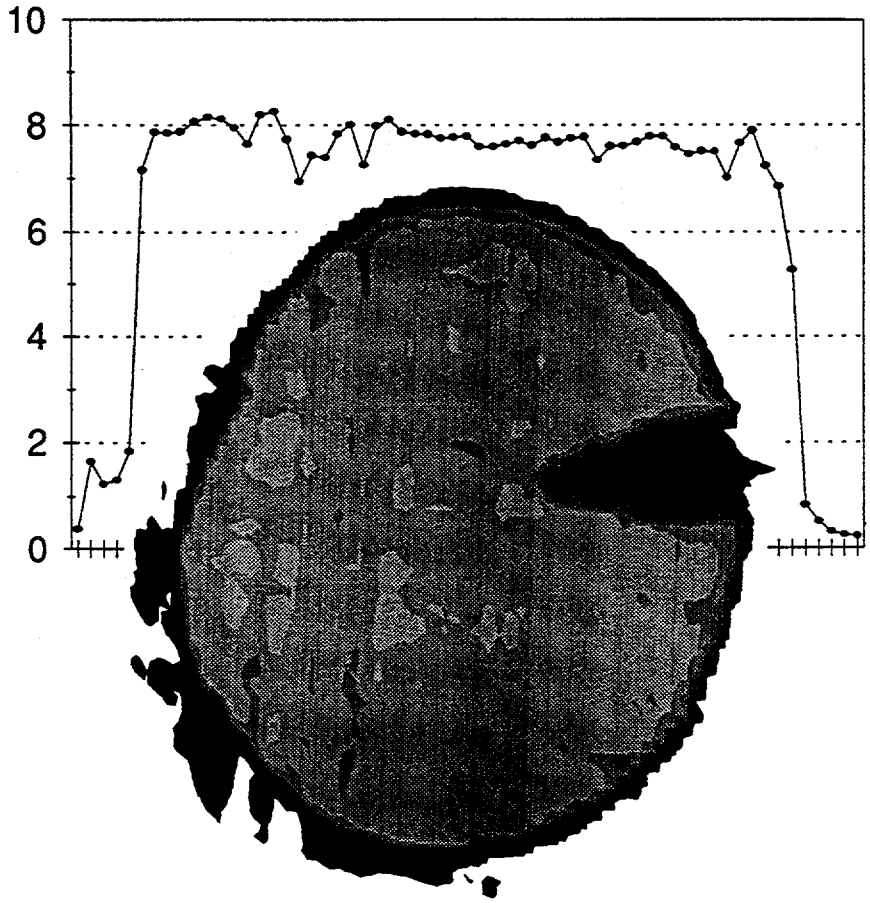


Figure 4. EBIC (a) and LBIC (b) images of the same mesa. Linescans for both devices are also shown.

2.3 Processing Enhancements

The deleterious effects of impurities on minority carrier properties remain the primary item to be addressed in the Silicon-Film device development. Chemical analysis work identified aluminum, copper, chromium, iron and tungsten as impurities in high concentration in the deposited silicon films. Impurities not removed by segregation effects during the growth process can potentially be removed or passivated by gettering. Tungsten is known to be a slow diffuser that does not passivate with gettering. This is consistent with previous results indicating that gettering does not improve minority carrier properties in Silicon-Film devices.

In an attempt to verify the impact of tungsten in the silicon layers, samples were fabricated using an alternate silicon deposition technique that is known not to contain significant levels of tungsten. Samples were fabricated and the impact of a phosphorus gettering process was measured in a controlled experiment. All devices made with tungsten free films were formed on the same ceramic substrate. One half was processed with a standard shallow emitter resulting in a sheet resistivity of 40 ohms per square, the other half was processed with a deep emitter (10 ohms per square). A summary of the results is shown in Figure 5. The material starts with an average L_n of 12.5 μm and increases to an average of 18.6 μm with gettering. The control set of devices, with tungsten present, has an average L_n= 6.3 μm and decreases to 5.6 μm with gettering (not shown in Figure 5).

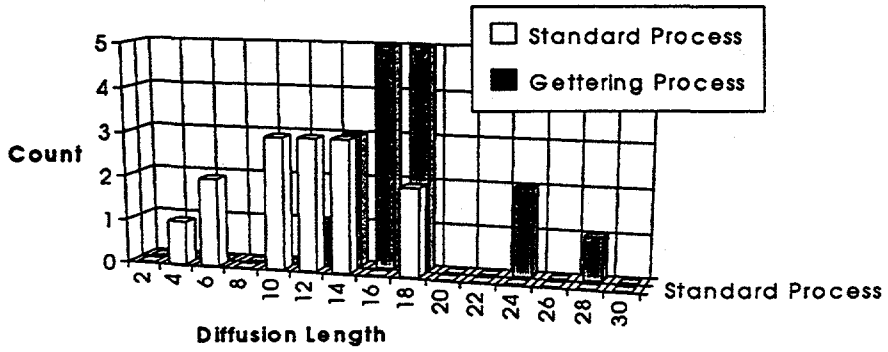


Figure 5. Effects of gettering on silicon layers known to be free of tungsten.

The deep emitter process has been known to benefit minority carrier properties in other multi-crystalline silicon materials, but has historically not benefited ceramic based Silicon-Film layers. The fact that diffusion lengths increased in this Silicon-Film material indicates that the poor minority carrier properties were being limited by a getterable impurity.

Passivation of bulk recombination sites is also being evaluated with hydrogenation. Experience to date has been that hydrogenation does not affect material that has a diffusion length less than 10 μm. This result can be understood if the recombination properties are driven by chemical impurities.

3. Ceramic Development

3.1 Ceramic Fabrication Process

The ceramic is fabricated from low cost materials using conventional ceramic methods. Ceramic powders of the appropriate particle size and purity are batch mixed with a water-based organic binder, then sieved to remove agglomerates. The resulting slurry is then tape-cast onto polyethylene coated aluminum setters using a laboratory scale tape casting unit with adjustable doctor blade assembly. Tape casting is a continuous process which is currently being done at the rate of 30 cm/min based on the viscosity of the slurry. The tape cast substrates are then dried in air at 100°C to remove volatile materials, and delaminated. The dried substrates, which are 45cm x 13cm x.12cm thick, are then trimmed and cut to the appropriate size. Our present capabilities are limited to 582 cm^2, however, with upgrades to the equipment ceramic size could be increased.

The sintering process is done in an electric furnace that utilizes silicon carbide heating elements in an argon atmosphere. In the first stage of the furnace binder burn-out occurs at 850°C, and in the second stage sintering occurs over 1300°C. Ceramic thickness is reduced by 40% due to shrinkage during firing, linear and cross dimensional shrinkage are negligible. The sintering process is a unique step that differs from conventional ceramic sintering processing in that we are able to suitably densify our ceramic very rapidly. The sample moves through the furnace which is 160 cm long, on a refractory setter at a rate of 15 cm/min. We are able to sinter at this rate because of the combination of materials used, and the fact that we do not need to achieve densities comparable to conventionally fired ceramics, resulting in low-cost fabrication.

3.2 Metallurgical Barrier Fabrication Process

The metallurgical barrier is fabricated from high purity dielectric materials. The dielectric, in powder form, is dispersed in a colloidal solution, then sprayed (atomized) onto the ceramic substrate at 100°C (substrate temperature). The substrate is fired at 1400°C in an argon atmosphere and is then ready for silicon deposition. Fired barrier thickness is 35-45 um. This barrier fabrication process yields an insulating barrier that is required for the PIII structure. For the PII structure the barrier must allow for ohmic back contact.

One of the difficulties in selecting a barrier material is finding one that allows wetting in the growth process. Dielectric materials, which consist primarily of metal oxides and nitrides, are typically difficult to wet with molten metals. Although we have fabricated devices, wetting of our current dielectric barrier is not reproducible and depends on variables such as powder particle size and surface texturing. Efforts are continuing to develop a barrier that is easily wet and exhibits the proper mechanical and electrical properties.

3.3 Ceramic Resistivity: Uniformity and Repeatability

Ceramic resistivity can be controlled by varying the composition of the ceramic, without giving up any of the mechanical strength. Resistivity of the Product II substrate is designed to be 0.5 to 2.0 Ωcm to the Product II structure. Product II substrates have been reproducibly fabricated with resistivities of 15 to 30 Ωcm to provide electrical back contact to the device. With a slight variation in the composition, the Product III substrate can reproducibly be fabricated with resistivities from 10K Ωcm to > 40K Ωcm. There are edge effects associated with the sintering process that affect the uniformity of the ceramic resistivity. The leading edge, corresponding to the direction of travel through the furnace, and both sides of the sample, which comprise about 15-20% of a 100 cm^2 sample, have low resistivities(< 2K Ωcm). It is believed that this is due to a thermal gradient during sintering that affects density. Development of the thermal profile during firing continues in an attempt to improve the uniformity of the ceramic resistivity, and to fabricate areas of localized conduction.

4. Device Processing and Results

Device-related research has focused on modeling the significant power loss mechanisms in the Product III device, and developing the key processes required for metallization. The base and emitter series resistance losses, and shading and kerf losses were identified as the most significant loss mechanisms. These losses were modeled to determine the optimum cell dimensions and contact pattern. The model is discussed in Section 4.1. The Product III processing uses standard solar cell processing techniques, with the exception of three process steps: the top base contact, the cell isolation, and the re-interconnection steps. Therefore, efforts have focused on these three unique process steps. Device processing is discussed in detail in Section 4.3.

4.1 Power Loss Modeling

The structure of the Product III device introduces two potentially significant loss mechanisms: contact shading losses (including the kerf loss of the isolation process), and emitter and base series resistance loss. An all-top contact design is necessary for the Product III device, since the ceramic substrate is not conducting and contact from the back is impossible. The extra metallization on the front of the cells increases the loss due to contact shading. In addition, the kerf loss associated with the isolation process reduces

the active area of each cell (dicing is typically used, resulting in about 4 mils of kerf loss per cell). These two factors can result in significantly higher shading losses compared to standard solar cell designs. This is offset by the reduced current generated in a interconnected array (as compared to a single junction device), which lowers the current carrying requirements on the metal systems. The second loss mechanism is due to the series resistance of the laterally connected cells. In general, the loss due to series resistance increases as the cell length is increased. Although the series connected configuration lowers the total current of the array, the power loss due to the series resistance can still be considerable, especially at longer cell lengths (> 10 cm).

The power loss model of the Product III device accounts for series resistance in the base, emitter, and grid lines as well as the shading loss due to the emitter grid and bus lines, the base bus line, and the kerf losses. The model inputs are relevant process-related information, such as emitter, base, and metallization sheet resistivities, bus and grid line widths, and isolation trench widths. The series resistance losses are calculated by integrating the I^2R loss over the active area of the device, where the limits of the integration account for the particular cell area and contact geometry. The shading losses are determined by the percent area covered by the contacts and the diced isolation trenches. The total loss is the sum of all loss mechanisms.

Three contact patterns were examined: no grid lines, emitter grid lines, and inter-digitated emitter and base grid lines. (Each of these three patterns utilizes a base bus line, which is necessary for the re-interconnection step.) The results of the model are plotted as a 3-D graph (see Figures 6 and 7), which shows the total power loss as a function of the device length and the grid line spacing.

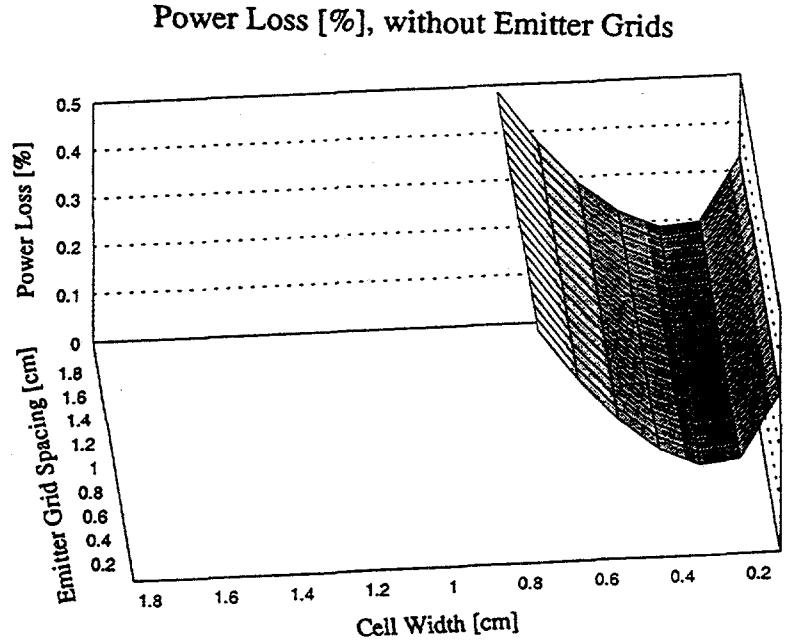


Figure 6. A 3-D plot of the significant loss mechanisms of the Product III structure for the case with no emitter or base grid lines. The relevant process parameters are inset.

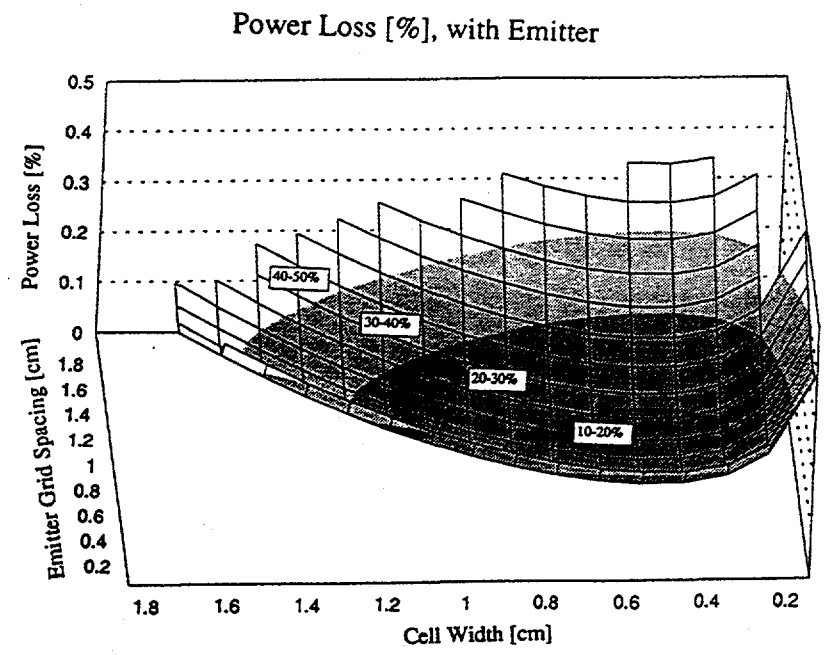


Figure 7. A 3-D plot of the significant loss mechanisms of the Product III structure for the case with emitter grid lines only. The relevant process parameters are inset.

The results of the modeling indicate that for a contact pattern that did not include an emitter or base grid pattern, the series resistance losses were unacceptable for cell lengths greater than about 0.2 cm (see Figure 6). This places a significant restriction on the allowable cell dimensions. An emitter grid lowered the total overall loss, but, more importantly, it diminished the strong dependence of the resistance losses on the cell width. This allows more flexibility in the design of the array. An additional base grid pattern would further reduced the total power loss, but only marginally. The base grid pattern was therefore omitted from the design due to the complexity of incorporating the interdigitated grid into the process sequence. Instead, the sheet resistivity of the base was lowered by using a thicker (300 micron), more heavily doped (0.3 ohm-cm) layer. The final design was optimized at a cell length of about 0.6 cm and an emitter grid line spacing of about 0.33 cm. With this design, total shading and series resistance losses are limited to about 15%.

4.2 Device Fabrication Procedures

With the exception of the top base contact, cell isolation, and re-interconnection steps, the Product III fabrication sequence uses standard solar cell processes. The current Product III fabrication sequence is illustrated in Figure 8. Many subtle variations of this sequence were evaluated during the last year. Process changes have been driven by efforts to simplify production and minimize resistance effects.

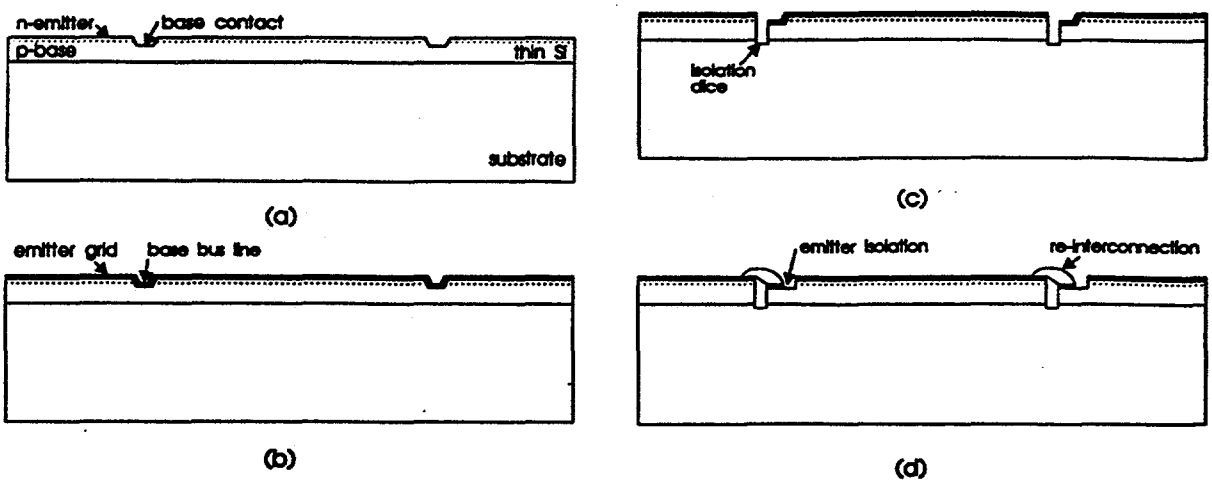


Figure 8. Product III fabrication sequence: (a) surface preparation and diffusion and base contact area definition, (b) metal evaporation and liftoff, (c) cell isolation, and (d) re-interconnection.

After surface preparation and diffusion, the base layer was exposed in a stripe pattern by using photolithography and a Freon-based plasma etch to remove 1 micron of silicon from the surface (a). This process allows the base contact metal to be in direct contact with the base layer from the top of the device. An alternative method of contacting the base from the top are discussed in section 4.2.2. Photolithography, evaporation and metal liftoff were used to define the contact pattern, with the base bus line aligned in the etched stripes and the emitter grid lines perpendicular to the base grid lines (b). The sample was then diced to isolate the individual cells, and mechanical saw damage was removed with a Freon-based plasma etch (c). Finally, the re-interconnection metallization was applied to connect the cells as a series-connected array (d). In some cases an additional dice was required to isolate the base contact from the adjacent emitter and emitter contacts. The details of these process steps are described in more detail in the following sections.

4.2.1 Diffusion and Emitter Etch Back

The Product III diffusion sequence currently employs a relatively high temperature deposition followed by a long drive-in time. This diffusion sequence improved the minority carrier diffusion lengths by gettering impurities as discussed in Section 2.3. The resulting low emitter sheet resistivity (15-18 ohm/□) was also beneficial in reducing the series resistance of the emitter. The diffusion preparation clean consisted of a weak hydroflouric-water ($HF:H_2O$ (1:10)) strip and deionized (DI) water rinse to remove any

oxides grown during the silicon layer formation. The surface was then cleaned in hot $HCl:H_2O_2:H_2O$ (1:1:1) for 15 minutes, and rinsed in DI water. Immediately prior to the diffusion, the samples were stripped in a weak hydoflouric-water and rinsed in DI water.

The pre-deposition was carried out at 890 °C for 42 minutes using $POCl_3$ as a dopant source gas in a carrier of nitrogen and oxygen. The drive-in step occurred in a nitrogen/oxygen ambient at 890 °C for 35 minutes. The resulting sheet resistivity was between 15 and 20 Ω/□. The phos-glass residue was removed with a weak hydroflouric-water strip and DI water rinse. An emitter etch back process was also developed to thin the emitter layer and improve the blue response of the cells, however, this process step has not yet been incorporated into the fabrication sequence. The process uses a weak $HF:HNO_3$ mixture (1:100) to controllably thin the emitter. Typically, 30-40 seconds were required to change the emitter sheet resistivity from 10-15 Ω/□ to 50-60 Ω/□. This will be incorporated when the other key processes are well developed.

4.2.2 Top Base Contact

The Product III device requires the base contact to be made from the top, due to the non-conducting ceramic substrate. Two methods have been developed for making the top base contact: an aluminum alloy step to punch through the emitter to the base contact, and an etch step to remove the emitter and expose the base. Each approach was evaluated for its ability to make ohmic contact to the base, and its compatibility with the re-interconnection step.

Aluminum-based contacts, either screen-printed or evaporated, are suitable for making contact to the base by punching through the emitter. A significant amount of silicon will go into solution with aluminum at 800 to 900 °C, which allows the alloy to extend well into the base region. Good ohmic contact to the base region was achieved using this technique, however there were several technical problems associated with this approach. The punch-through contact also shunted the junction, since it also contacted the emitter region. This required an extra dicing step to isolate the emitter from the base contact. Also, the evaporated contacts suffered from severe oxidation during the alloy step, in spite of efforts to control the oxygen in the ambient during the firing sequence. This prevented low resistance contacting during the re-interconnection step. Both screen-printed and evaporated aluminum contacts shunted the emitter. This could be addressed by using an additional dicing step. Screen printing, however, left small dots of aluminum paste on the active region of the emitter that could not be isolated. For this reason, nearly all devices made with screen printed aluminum contacts suffered from severe shunting.

An alternative to punching through the emitter to make contact is to remove the emitter before applying the contact metal. The contact area was defined by photolithography and the emitter layer was removed by plasma etching. Titanium-palladium-silver contacts can be used for both emitter and base contacts in this case, and can be applied with a single evaporation. After sintering the contacts at about 450 °C, the Ti/Pd/Ag contacts can be plated with silver to increase thickness and reduce series

resistance of the contacts. The plated Ti/Pd/Ag contacts have been the most successful contact to date. Excellent ohmic contact to both the emitter and base regions has achieved, the contacts are compatible with each of the re-interconnection techniques evaluated.

Electroless nickel plating has also been evaluated as a metal contact system. Electroless nickel required a separate plating step for the base and emitter contacts, since the sintering conditions were not compatible. Additionally, the nickel plated contacts were not uniform in coverage of the contact area. This led to poor electrical characteristics of the contact.

4.2.3 Cell Isolation

Cell isolation was achieved by dicing through the silicon layer to the ceramic substrate. Silicon layers as thick as 25 mils were isolated by dicing. The width of the diced isolation trench was typically 4 mils, although this width can be reduced by using narrower dicing wheels. Typically, dicing introduced significant saw damage which decreased the performance by reducing the shunt resistance. The damage was removed by etching in a plasma etch chamber for 5-7 minutes. The surface of the device was protected during this process step by photoresist, which was applied before dicing.

Some processes required an additional dicing step to isolate the base contact from the emitter. This step was generally undesirable, since it reduced the active area of each cell. When it was necessary, the saw damage from this step was removed by using the damage etch process described above.

4.2.4 Re-interconnection

The re-interconnection step has remained the least well-developed step of the Product III process. The major difficulty is due to the deep isolation trench. The trench eliminates evaporated contacts as a possible method of re-interconnection, since these contacts cannot conform to a step of this height (as high as 10 mils). Therefore, three alternative techniques were investigated: polyimide planarization, solder paste or solder dipping, and conductive epoxy.

A polyimide coating loaded with silicon powder (to reduce shrinkage during curing) was used to planarize the diced isolation trench so that evaporated contacts could be used. A photomicrograph of a refilled trench is shown in Figure 9. The polyimide was loaded with silicon powder to the consistency of toothpaste, then squeegeed into the trenches with a soft rubber squeegee. The filler was cured at 120 ^{o}C for 30 minutes, and any polyimide remaining on the surface was removed with a swab in photoresist developer. Unfortunately, the resulting surface was not consistently planar enough for the evaporated metal, which resulted in a high series resistance in the interconnections. This difficulty could be solved by applying the filler and planarizing in a repeatable production mode.

Figure 9. Photomicrograph of a polyimide filled isolation trench (magnification= 100X).

The second approach used solder to bridge over the diced isolation trench. The solder was applied both in paste form and by dipping in a pot of molten solder. The solder dipping technique was difficult to control and left a film of oxidant on the surface of the sample. This problem could be solved by more careful control of the ambient gases. The solder paste was more successful. It was applied with a syringe over the isolation trench and reflowed by placing the sample on a hot plate. The major difficulties with both solder-based re-interconnection techniques were wetting to the evaporated contact metal, and bridging the isolation trench. When wetting was not obtained, the surface tension of the solder caused it to ball up rather than form a continuous bridge connection. Wetting was easily obtained with screen printed contacts. A successful solder bridge is illustrated in Figure 10.

The third approach used conductive epoxy to re-interconnect the cells. Small drops of epoxy were placed across the isolation trenches. This technique has been the most successful, however, its use on laboratory scale devices is highly labor intensive.

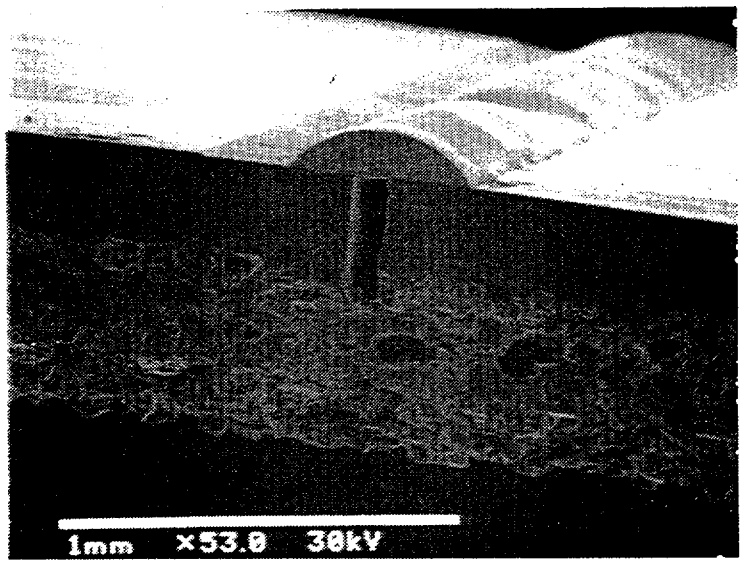


Figure 10. Photomicrograph of a solder bridge.

4.3 Device Results

Monolithically interconnected arrays were formed following the procedures described above. Laboratory scale devices (16 to 25 cm^2) were used in this process-development effort. The I-V curve of one of the best devices is shown in Figure 11. The device was fabricated without antireflection coating. No passivation or gettering techniques were used. The overall array characteristics were: Voc = 3.7 V, Isc = 19.4 mA, and FF= 0.51 for the 20.35 cm^2 device. As the curve indicates, the low fill factor was caused by high series resistance (metallization difficulties). The current was low due to a lack of anti-reflection coating, low minority carrier diffusion length and a heavily doped emitter. This device was fabricated to demonstrate the feasibility of device isolation and interconnection on a ceramic substrate. Efforts will now be focused on improving device performance.

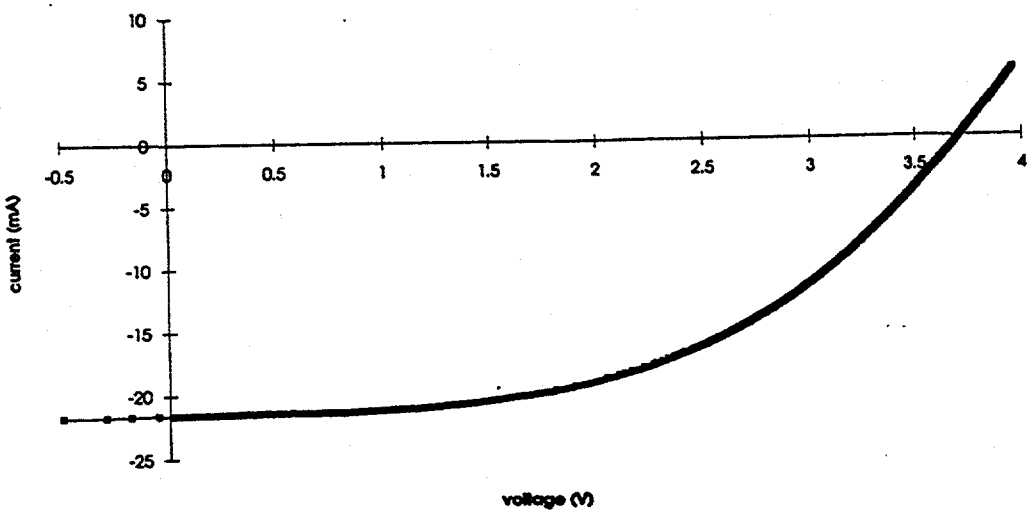


Figure 11. I-V curve of a 9 element monolithically interconnected array.

5. Conclusions

Significant improvements have been made in the material quality of Silicon-Film layers on ceramic substrates. Thin, large-grain polysilicon layers can be grown routinely on ceramic substrates. Minority carrier diffusion lengths, however, had been limited to less than 10 μm. Recent success identifying and controlling contamination sources has lead to lifetime improvements and the development of a successful gettering process. Prototype arrays have been fabricated that demonstrate the successful interconnection of 9 cells on a ceramic substrate. Optimizations in device processing are expected to generate monolithic arrays with efficiencies over 8% in the short term.

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16. Abstract (Limit: 200 words)
This report describes work to develop Silicon-Film™ Product III into a low-cost, stable solar cell for large-scale terrestrial power applications. The Product III structure is a thin (<100-μm) polycrystalline layer of silicon on a durable, insulating, ceramic substrate. The insulating substrate allows the silicon layer to be isolated and metallized to form a monolithically interconnected array of solar cells. High efficiency is achievable with the use of light trapping and a passivated back surface. The long-term goal for the product is a 1200-cm^2, 18%-efficient, monolithic array. The short-term objectives are to improve material quality and to fabricate 100 cm^2 monolithically interconnected solar cell arrays. Low minority-carrier diffusion length in the silicon film and series resistance in the interconnected device structure are presently limiting device performance. Material quality is continually improving through reduced impurity contamination. Metallization schemes, such as a solder-dipped interconnection process, have been developed that will allow low-cost production processing and minimize R_s effects. Test data for a nine-cell device (16 cm^2) indicated a V_{oc} of 3.72 V. These first-reported monolithically interconnected multicrystalline silicon-on-ceramic devices show low shunt conductance (<0.1 mA/cm^2) due to limited conduction through the ceramic and no process-related metallization shunts.

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