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PREFACE

This document contains preprints of papers prepared by photovoltaics researchers at the National Renewable Energy Laboratory (NREL) and collaborating researchers for the 23rd IEEE Photovoltaic Specialists Conference. The conference was held May 9-14, 1993, in Louisville, Kentucky. The NREL work described here was funded by the U.S. Department of Energy under Contract No. DE-AC02-83CH10093.

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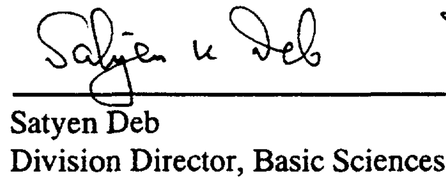

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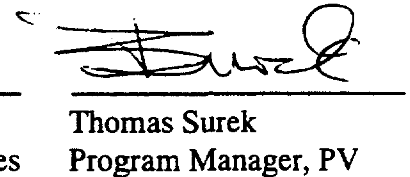

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EFFECTS OF PROCESSING ON THE PROPERTIES OF POLYCRYSTALLINE CDTE GROWN BY VARIOUS DEPOSITION TECHNIQUES

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ABSTRACT

Enhanced performance of CdS/CdTe polycrystalline heterojunction cells has been observed following post-deposition chemical and temperature processing. However, correlation of the effects of the $CdCl_2$ and 300°-500°C treatments with the resulting film properties seems to vary with the origin of the material. This paper examines and compares the effects of these treatments on the physical, structural, chemical, compositional, and electro-optical properties of polycrystalline CdTe films produced by sputtering, close-spaced sublimation, physical vapor deposition and metallo-organic chemical vapor deposition. The chemical and heat treatments are shown to decrease Cd-vacancy levels (PL measurements) and quench deep electronic levels (DLTS). These defect level determinations are correlated with increases in the minority-carrier lifetimes. Differences in grain growth and densification are reported for various deposition techniques. The possibility of grain boundary passivation associated with Cl and oxygen diffusion at that defect is reported. Atomic-force microscopy (AFM) is used to investigate nanostructural differences among the films, especially the presence of small grains (not observable by Scanning Electron Microscopy [SEM]) in the vicinity of grain boundaries. The change in structure in these intergrain regions and annihilation of these <300-Å grains following processing are observed and correlated with the passivation and change of electronic defect levels.

INTRODUCTION

To date, CdTe/CdS polycrystalline thin-film heterojunction demonstrated solar cell efficiencies in excess of 15% and module efficiencies in the 9%-11% [1-3] range. Among the methods successfully used to prepare the p-type CdTe thin films involved in these junctions are electro-deposition, physical vapor deposition, and close-spaced sublimation. Enhanced performance of CdS/CdTe polycrystalline heterojunction cells has been observed following post-deposition chemical and temperature processing [4,5]. However, correlation of the effects of the $CdCl_2$ and 300°-500°C treatments with the resulting film properties seems to vary with the method of depositing the CdTe films as well as the specifics of the post-deposition heat treatments. The latter determine various materials parameters that influence the device performance. These include the type and concentration of the dominant defects, interface states, and deep trap levels. This paper examines and compares the effects of these treatments on the physical, structural, chemical, compositional, and electro-optical properties of polycrystalline CdTe films produced by rf sputtering (RFS), close-space sublimation (CSS), physical vapor deposition (PVD) and metallo-organic chemical vapor deposition (MOCVD). Atomic-force microscopy (AFM) is also used to investigate nanostructural differences among the films, especially the presence of small grains (not observable by SEM) in the vicinity of grain boundaries.

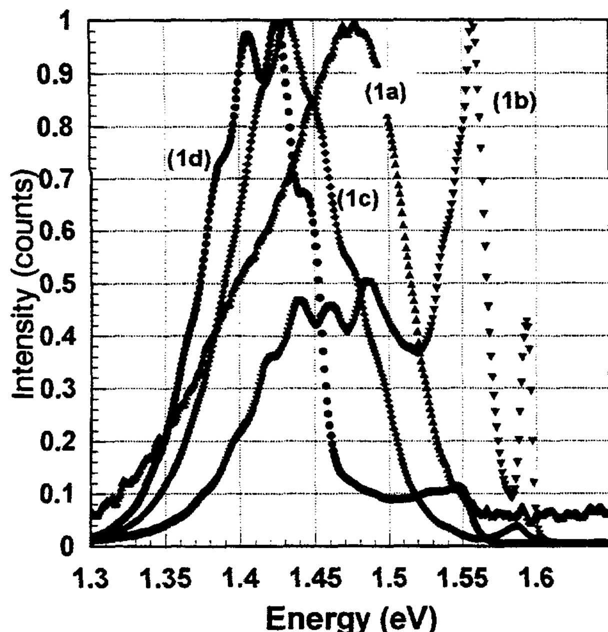
EXPERIMENTAL METHODS

Samples of polycrystalline CdTe thin films prepared by CSS, PVD, MOCVD, and RFS methods were investigated in this study. Heat treatments were carried out by depositing a thin layer of CdCl from CdCl-saturated solution in methanol, on the CdTe film; the structures were then heat treated for 20-30 minutes at 350°-450°C in a tube furnace. In some cases, oxygen or nitrogen was flowing during the heat treatment. The chemical compositions of the CdTe films were measured using wavelength-dispersive X-ray spectrometry with a CAMECA electron microprobe and Physical Electronics Model 600 scanning Auger microprobe. High-resolution photoluminescence (PL) emission spectra were obtained at different temperatures (5-300 K) using the 6471-Å Ar laser line at different excitation powers (2-10 mW unfocused). The PL measurements were also taken before and after the CdTe films were annealed in Cd and Te atmospheres. Deep-level transient spectroscopy (DLTS) also has been used to determine both the trap levels and densities dominating each material. TEM and X-ray measurements were used to study the crystallinity, grain size, and morphology of the film material. AFM is used to image the surface structure of each CdTe film.

RESULTS

CdTe Electro-optical Properties

The PL emission from as-deposited samples of CdTe films, of very close composition, prepared using PVD, CSS, MOCVD, and RFS methods are shown in Figs. 1a, 1b, 1c, and 1d. The respective emission after heating in air at 400°C for 30 minutes is shown inFigs. 2a, 2b, 2c, and 2d. It is clear that the PL emission and consequently the defect configuration is completely different for each sample. In addition the effect of heat treatment varies from sample to sample. The broad emission from the PVD sample is dominated by a transition at 1.47 eV before heating and at 1.4 eV after the heat treatment. The CSS sample , on the other hand, has demonstrated a well-resolved emission before and after annealing. However, the dominating luminescence has changed its location from 1.55 eV to 1.41 eV after receiving the heat treatment. The



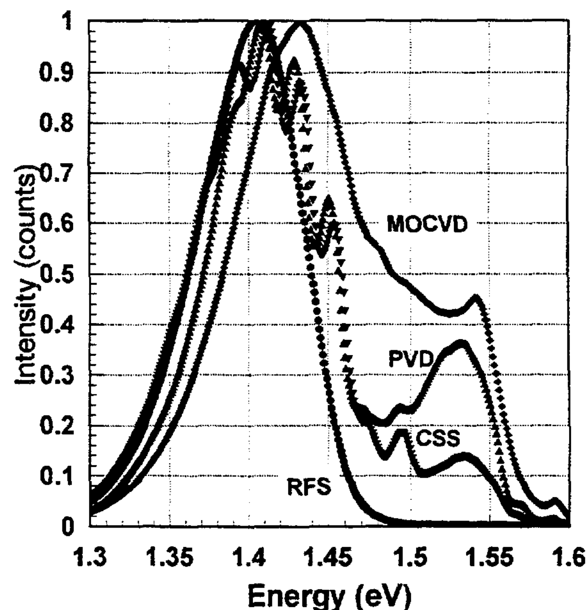


Fig. 1. PL emission from thin films of CdTe deposited by PVD (1a), CSS (1b), MOCVD (1c), and RFS (1d) before receiving the CdCl treatment.

Fig. 2. PL emission from the same CdTe films of Fig.1 after receiving the CdCl treatment at 400°C for 30 minutes.

MOCVD sample has also emitted a broad spectrum with almost identical features and the same dominating transition at 1.425 eV before and after the treatment. The main difference observed is the increase in intensity of the peak at 1.54 eV after annealing. It is noteworthy that the emission from the RFS film is almost identical to that obtained from the MOCVD film except some differences in the relative intensity. The luminescence at 1.55 eV is caused by bound exciton recombination [6]. A donor level (D) at 50 meV [7] below the conduction band (CB) is involved. This donor level is probably related to Cd atoms substituting for Te. This peak decreases in intensity after annealing at temperatures above 425°C, where Te is depleted from the CdTe surface. From the change in intensity and peak position of the 1.47- and 1.425-eV emission with measuring temperature and excitation power, it is deduced that both are band-defect recombinations. The 1.47-eV luminescence is attributed to CB-acceptor (A1) recombination involving the antisite CdTe acceptor defect or CdTe/donor complex defects, and the 1.425-eV luminescence is a Cd_i D-valence band (VB) transition. The low energy emission at 1.410 eV and 1.400 eV exhibited a red shift by lowering the PL measurement temperature; therefore, they are attributed to D-A transition. Using D1 as a common donor level involved in these two D-A recombinations, then they would end at two acceptor levels A2 at ~140 meV and A3 at ~150 meV above VB. The 1.47- and 1.41-eV peak has been found to dominates the spectrum of Te-rich films, and its intensity increases with annealing in the presence of Te [8]. This result suggests that the concentration of both defects D1 and A2 are increased. It is therefore deduced that D1 is attributed to the CdTe defect and A2 is attributed to Te_i. On the other hand, annealing CdTe in the presence of Cd reduces the intensity of the 1.40- eV emission [8] because of the reduction of the concentration of both D1 and A3, identified as VCd [9]. It is also noted that the emission at 1.47 eV dominates this spectrum. The reduction of the luminescence intensity of the D-A recombination as a result of the CdCl/ high-temperature heating explains the loss of hole density [10,11], and then the V_{Cd} and Te_i acceptors are formed. The defect configuration and, consequently, the degree of compensation is determined by the process residual impurities. These are crucial parameters to the CdS/CdTe junction characteristics.

The results from minority-carrier lifetime (MCL) are also correlated with the other measurements. An increase of 25%-50% in the value of MCL was observed after the CdCl treatment of the PVD film (original MCL was ≥ nsec) at temperatures ≥355°C. The MOCVD and RFS films that have very low MCL (≤ 0.2 nsec) before the CdCl treatment demonstrated a substantial increase (up to 10 times in the RFS film) after receiving the treatment. On the other hand, the MCL of the CSS film did not respond so well to the CdCl treatment, which indicates that this treatment is not effective enough to passivate the non-radiative high speed defect states dominating this particular sample.

DLTS measurements have confirmed that a major electron trap at about 1.2 meV below the CB dominates most of the CdTe heterojunction devices (the exact location depends on the origin of the CdTe film). Several trap levels (deeper and higher in density than that in the heterojunction) were detected in Schottky barrier devices, fabricated on CdTe film without heating at high temperature. This explains the enhancement of the V_{oc} of the heterojunction devices after annealing at 400°C or higher.

Structural Properties

All untreated CdTe samples have shown a strong (111) orientation, though some small misorientation toward *(511)* was observed in the X-ray diffraction data. On the other hand, the heat-

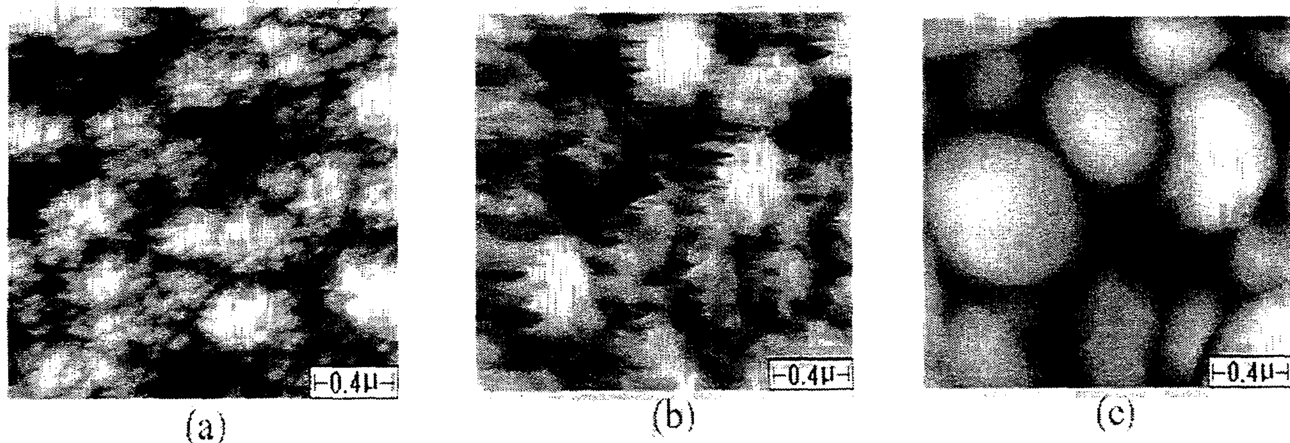


Fig. 3. AFM pictures of RFS CdTe film before (a) and after receiving the CdCl heat treatment at 300°C (b), and 400°C (c).

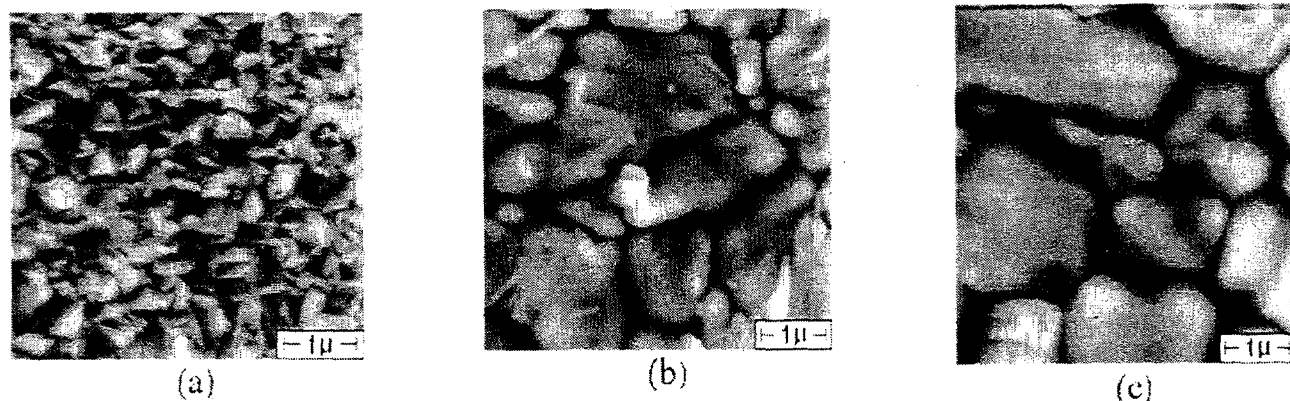


Fig. 4 . AFM pictures of PVD CdTe film before (a) and after receiving two different CdCl heat treatments (b and c).

treated CdTe film demonstrated strong preferred (111) orientation. Plan-view investigation using transmission electron microscopy (TEM) revealed the grain size and individual crystallographic orientation of the grains. In general, these polycrystalline films are composed of a close-packed array of single crystal grains of dimension 0.25-2.0 μm. It has been observed that the individual CdTe crystallites grow with a preferred crystallographic orientation. Most often the [100], [110], and [111] CdTe axes are aligned perpendicularly to the substrate surface. Atomic resolution images have shown that the predominant type of structural defect is coherent microtwin boundaries. Both the real space electron images and selected area diffraction patterns of single grains indicate that the twinning occurs perpendicularly to the {111}-zincblende directions. In some cases (films deposited by CSS and PVD), TEM studies showed that the CdTe films exhibited intergrowths of the cubic zincblende phase with the hexagonal wurtzite (hexagonal zinc sulfide structure) variant of CdTe. The wurtzite variant always occurred as the minority phase. The individual hexagonal domains were small, on the order of 10 to 100 atomic layers. This highly twinned growth habit and zincblende/wurtzite intergrowth structure were not observed in polycrystalline CdTe thin films deposited by rf sputtering. It is noteworthy that both types of deposited films showed significantly improved micro structure, lattice constant, and grain size after high temperature (350°-450°C).

AFM investigation of the nanostructure differences after post deposition CdCl treatments, of films prepared by different growth techniques, have confirmed the presence of structural changes in the inter-grain regions and annihilation of less than 300-Å grains in the RFS film after processing. Figure 3 shows AFM images from RFS thin films before and after the treatment. Image 3a shows the nanograins which cannot be seen with the SEM within the larger grains; images 3b and 3c show the grain growth resulting from the CdCl treatment as a function of temperatures. Figures 4a, 4b, and 4c also show the grain growth of the PVD film after receiving to different CdCl treatments. It is clear that the increase in the size of the grains is determined by the temperature at which the sample was heated. The change in the grain size of the CSS and MOCVD films, that have originally large grains as grown (≥ 1 mm), was not appreciable. However, well-defined grains were observed (Fig. 5c) in the MOCVD CdTe only after the 400°C CdCl treatment. This observation is correlated with restructuring, passivation, and, consequently, change of electronic defect levels of this material.

SUMMARY

The CdTe film in the CdTe/CdS structures undergoes physical and compositional changes, which result in a change in the

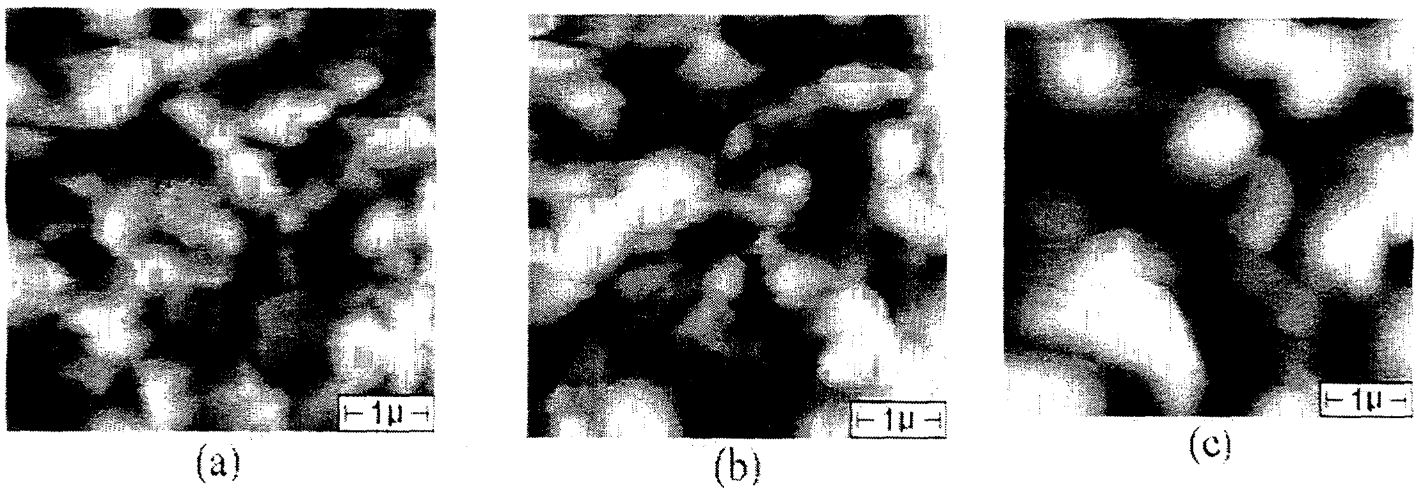


Fig. 5. AFM pictures of MOCVD CdTe film before (a) and after receiving two different CdCl heat treatments (b and c).

configuration of its defects (intrinsic, extrinsic, and structural) and consequently improvements in the cell performance, after receiving the appropriate chemical and heat treatments. However, the specifics of the treatment vary with the CdTe deposition method. Structural change in the intergrain regions and annihilation of nanograins following processing are observed (mainly in RFS material) and correlated with the passivation and change of electronic defect levels.

ACKNOWLEDGMENT

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RECOMBINATION LIFETIME AND PERFORMANCE OF III-V COMPOUND PHOTOVOLTAIC DEVICES

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ABSTRACT

High-efficiency photovoltaic (PV) devices are based both on the III-V compound and silicon semiconductor technologies. The III-V semiconductors are more efficient than silicon for concentrator technology when the incident flux exceeds about 200 suns. These devices are of both single- and multijunction configurations, the latter being primarily feasible by the epitaxial growth of combinations of binary and ternary compounds. Work has focused on semiconducting materials in the GaAs and $Al_xGa_{1-x}As$ series, although other III-Vs have recently been developed for PV applications. The role of the minority-carrier lifetime and mobility in high-efficiency devices is discussed. The state-of-the-art of current popular materials is reviewed.

INTRODUCTION

High-efficiency device research has focused on both material improvement and device design. Photovoltaic (PV) devices are minority-carrier devices, and optimizing minority-carrier properties is a crucial component of processing research. We will show here that, from among the various minority-carrier transport parameters, the minority- carrier lifetime is of greatest importance in determining PV performance and efficiency. Here we will review work from a number of laboratories. The analysis of time-resolved photoluminescence (TRPL), as a technique for determining minority-carrier lifetime, is discussed. Recent innovations and improvements in the technology will be emphasized.

A. Minority-Carrier Lifetime

The basic recombination mechanisms in semiconductors have been reviewed extensively in the literature [1,2,3]. These include radiative recombination, Shockley-Read-Hall (SRH) recombination, and Auger recombination. The recombination lifetime is controlled by all of these mechanisms in the wide range of PV materials.

The low-injection, radiative lifetime is given by

$$\tau_R = \frac{1}{BN} \qquad \text{(Eq. 1)}$$

Here, N is the majority-carrier concentration, and B is a coefficient that has been calculated from band theory [4, 5]. The calculations show that B is about 1-2 x 10^{-10} cm^3/s for GaAs.

Chemical and mechanical defects, such as dislocations, produce energy levels in the forbidden gap leading to SRH recombination. For a near-midgap levels inducted by a defect, the SRH lifetime is given by

$$\tau_{SRH} = \frac{1}{N_t \sigma v_{th}} \qquad \text{(Eq. 2)}$$

Here, N_t is the volume density of the defect, σ is the minority-carrier capture cross section, and v_{th} is the thermal velocity. Surface or interface recombination is treated as a 2-dimensional extension of SRH recombination. When a number of recombination mechanisms are present, the total lifetime is determined by adding reciprocal lifetimes. Several detailed reviews of recombination processes in the III-V compound semiconductors have been recently published [1,2,3].

B. Photon Recycling

For the direct bandgap materials, self-absorption and reradiation of photons have been found to be important. The photon recycling effect has potential applications for improved PV devices [6]. The self-absorption and re-emission of radiative recombination were proposed by Dumke [7] and by Moss [8] many years before significant experimental data were available. A number of researchers [9,10] suggested that self-excited luminescence or photon recycling is an important effect in GaAs. Early measurements using TRPL in $Al_xGa_{1-x}As$/GaAs DH devices showed that the lifetime increased with active-layer thickness [11]. Calculations [12,13,14,15,16] explained these data in terms of the photon recycling effect. Garbuzov and coworkers [15] presented experimental data and theory indicating that the recycling effect is greatly enhanced by substrate removal. All theories show that the effective lifetime can be written in terms of a photon recycling factor ϕ that multiplies the radiative lifetime, increasing the radiative lifetime by the factor ϕ. Measurements of the factor ϕ are discussed in detail in a later section.

$$\frac{1}{\tau_R} \rightarrow \frac{1}{\phi_{\tau R}} \qquad \text{(Eq. 3)}$$

C. Lifetime Diagnostics

The TRPL technique has become the standard for measuring recombination lifetimes in light-emitting materials. Here time-

correlated single-photon counting is the most popular and powerful configuration for measuring TRPL [1]. One can measure TRPL on many types of devices, including solar cells [17]. The most easily interpretable results are produced by diagnostic devices called isotype double heterostructures (DHs), where the corrections between the measured photoluminescence (PL) lifetime and the recombination lifetime are minimal. At low injection levels, the PL lifetime of a DH structure, with active layer thickness d, has been derived as

$$\frac{1}{\tau_{PL}} = \frac{BN}{\phi} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_A}\frac{2S}{d} \quad \text{(Eq. 4)}$$

Here, τ_A is the Auger lifetime and S is the surface/interface recombination velocity at the active layer/confinement layer interface. This formula is accurate only under the conditions that $Sd/D < 1$. For larger values of S, the surface term on the right must be modified [18]. Here τ_{PL} is really equivalent to the minority-carrier lifetime in the DH device.

In concentration cells, the injected carrier densities becomes large and Eq. 4 above may not apply. At high injection, a recombination lifetime is derived that is usually a function of the injected carrier density. Designating the injected carrier density as ρ and the doping density as N, the high-injection rate equation is written as [18];

$$\frac{d\rho}{dt} = -\left(\frac{B}{\phi(d)} + \sum_{i=1}^{k}\frac{1}{\tau^{i}_{min}(N+\rho) + \tau^{i}_{maj}}\right)(\rho N + \rho^2) \quad \text{(Eq. 5)}$$

Here, the sum is over the types of SRH centers, including those at the interface, contributing to the interface recombination velocity. The radiative recombination rate at high injection is reduced by photon recycling, and will be discussed in detail elsewhere [19]. The solutions of Eq. 5 when SRH recombination dominates have been discussed in the literature [20]. In the case of very high injection, the effective lifetime becomes:

$$\frac{1}{\tau_{eff}} = \frac{B(N+\rho)}{\phi} + \frac{1}{\tau_{min} + \tau_{maj}} \quad \text{(Eq. 6)}$$

In SRH-dominated materials, the second term on the right dominates τ_{eff} and the recombination lifetime increases accordingly. This effect produces an increase in efficiency in concentrator cells.

D. Electron and Hole Mobility

The mobility for both electrons and holes is controlled by scattering mechanisms arising from several sources. The intrinsic mobility is determined by scattering by lattice vibrations or phonons and is designated μ_L. Scattering also occurs because of neutral and ionized defects, the latter being much stronger scattering centers because of the long range Coulomb force. Dislocations, grain boundaries, and other mechanical defects also contribute to the mobility by scattering electrons and holes. Here, we will designate the contribution of each defect type to the mobility as μ_i. The total mobility is obtained by adding the reciprocal mobilities of each scattering mechanism.

$$\mu = \left(\frac{1}{\mu_L} + \sum_i \frac{1}{\mu_i}\right)^{-1} \quad \text{(Eq. 7)}$$

The solution of device equations for PV devices indicate that open-circuit voltage and short-circuit current depend strongly on the minority-carrier diffusion length in different regions of the device. The minority-carrier diffusion length (L), lifetime (τ), and diffusivity (D) are related by the well known relationship

$$L^2 = D_\tau \quad \text{(Eq. 8)}$$

For nondegenerate semiconductors, the minority-carrier diffusivity is related to the minority-carrier mobility through the Einstein relationship

$$D = \frac{KT}{q}\mu \quad \text{(Eq. 9)}$$

Therefore, PV device performance is dependent upon both the minority-carrier lifetime and mobility. We will show here that the minority-carrier lifetime is the most materials-sensitive and widely varying parameter. On the other hand, we will show that the minority-carrier mobility is fairly structure-insensitive. Therefore, the minority- carrier lifetime generally controls the minority-carrier diffusion length. One could summarize PV materials research as a search for growth technologies that produce adequate lifetimes at the lowest possible cost. Here we will undertake a detailed analysis of GaAs PV devices in terms of the known minority-carrier properties of the material.

MINORITY-CARRIER PROPERTIES OF GaAs

A. Electron and Hole Mobility in GaAs

The strength of phonon scattering in silicon and compound semiconductors is such that the mobility is relatively insensitive to mechanical and chemical defects. Curve A of Figure 1 shows the theoretical electron mobility in n-type GaAs from the textbook by Sze [21]. The mobility is dominated by phonon scattering for donor densities less than about 1×10^{18} cm^{-3} in uncompensated material. At higher donor densities, ionized impurity scattering becomes dominant and reduces the mobility as $1/N_D$. The mobility is seen to vary by about a factor of 8 as the donor density varies from 1×10^{14} cm^{-3} to 1×10^{18} cm^{-3}. The square data points are measurements of electron mobility in n-type GaAs grown by molecular beam epitaxy (MBE) on a GaAs substrate [22]. Most of data points (■) fall about Curve A. The data points (▲) are measurements of the electron mobility grown by MBE on a silicon substrate [23]. These MBE layers are between 2.4-μm and 4.0-μm thick, and are grown directly on the silicon substrate. Because of a large lattice mismatch between GaAs and silicon (about 4.1%), these thin GaAs films usually contain mismatch-generated dislocations with densities between 1×10^7 to $1 \times 10^9/cm^2$. In GaAs films grown on GaAs substrates, the dislocation densities are usually less than 1×10^4 cm^{-2}. One sees from the data that the electron mobility is only slightly lower because of dislocation scattering. This observation has allowed the development of many majority-carrier devices using GaAs grown on silicon substrates [24]. In summary, these data show that the electron mobility varies less than 1 order of magnitude even when ionized impurity densities vary five orders of magnitude. The electron mobility is very slightly reduced by dislocation densities exceeding 10^7 cm^{-2}.

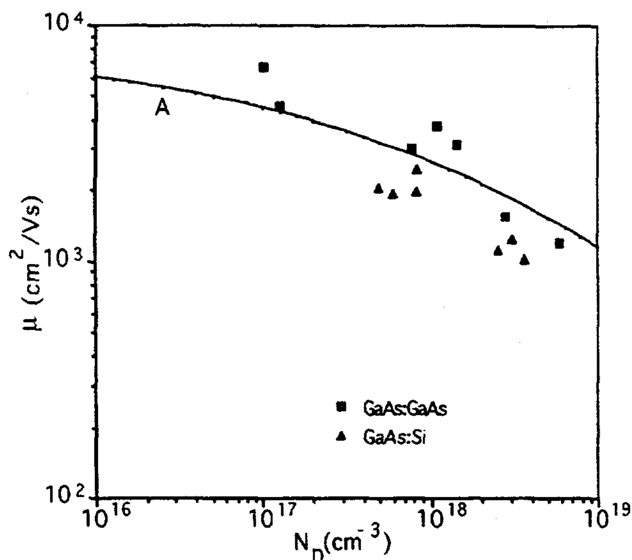

Figure 1: Electron mobility in n-type GaAs.

Figure 2 shows experimental Hall data, giving the majority-carrier hole mobility for p-type GaAs [25]. The Hall mobility drops about a factor of three over as the ionized acceptor density increases from 1 x 10^{16} cm^{-3} to 1 x 10^{19} cm^{-3}. The data points (●) are measurements of the minority-carrier hole mobility in n-type GaAs by Lovejoy and coworkers [26]. Lovejoy used the zero-field time-of-flight (ZFTOF) technique to measure the hole mobility in n-GaAs over a range of ionized donor densities from about 1 x 10^{17} cm^{-3} to 2 x 10^{18} cm^{-3}. The hole mobility is approximately constant (280 cm^2/s) over this doping range in accordance with the calculations of Lowney and Bennett [27]. However the theory produced lower absolute values, about 100 cm^2/Vs, for this doping range. Finally, the square data (■) is a measurement of the hole mobility in n-GaAs by Slater and coworkers [28]. This datum is consistent with the ZFTOF data of Lovejoy and coworkers. An important point here is that minority-carrier mobility (and diffusivity) appear to be less sensitive to ionized impurity scattering than the majority-carrier mobility. This finding has positive implications for PV devices as performance increases with doping levels provided that minority-carrier diffusion length is not degraded.

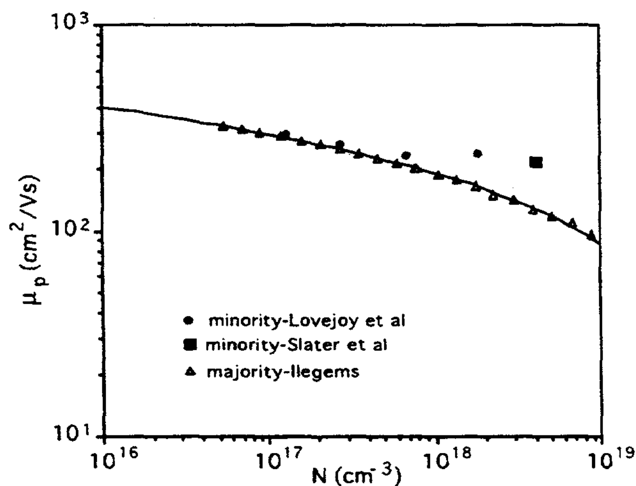

Figure 2: Hole mobility in n- and p-type GaAs

B. Minority-Carrier Lifetime in GaAs

Early measurements on bulk GaAs wafers [29] indicated that the room temperatue lifetimes were in the range of 10 to 20 ns at doping levels below about 1 x 10^{17} cm^{-3}. At higher doping levels, the lifetimes decrease approximately as 1/N where N is the donor or acceptor concentration. Figure 3 shows Hwang's early measurements of minority-carrier lifetime in GaAs wafers over a range of doping densities. The radiative or theoretical lifetime is shown by a solid line. These measurements were made on unpassivated wafers, and the surface recombination loss accounted for the data analysis. As noted above, the lifetimes are independent of doping from about 1 x 10^{16} cm^{-3} to 1 x 10^{18} cm^{-3}. A recent measurement on AlGaAs passivated wafers by Ehrhardt and coworkers [30] is also shown in the figure. The wafer doping is 1 x 10^{18} cm^{-3}, and the measured lifetime is 6 ns. With no AlGaAs passivating layer, the measured lifetime on the same wafer was 0.16 ns, showing the dominanting effect of free surface recombination in GaAs. The Ehrhardt data on the passivated wafer is comparable to the earlier measurment of Hwang. At the lower doping levels, the lifetimes are also much smaller than the radiative lifetime, and are determined by deep level defects in the wafers; i.e., by Shockley-Read-Hall recombination.

In 1976, Nelson and Sobers measured the minority-carrier lifetime in epitaxial, p-type GaAs-isotypeDHs and found quite different results [31,32]. Here, the surface recombination rate is reduced by epitaxial AlGaAs. Their data (●) are shown in Figure 4 and indicate lifetimes that are comparable to the intrinsic radiative recombination rate (τ_R). Here τ_R is given by the solid line, and

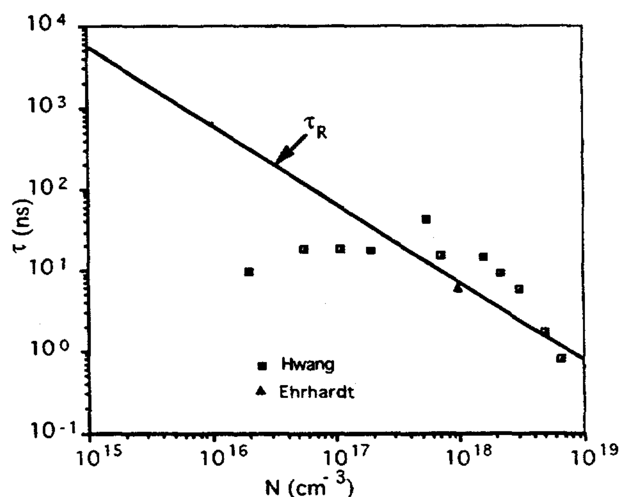

Figure 3: Hole lifetime in n-type GaAs wafers. The solid line is the calculated radiative lifetime.

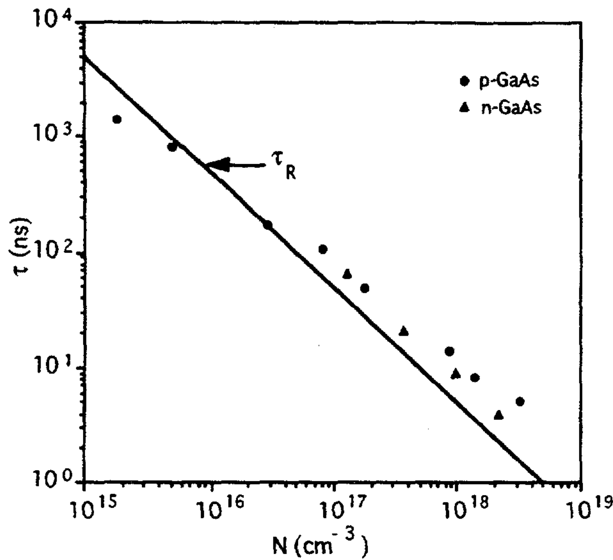

Figure 4: Minority-carrier lifetime in p- and n-type epitaxial GaAs.

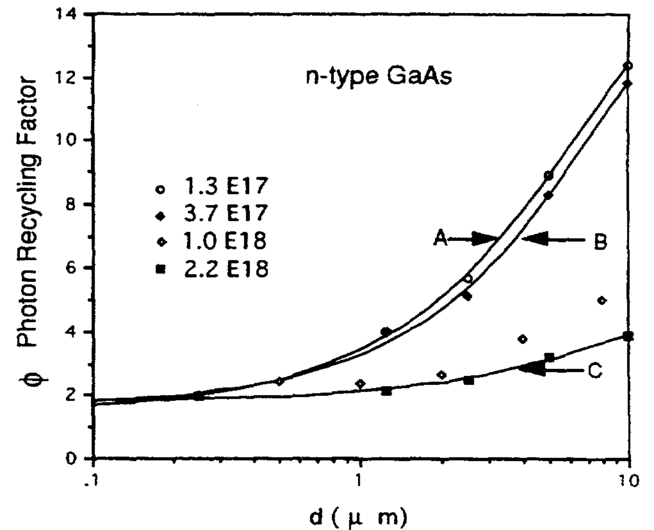

Figure 5: Measured and calculated photon recycling factor in n-type GaAs versus active layer thickness.

was calculated assuming that B= 2 x 10^{-10} cm^3/s. Moreover, one sees that the PL lifetime was larger than the radiative lifetime over a range of doping levels from about 1 x 10^{17} cm^{-3} to 1 x 10^{19} cm^{-3} because of photon recycling. The active-layer thickness of these devices varied from several μm to about 15 μm.

Also shown in the figure is recent TRPL data (▲) on metal-organic chemical vapor deposition (MOCVD)-grown n-type GaAs obtained by Lush and coworkers [33]. These data were measured on thin (1.0-μm or less) DH structures for which the photon recycling effects are minimal. Data on thicker structures will be shown in the next section. In summary, these data show that the GaAs bulk lifetime in epitaxial material is primarily controlled by the intrinsic, radiative recombination. By contrast, the lifetime in wafer material is controlled by bulk SRH recombination except at very high carrier concentrations.

C. Photon Recycling Effects Measured in GaAs

Recent TRPL measurements [34] on n-type DH structures provided by Lush were analyzed using the photon recycling effect. Figure 5 shows the calculated photon recycling factor in these devices using the experimental TRPL data and B = 2 x 10^{-10} cm^3/s. Curves A, B, and C are the values of ϕ calculated by Asbeck [12] for DH structures at similar doping concentrations. The factor ϕ is about 12 for a 10 μm DH structure when the doping level is below 1 x 10^{18} cm^{-3}. The decrease in ϕ at the higher doping levels is caused by the perturbation of the "sharp" absorption edge cause by ionized donors. This decreases the overlap of the internal emission spectrum with the absorption spectrum.

A remarkable enhancement of the photon recycling effect was recently reported [35] Lush and coworkers. A hole was etched through the substrate of the DH. TRPL measurements were made in etched regions and in the unetched regions. The PL lifetime for the d = 5.0-μm device (substrate etched) is 1.07 μs and is 28 times the radiative lifetime. This result verifies calculations that photon recycling is greatly enhanced by substrate removal [15]. The PL lifetime varies from about 500 ns for thin DHs to over 1 μs for thicker DHs. These data suggest that very long lifetimes are feasible in more heavily doped, free-standing thin-film devices because of the photon recycling effect. These effects have potential use for high-efficiency PV devices [6] as will be shown later in this paper.

D. GaAs Grown Heteroepitaxially on Siilicon

In recent years, there have been many reports of GaAs PV devices grown on silicon substrates. The cost advantage of using a silicon substrate rather than a GaAs substrate is a prime motivating factor. As is obvious from the previous section, majority-carrier devices have been very successful.

The minority-carrier lifetime is greatly degraded by dislocation recombination in the GaAs:Si system. For PV applications, a number of strain reduction schemes have been published [36]. These include GaAs buffer layers that are subjected to various thermal treatments for strain reduction in the active layer. Measurements by Ahrenkiel and coworkers [37], combined with a recombination theory developed by Yamaguchi and coworkers [38] at Nippon Telephone and Telegraph (NTT), find the lifetime in GaAs as a function of dislocation density. The dislocation contribution to the lifetime is given by

$$\frac{1}{\tau_d} = \frac{\pi^3 D N_d}{4} \qquad \text{(Eq. 10)}$$

Here N_d is the dislocation density in lines/cm^2, D is the minority-carrier diffusivity, and τ_d is the lifetime produced by the dislocations. The total lifetime is given by the addition of reciprocal lifetimes assuming only radiative and dislocation recombination mechanisms.

$$\frac{1}{\tau} = BN + \frac{\pi^3 DN_d}{4} \qquad \text{(Eq. 11)}$$

Figure 6 plots the theoretical lifetime according to Eq. 11 over a range of dislcoation densities and doping concentrations. The parameters are appropriate to n-type GaAs with D chosen to be 7 cm^2/s (from Fig. 3). (However, photon recycling is not included in this model.) The calculated lifetime varies over about 5 orders of magnitude for a range of dislocation densities found in epitaxial GaAs:GaAs and GaAs:Si. Theory indicates the extreme sensitivity of the lifetime to dislocation recombination. To obtain the largest open-circuit voltages and fill factors, one requires that the base doping level be greater than about 1×10^{17} cm^{-3}. As will be shown later, the minority-carrier lifetime needs to be larger than about 1 or 2 ns for useful efficiencies. Thus, in GaAs:Si PV devices, minority-carrier lifetime is the limiting factor for device performance.

Figure 6 shows data measured by the TRPL technique on n-type (2×10^{17} cm^{-3}) GaAs:Si DH devices grown at Spire Corporation. The dislocation density was measured at NREL by M. M. Al-Jassim and coworkers on the same samples. The solid line is a fit of the NTT model to the experiment data using a value of minority-carrier diffusivity D of 2 cm^2/s. In addition, a photon recycling factor, $\phi = 8.84$, was needed to fit the GaAs on GaAs device. One sees that the NTT model fits the data, except that a somewhat low value of D must be used. However, that can be explained by the fairly simplistic model used to determine the capture cross-section of dislocations. These data, when combined with device modeling calculations in the next section, will give us an estimate of the current expected PV efficiency and the goals of dislocation reduction chemistry.

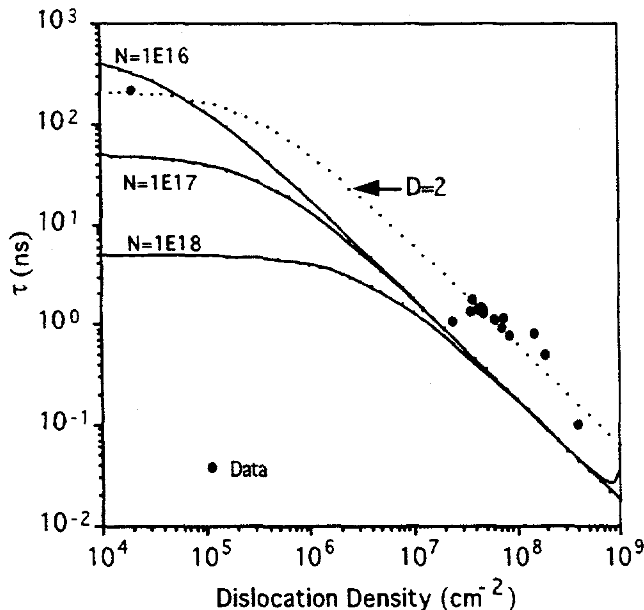

Figure 6: Hole lifetime in n-type GaAs versus dislocation density using the NTT model. Measured lifetimes in GaAs:Si DH devices.

In summary, the doping density and dislocation density of GaAs films were varied over many orders of magnitude. These data show that the minority-carrier lifetime typically varies 4 or 5 orders of magnitude in GaAs in response to these changes. By contrast, the mobility varies very little over the same range of doping or dislocation densities. These data disagree with a recent theory that variations in minority-carrier mobility rather than lifetime are the primary contributer to PV performance [39].

E. S of the $Al_xGa_{1-x}As$/GaAs Interface

The measurement of interface recombination velocities in $Al_xGa_{1-x}As$/GaAs DHs was first shown by Nelson [40] using the TRPL technique. These data are shown in Fig. 7 and show that $1/\tau_{PL}$ is nearly linear in 1/d. Variations occur in thicknesses greater than 1 or 2 µm and are caused by the photon recycling effect. By measuring the slope of $1/\tau_{PL}$ versus 2/d, S can be calculated. Figure 7 shows TRPL measurements on 15 $Al_xGa_{1-x}As$/GaAs DH devices with doping of about 1×10^{17} cm^{-3} and a range of active layer thicknesses. Most devices were fabricated with active layer thickness $d < 1$ µm so that S dominates the lifetime. The figure shows a least-squares fit to the data over the range $2/d > 0.25 \times 10^5$ cm^{-1} that gives S ~ 500 cm/s.

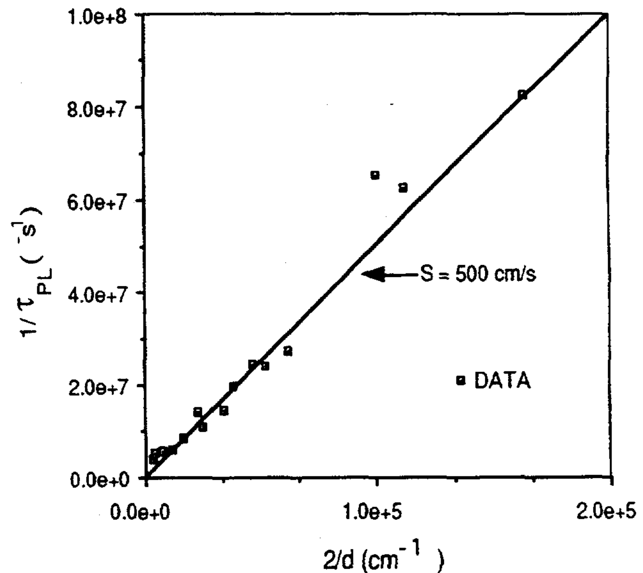

Figure 7: Calculation of interface recombination velocity using TRPL data from a thickness series of DH devices (Ref. 40).

This work [37] first noted that S increases with the GaAs doping level, and finds S is about 350 cm/s at 3×10^{16} cm^{-3} compared to 550 cm/s at 2×10^{17} cm^{-3}. Much larger values of S are frequently found for similiar devices that have been submitted to NREL for measurement.

F. Dependence of S on Growth Temperature

Recent studies [41,42] found that the recombination velocity at the MOCVD n-$Al_{0.30}Ga_{0.80}As$/GaAs interface changed by orders of magnitude, depending on growth temperature. Diagnostic DH devices were made in paralled with PV devices hoping to improve the PV efficiency by optimizing the growth temperature.

Here, one is improving the $Al_{0.30}Ga_{0.80}As/GaAs$ interface that is used as a back-surface minority-carrier reflector for the base (n-type, 2 x 10^{17} cm^{-3}). The diagnostic DHs were also made in a series of thicknesses at each growth temperature. The data analysis included the photon recycling factor, ϕ, that was specifically calculated [43] for the structure. Figure 8 shows the variation of the recombination velocity S with growth temperature. The data show that S drops a factor of 40 for growth temperatures greater than 740°C. The interface recombination velocity varies from a maximum of 20,000 cm/s (700°C growth) to a minimum of about 500 cm/s (775°C growth). In general, the interface recombination velocity of MOCVD-grown $Al_xGa_{1-x}As/GaAs$ improves with growth at temperatures greater than 740°C.

The smallest measured values of S on doped DHs were obtained by Lush and coworkers [33]. These DH devices were grown by MOCVD at 740°C. For an active layer doping of 1.3 x 10^{17} cm^{-3}, they found S less than 11 cm/s using a $Al_{0.30}Ga_{0.70}As$ window layer.

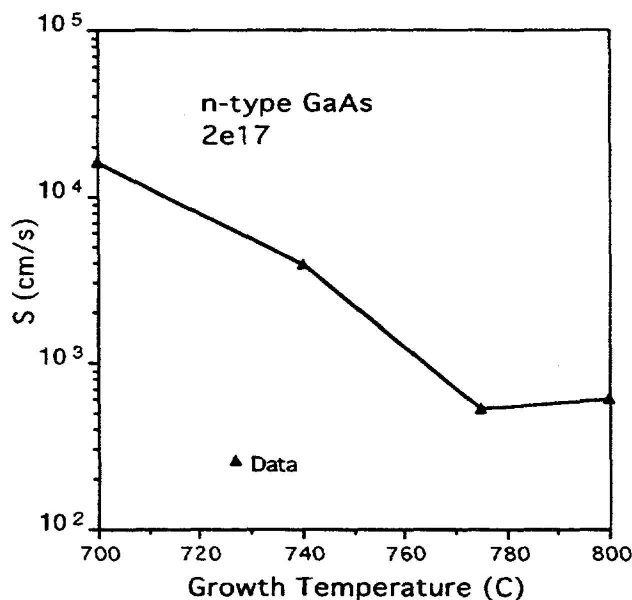

Figure 8: Interface recombination velocity versus growth temperature of GaAs DH devices.

MODELLING OF GaAs SINGLE JUNCTION DEVICES USING LIFETIME DATA

Single-junction GaAs devices, fabricated at Spire Corporation, were described in a previous paper [44] and are very representative of the current technology. That report described GaAs devices grown on both GaAs substrates and silicon substrates. The best GaAs-on-GaAs device had a one-sun efficiency of 24.7% and a 200-sun efficiency of 25.4%. By contrast, the best GaAs:Si device had a 1-sun efficiency of 17.6%. Most of these devices had companion DH diagnostic structures on which lifetime measurements were made.

Figure 9 is a plot of the V_{oc} and the J_{sc} versus base lifetime in seconds. The emitter lifetime was fixed at 0.5 ns. This is comparable to the measured emitter lifetime of 2.5 to 4 ns [45] for GaAs. The base lifetime varies over a range that has been measured in our laboratory for n-type GaAs doped to about 2 x 10^{17} cm^{-3}. The lowest lifetimes of about 10^{-10} seconds correspond to GaAs grown on silicon with no annealed buffer layer for strain reduction. The largest lifetimes of about 1 μs correspond to the data of Lush and coworkers, in which the substrate is removed for enhanced photon recycling. The V_{oc} increases from 856 meV at $\tau = 0.1$ ns to 1029.7 meV at $\tau = 1$ ms. At the same time, the J_{sc} increases from 24.3 mA/cm^2 to 27.3 mA/cm^2 over the same range of lifetimes. The V_{oc} is clearly much more affected by the lifetime variation.

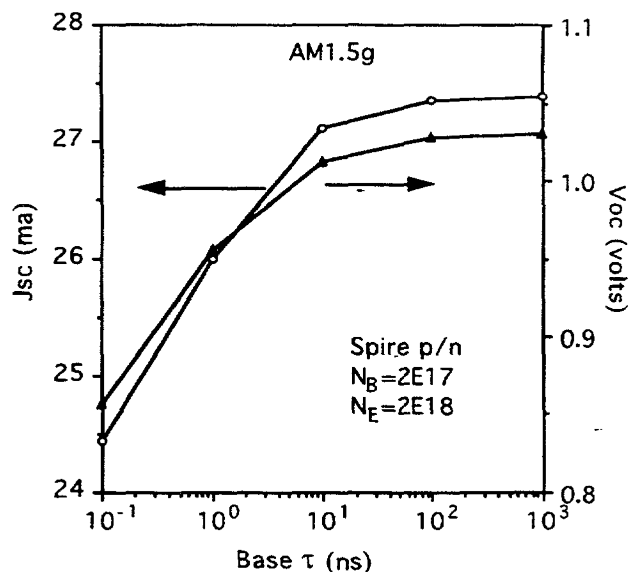

Figure 9: Calculated open-circuit voltage and short-circuit current for N+/P GaAs solar cell. Base lifetime is the independent variable.

Figure 10 is a plot of the TRPL low-injection lifetime of the materials versus the measured efficiency using an AM1.5g solar spectrum. The devices with base lifetimes of 2 ns or less were grown on silicon substrates. The calculated efficiencies of the device, with base lifetime as a variable, are shown in the figure. The base and emitter doping levels were fixed at 2 x 10^{17} cm^{-3} and 2 x 10^{18} cm^{-3}, respectively. The lower measured efficiencies for the GaAs:Si devices are undoubtedly due to degradation of the emitter lifetime due to dislocation propagation into the emitter. Taking the case respresenting a device grown on silicon with no subsequent heat treatment, the TRPL measurements indicate that the base lifetime is about 100 ps or less. Using an emitter lifetime of 8 ps in the model, the calculated efficiency is 8.9% and is in agreement with the data.

The vertical lines represent a range of GaAs lifetimes reported either in our laboratory or elsewhere. The lifetime region at A corresponds to GaAs devices grown directly on silicon without annealed buffer layers. The region about B corresponds to the best

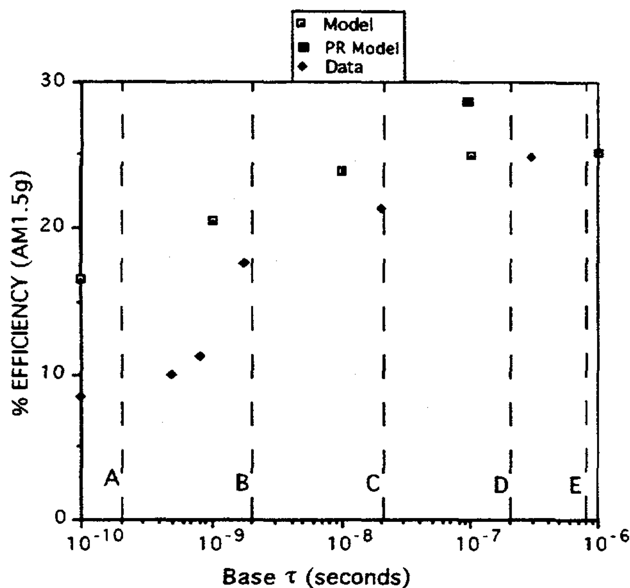

Figure 10: Calculated AM1.5 efficiency versus base lifetime in N+/P solar cells. Measured efficiency versus minority-carrier lifetime.

GaAs:Si devices with annealed buffer layers, while region C corresponds to the lifetime range found in bulk wafers. The region at D corresponds to the best MOCVD-grown epitaxial devices with low S values and with an enhanced radiative lifetime because of photon recycling. Finally, region E corresponds to a lifetime regime produced by enhanced photon recycling of the type found in the devices of Lush and coworkers [33]. The enhancement here is produced by etching away the substrate increasing the lifetime to about 1 μs. One sees that the efficiency has saturated, and there is not much improvement in performance between lifetime regions D and E. However, in these calculations, we have fixed the base doping at 2×10^{17} cm^{-3}. In practice, one could increase the base doping to, for example, 1×10^{18} cm^{-3} and thereby increase both V_{oc} and the fill factor. The calculated AM1.5 efficiency of this hypothetical device is 28.7%, and is shown. Photon recycling enhancement is an evolution of the technology and device design that more effectively utilizes the intrinsic optical properties.

A. $Al_xGa_{1-x}As$ Lifetimes

A review of lifetime measurements in $Al_xGa_{1-x}As$ can be found in some recent literature [1, 46, 47]. In contrast to GaAs, the lifetime in $Al_xGa_{1-x}As$ has been shown to be SRH limited over a wide range of doping levels. A composite of the published data is shown in Figure 11.

Among the first reported lifetime measurements on $Al_xGa_{1-x}As$ lifetime was that of van Opdorp and 't Hooft [48] on DHs. They grew DHs with $Al_yGa_{1-y}As$ confinement layers and $Al_xGa_{1-x}As$ (y > x) active layers over the composition range 0.4 < y < 0.62 and 0.10 < x < 0.17. These structures were grown both by liquid phase epitaxy(LPE) and by MOCVD [49]. These data indicate that the $Al_xGa_{1-x}As$ lifetime drops sharply with increasing Al concentration. This was the first work to report that the PL lifetime in $Al_xGa_{1-x}As$ increases with incident light intensity because of the SRH-dominated recombination.

A recent paper [50] presents data on MBE grown $Al_xGa_{1-x}As$ with x = 0.27 (p-type) and x = 0.365 (n-type). A thin AlAs confinement window layer was grown adjacent to the active layer. An outer window layer of $Al_{0.6}Ga_{0.4}As$ was used to protect the AlAs. The low-injection lifetimes in 4.0μm devices were 13.6 ns for the p-type structure and 11.6 ns for the n-type structure. By doing a thickness series, researchers found the S-value to be about 9×10^3 cm/s for the n-type DHs. Reproducible growth (in terms of lifetime) was reported for these structures.

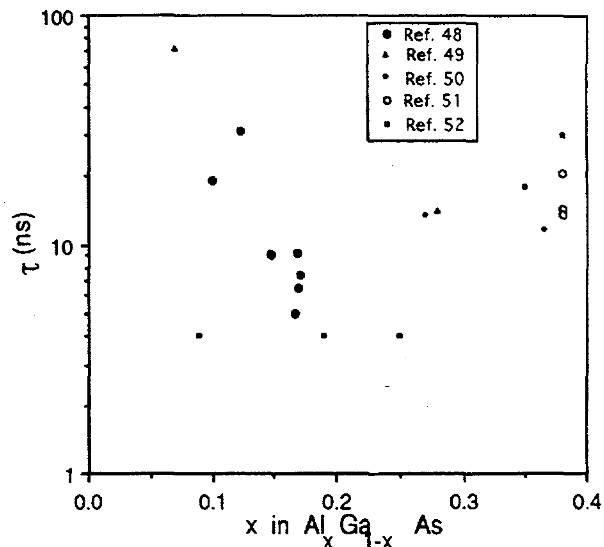

Figure 11: Summary of $Al_xGa_{1-x}As$ minority-carrier lifetime data versus aluminum concentration.

The largest lifetimes in high Al (x~0.40) compositions were grown by LPE. These were DHs [51] had active layers of composition n-$Al_{0.38}Ga_{0.62}As$ and window layers of n-$Al_{0.8}Ga_{0.2}As$ (the response of these devices has erroded over time as they had no GaAs protective layer to protect the n-$Al_{0.8}Ga_{0.2}As$).

Many devices in the series had hole lifetimes greater than 10 ns for active layers between 3.0- and 6.5-μm thick. A record low-injection lifetime of 20.2 ns was measured for a 5.0-μm device doped to 4×10^{15} cm^{-3}. Here SRH recombination is dominant, and no dependence on majority-carrier concentration was observed.

Zarem and coworkers [52] measured the PL lifetimes in MBE-grown, undoped $Al_xGa_{1-x}As$ DHs over the range 0 < x < 0.38 (x = 0.0, 0.9, 0.19, 0.25, 0.35, and 0.38). High-injection densities (3×10^{18} cm^{-3}) were used for the TRPL measurements. The measured lifetimes were less than the instrumental response, or about 4 ns for x < 0.35. At x = 0.35, τ_{PL} increases to 20 ns; and at x = 0.38, to about 30 ns. The lifetime is attributed to effects related the direct-indirect crossover. The alloy changes from a direct to an indirect gap semiconductor near x = 0.37 with E_g = 1.92 eV [53]. One expects a smaller B-value for increasing Al content. The authors described these effects using a model of population of the indirect L and X valleys relative to the direct Γ valley. Their model assumes that using the L and X valleys, B-values equal zero. For

larger X-values, the lifetime reduction should increase sharply, according to their theory.

Recent studies of the SRH defects of oxygen origin are described in another paper at this conference [54]. These are oxygen complexes that capture two electrons per center and are called double acceptors. Because of their large capture cross-sections for holes (q = -3 e), a fairly low concentration (~10^{14} cm^{-3}) effectively "kills" the minority-carrier lifetime in n-type material. These centers are deactivated or removed by growth above 740°C. The accumulation of these centers may account for the degradation of S when interfaces are grown at the lower temperatures (see Figure 8). The residual SRH centers that limit the lifetimes to 5 to 20 ns in bulk material are of unknown origin. High temperature growth has no apparent effect on the latter.

B. GaInP Lifetimes

GaInP, that is lattice-matched to GaAs, has shown very promising properties as both a wide band-gap passivating window layer and as a top junction in a cascade cell [55]. Recent measurements on undoped GaInP/GaAs DH devices have shown record long PL lifetimes. Figure 12 shows TRPL data of the best device of the series, which has a lifetime of 14.2 µs. This is a world record for minority-carrier lifetime in GaAs [56]. The best comparable $Al_xGa_{1-x}As$/GaAs devices have lifetimes of several µs. The S-value for the GaInP/GaAs was too small to deduce by only measuring two or more devices. However, our analysis [57] of temperature-dependent TRPL data indicated that the room-temperature S was less than 1.5 cm/s.

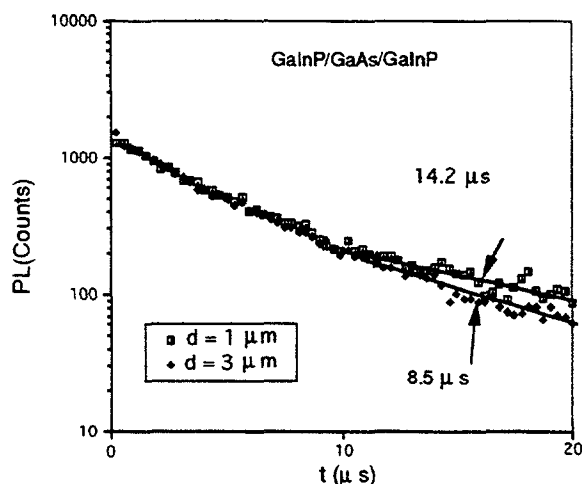

Figure 12: PL lifetimes of two GaInP/GaAs undoped DH structures.

Several DH diagnostic devices have been fabricated using the ternary $AlInP_2$ as the window/confinement layer. The band-gap of these GaInP alloys has been about 1.85 eV, and the lifetimes have ranged from 40 to 409 ns. These data are in marked contrast to $Al_{0.40}Ga_{0.60}As$ films that have a comparabale band-gap but much smaller lifetimes.

C. InP Lifetimes

InP-based technology has produced some very impressive high-efficieny solar cells. However, there is relatively little known about the minority-carrier properties of InP as compared to GaAs.

The radiative lifetime in InP should be very comparable to that in GaAs. InP is a direct-band-gap semiconductor with a room-temperature energy gap of about 1.34 eV. Application of the van Roosbroeck-Shockley relationship to the absorption spectra produces a B-coefficient very similar to that produced for GaAs. Data on InP has been marked by inconsistency and a large lifetime discrepancy between n- and p-type material. Also, in contrast to GaAs, bulk crystals have produced better lifetimes than epitaxial films.

Figure 13 shows a plot of available data on p-type InP from a variety of sources [58,59,60,61,62]. There is a great deal of scatter in the data, but the values generally are smaller than those of GaAs with comparable doping. The solid line is an estimate of the radiative lifetime assuming that B = 2 x 10^{-10} cm^3/s; i.e., that B has the same value as for GaAs. The data by Ahrenkiel and coworkers [61] lies above the estimated radiative lifetime and was obtained on Zn-doped wafer material. However, most of the data lie at least a factor of 10 below the estimated τ_R. One must suspect that some SRH defect is a contaminant in p-InP, but there is not definitive evidence for that speculation.

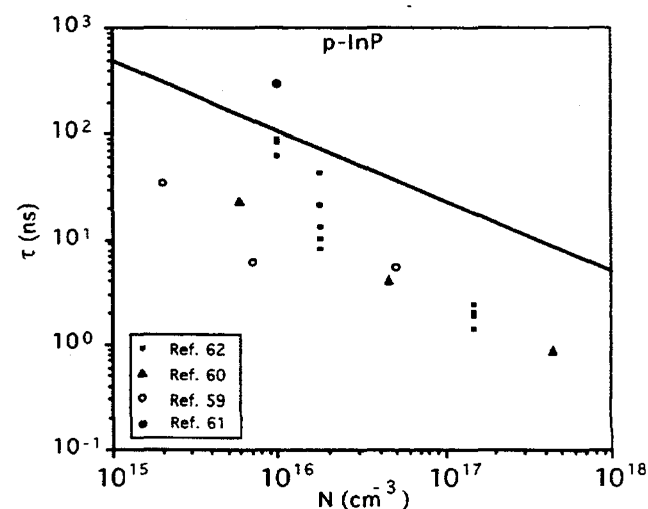

Figure 13: Summary of minority-carrier lifetimes of p-type InP versus hole concentration.

Figure 14 shows a plot of available data [60,62,63,64,65] on n-type InP from several different sources. Again, the estimated radiative lifetime is represented by the solid line, and most of the data lie above the line for n-type material. This observation has been noted in numerous reports; i.e., that n-type InP has much longer lifetimes than p-type InP. These data certainly have important consequences for new PV cell design. The mechanism of the difference between n- and p-type InP lifetimes is the focus of some current research [66].

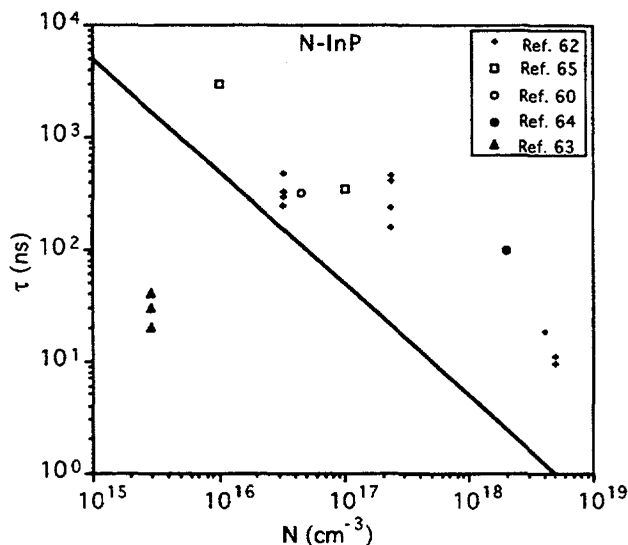

Figure 14: Summary of minority-carrier lifetimes of n-type InP versus electron concentration.

CONCLUSIONS

The maximization of minority-carrier lifetimes in PV materials is an important component of the materials research and development. Significant improvements in materials technology have been made in the last half decade of PV research. The TRPL technique is extrementy useful for research as well as quality control as these measurements relate so directly to PV performance.

ACKNOWLEDGMENTS

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RECOMBINATION EFFECTS AT OXYGEN RELATED DOUBLE ACCEPTORS IN $AL_{0.10}GA_{0.90}AS$

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ABSTRACT

$Al_xGa_{1-x}As$ is an important component of many high-efficiency photovoltaic devices. This work shows that the hole lifetime of n-type $Al_{0.10}Ga_{0.90}As$ is controlled by impurity-oxygen-related recombination centers with capture cross sections of about 10^{-12} cm^2 when the films are grown at temperatures of 720°C and lower. Correlated time-resolved photoluminescence and deep level transient spectroscopy measurements link these centers to well known impurity oxygen complexes. Film growth at temperatures above about 720°C eliminates these oxygen complexes from the epitaxial layer resulting in greatly improved photovoltaic properties.

INTRODUCTION

$Al_xGa_{1-x}As$ grown by metalorganic chemical vapor deposition (MOCVD) plays an important role in photovoltaic (PV) devices. It is used as both a wide band-gap component in multijunction devices and as a passivation/confinement layer for GaAs cells. MOCVD growth appears to be the preferred method of device fabrication for numerous reasons. These include the speed of fabrication, ease of making multilayer structures, and ability to scaleup to large area. Previous work has indicated that "good," high lifetime $Al_xGa_{1-x}As$ must be grown at temperatures of 740°C or higher. However, higher growth temperature produces interdiffusion problems that are undesirable. The ability to grow high-quality MOCVD $Al_xGa_{1-x}As$ at lower temperature would be very desirable for PV manufacturing technology. Here we investigated the defects by deep level transient spectroscopy (DLTS) in $Al_xGa_{1-x}As$ grown over a range of temperatures. Higher temperature growth appears to irradicate many of these defects from the film. Defect concentrations were correlated with minority-carrier lifetime measurements on the same films. This work showed that oxygen-related defects cause lifetime degradation and disappear with growth temperatures above about 720°C.

PREVIOUS WORK

Prior work has indicated that $Al_xGa_{1-x}As$ films grown by liquid-phase epitaxy [1] and by molecular beam epitaxy [2] have larger minority-carrier lifetimes than MOCVD-grown layers. Various compositions of $Al_xGa_{1-x}As$ are used in multijunction solar cells. The minority-carrier lifetime [3] is greatly improved by higher growth temperatures, and the concentration of recombination centers is believed to be accordingly reduced. The source of these recombination centers is generally believed to be related to oxygen or water-vapor contamination. Our work was limited to alloys with $x < 0.20$ to avoid the complication of DX-center formation.

Numerous reports indicate that oxygen defects are introduced during MOCVD growth that are lifetime killers. These are electron traps and would not be expected to be recombination centers in n-type $Al_xGa_{1-x}As$. This work will identify the recombination mechanism associated with these traps.

Electron traps with activation energies between 0.3-0.6 eV have been related to the presence of oxygen in AlGaAs and are highly sensitive to growth conditions [4,5]. A negative correlation was found between luminescence efficiency and the density of these electron traps [6,7,8] in n-type material. Wallis and coworkers [7] deliberately introduced oxygen during MOCVD growth of $Al_{0.10}Ga_{0.90}As$ and reported an oxygen-related deep level at 0.46 eV. Andre and coworkers [9] detected electron traps at about 0.3, 0.5, and 0.8 eV in $Al_{0.15}Ga_{0.85}As$, and the concentrations decreased with growth temperature. Sakamoto and coworkers [5] found two electron traps in undoped $Al_{0.10}Ga_{0.90}$ and selenium-doped $Al_{0.10}Ga_{0.90}$ that were not intentionally doped with oxygen. They labeled these the A (0.27-eV) and the B (0.41-eV) trap and found that the concentrations were always about equal. They found the ratio of photoluminescence (PL) intensity to donor density decreased with the concentration of A and B traps. Recently, Watanabe et. al [10] showed that an electron trap at 0.45 eV acted as an effective recombination center in the AlGaAs epilayer and reduced the current gain of heterojunction bipolar transistors (HBTs).

EXPERIMENTAL TECHNIQUES

In this report, we investigate electron traps in Se-doped, MOCVD-grown $Al_{0.1}Ga_{0.9}As$ epitaxial films. The source materials for the Ga, Al, and As were trimethylgallium (TMG), trimethylaluminum (TMA), and liquid arsine (AsH_3), respectively. This composition was chosen to avoid the complication of DX-center formation on the data interpretation. All the films in this study were grown in a vertical MOCVD reactor using palladium-purified hydrogen as the carrier gas. The films were grown at reduced pressure (33.33 kPa) [250 Torr] using a carrier flow of 6 l/

min. Hydrogen selenide (H_2Se), diluted to 50 parts per million in purified hydrogen, was the n-type dopant source in all growths. Substrates were (100)-oriented GaAs wafers, that were mounted on an inductively-heated, silicon-carbide-coated graphite susceptor. The growth temperatures were 6608°, 700°, 720°, and 780°C.

Correlated measurements were made using DLTS and time-resolved photoluminescence (TRPL). Some secondary ion mass spectroscopy (SIMS) measurements were made on selected films. Even though oxygen was not intentionally added, it was detectable by SIMS for films grown at 660°C. No detectable oxygen was found by SIMS in samples grown at the higher temperatures.

The epitaxial structure designed for this study is a double heterojunction (DH). $Al_{0.1}Ga_{0.9}As$, grown 2- to 5-um-thick, is the active layer and sandwiched between thin $Al_{0.8}Ga_{0.2}As$ confinement layers. Doping densities in the active layers range from 1-2 x 10^{17} cm^{-3}, determined from capacitance-voltage (C-V) measurements. After growth, the DH structures are scribbed into two pieces, one for DLTS measurements and the other for photoluminescence (PL) measurements. No further processing is needed for the PL sample. For samples intended for DLTS work, the top $Al_{0.8}Ga_{0.2}As$ is removed selectively by wet-chemical etching with peroxide/ammonium hydroxide solutions. Gold dots are deposited on the $Al_{0.1}Ga_{0.9}As$ surfaces to form Schottky barriers. Hence, the same active layer is examined by both PL and DLTS. Minority- and majority-carrier traps are determined from DLTS. Minority-carrier lifetime is extracted from TRPL. Thus the same active layer is investigated by both techniques in order to correlate distinct traps with minority-carrier lifetime.

No minority-carrier traps were found directly by the DLTS technique, indicating that the former lie well above the valence band. Our measurements indicated fairly large concentrations of majority-carrier, electrons traps that we labeled A, B, and C for epi-layers grown at 660°C. These are apparently the same traps found by Sakamoto [5] and by Wanatabe [10]. Some representative DLTS data, from three different samples, are shown in Fig. 1, with the rate window set to 23.25 s^{-1}. Sample #1562 had only A-centers, #1366 had only B-centers, and #1638 had only C-centers. Our work indicates that the relative concentration of the three traps varies from sample to sample. Most of our samples contained only one of these three types of centers. The defect concentration in each sample is shown in the table, and they varied from about 2 x 10^{14} to 3 x 10^{15} cm^{-3}.

By doing a temperature scan with seven different rate windows, an Arrenhius plot was generated for each of the defects. This plot is shown in Fig. 2 for the three samples of Fig. 1. The energy levels are 0.32 eV (A trap), 0.46 eV (B trap), and 0.56 eV (C trap) for x = 0.10. The C-V measurements indicate that these low-temperature films are partially compensated. The A, B, and C traps all have the common property of capture cross sections less than 10^{-20} cm^2, as described in the next section. Several deeper electron traps, with large cross sections (10^{-16} cm^{-2}), are occasionally found in the 0.65 eV to 0.90 eV range, but these do not appear to be recombination centers.

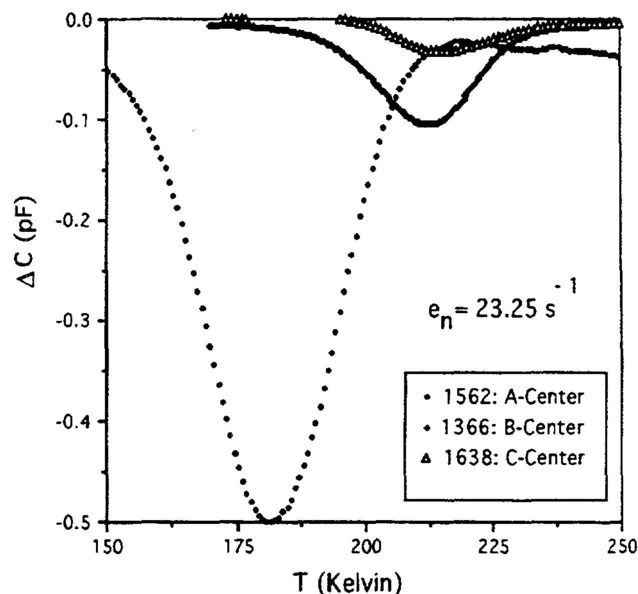

Figure 1: DLTS signals for the A-, B- and C-centers in three different $Al_{0.10}Ga_{0.90}As$ films with a rate window of 23.25 s^{-1}.

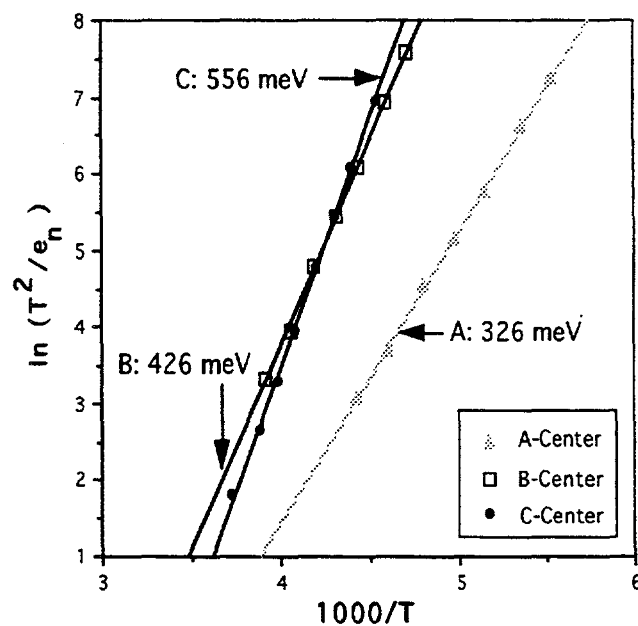

Figure 2: Arrenhius plots for the A-, B- and C-center using DLTS data from 7 temperature scans.

CAPTURE CROSS SECTION AND DOUBLE ACCEPTOR MODEL

Capture cross section measurements were made on the A, B, and C traps as a function of temperature. The standard technique for measuring the capture cross section, σ, is to measure ΔC versus the filling-pulse width, t_p, and fit the following expression to the data

$$\Delta C(t_p) = \Delta C_{max}[1 - \exp(-n v_{th} \sigma_n t_p)] \qquad \text{(Eq. 1)}$$

Here, n is the free-electron density, v_{th} is the thermal velocity, and s_n is the electron-capture cross section.

In our measurements, rather long pulses (0.2 to 1.0 ms) were required to saturate the DLTS signal DC. The data for the A and B traps could not be fitted with the single electron capture model given by Eq. 1. Figure 3 shows capture rate data for the B trap at a sample temperature of 232 K. Curve 1 is the best fit to the data using Eq. 1. The data could be accurately fitted with a model that assumes that two electrons are sequentially captured by the center [11]. One can write a set of coupled differential rate equations assuming that the trap may contain no electrons, (N_0), one electron (N_1), or two electrons (N_2). Using c_1 and c_2 as the capture rates for one and two electrons, respectively, one finds that $c_1 = n\, v_{th}\, s_1$ and $c_2 = n\, v_{th}\, s_2$. The boundary conditions are N_1 and $N_2 = 0$ at $t = 0$ and $N_0 + N_1 + N_2 = N_t$, the total number of traps. The solutions are easily found by application of Mathematica [12] to the coupled differential equations. The total electronic charge on the centers is simply $N_1 + 2N_2$. The charge density per trap is shown to be

$$n(t) = 2 - \frac{(2c_2 - c_1)}{c_1 - c_2}\exp(-c_1 t) - c_1/(c_1 - c_2)\exp(c_2 t) \qquad \text{(Eq. 2)}$$

In Figure 1, Curve 2 is a fit of Eq. 3 to the experimental data, and the fit is very good. The parameters coming out of this fit are

$$\sigma_1 = 1.24\ 10^{-20}\, cm^2$$
$$\sigma_2 = 1.46\ 10^{-21}\, cm^2 \qquad \text{(Eq. 3)}$$

These very small cross sections are characteristic of the A-, B-, and C- centers and indicate a repulsive, electrostatic potential. The repulsive nature is verified by measuring these capture cross sections versus temperature and finding that σ is thermally activated, increasing with temperature. The capture cross section versus temperature is fit with the function in Fig. 4.

$$\sigma_n(T) = \sigma_\infty \exp(-E_b / KT) \qquad \text{(Eq. 4)}$$

Here σ_∞ is the capture cross section at infinite temperature, and E_b is the repulsive barrier height. For the B-center, the barrier height for the first electron is 71 meV; for the second electron, it is 142 meV. This measurement is consistent with the double-acceptor model, and the repulsive barrier height increases with the addition of the first electron.

In the neutral regions of the n-type material, the A and B traps are negatively charged with two electrons. As the low temperature capture cross section is very small (~10^{-20} cm^2) for the first electron, the unoccupied trap must be negatively charged. Therefore, the fully occupied trap must have a negative charge of at least -3q, where q is the electronic charge. Consequently, the traps have an attractive Coulomb potential for holes and, therefore, have a very large capture cross section. This contention is verified by PL lifetime measurements on the same films. A strong inverse correlation between A-, B-, and C-trap concentrations and the PL lifetime is shown in Table 1. The relationship between PL lifetime and minority-carrier lifetime has been explained in the literature [13].

PHOTOLUMINESCENCE LIFETIME

This work indicated an inverse correlation between the hole lifetime and the density of A-, B-, and C-type electron traps. These data are shown in the Table below. When measurable densities of these traps are detectable, the hole lifetime is always subnanosecond. The DLTS technique is able to detect double acceptor electron traps only for films grown at temperatures below 720°C.

Figure 5 shows the PL decay of a series of three $Al_{0.10}Ga_{0.90}As$ films grown identically except for temperature. The samples numbers and respective growth temperatures here are indicated in Table 1. A confinement layer of $Al_{0.80}Ga_{0.20}As$ was grown on top of each active layer to form a double heterostructure. DLTS measurements of the adjacent film indicated A traps with a volume density of 4.0 x 10^{14} cm^{-3} in sample 1366. No detectable DLTS signals from A or B traps were found for samples 1381 and 1385. Thus, higher temperature growth reduces the the A and B trap levels below DLTS detectability.

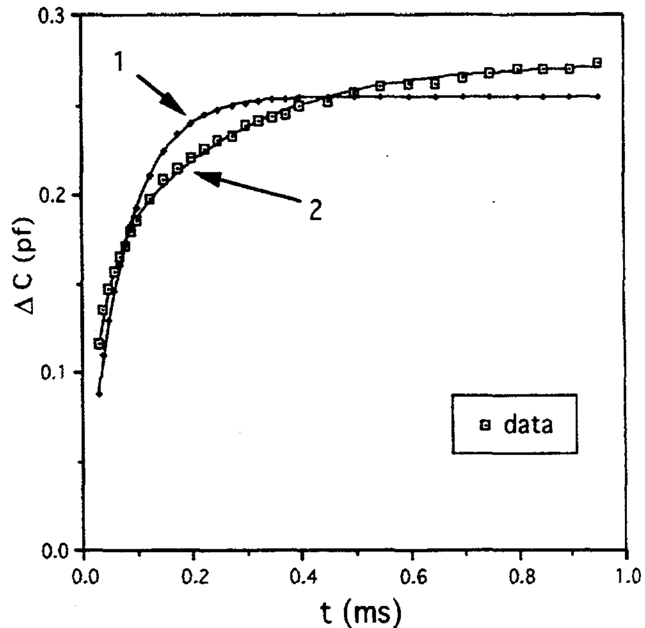

Figure 3: DLTS data (DC) versus filling pulse width t for the B center in $Al_{0.10}Ga_{0.90}As$. Curve 1 uses a 1-electron model and Curve 2 uses a 2-electron model.

TABLE 1			
Sample	Growth Temp (C)	Trap Type and Density (cm^{-2})	Lifetime (ns)
1366	660	B: 3.9 E14	0.123
1562	660	A: 3.2 E14	0.022
1638	660	C: 2.1 E14	0.076
1381	720	none detectable	6.86
1385	780	none detectable	17.2

The PL lifetime increases from 123 ps (3.9×10^{14} cm^{-3} A traps) to 17.2 ns (no detectable A traps) as the growth temperature is increased form 660°C to 780°C. Adding the reciprocal lifetimes from the B trap contribution and the other, unknown contributions, one can calculate the hole capture cross section of the former.

$$\frac{1}{\tau_{pl}} = \frac{1}{\tau_A} + \frac{1}{\tau_{SRH}} \quad \text{(Eq. 5)}$$

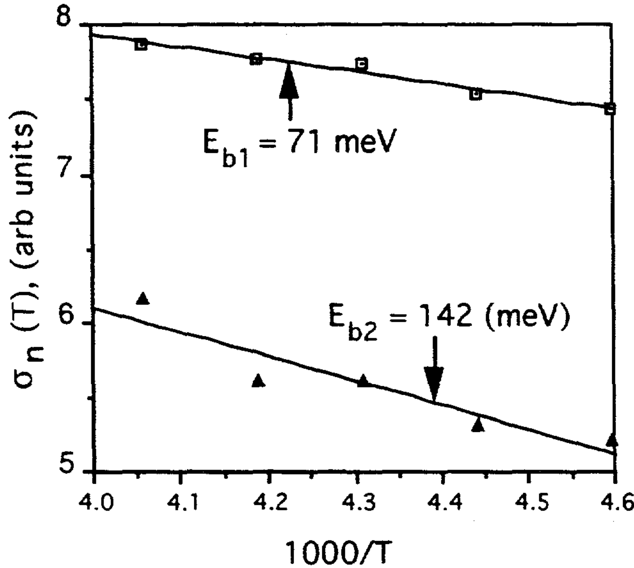

Figure 4: Temperature dependence of the electron capture cross sections, s_1 and s_2, of the B center in $Al_{0.10}Ga_{0.90}As$. The repulse barriers heights E_{b1} and E_{b2} are indicated in the figure.

Here, the PL lifetime is broken down into contributions from the A trap and the background Shockley-Read-Hall (SRH) recombination from other bulk states and from the interfaces. Here we take t_{SRH} as the measured lifetime of sample 1385 and assume that no A centers are present in that sample. Knowing N_t and v_{th}, the hole-capture cross section of the A trap is calculated to be 1.63×10^{-12} cm^{-2}. The lifetime of sample 1385 is larger than that of sample 1381. Assuming the lifetime reduction is due to an undetectable quantity of B centers, and using the calculated hole cross section, the concentration of B centers in sample 1381 is 4.6×10^{12} cm^{-3}. The calculated concentration is below the detection limit of our DLTS apparatus.

RECOMBINATION THEORY

In order for the lifetime data to be compatible with a model with the A, B, or C traps acting as recombination centers, one must consider the recombination theory for such processes. The very large cross section deduced from the lifetime data must be compatible with a model involving the attractive potential for holes of the A center. Lax has developed a theory [14] of cascade capture of electrons or holes by impurity levels in semiconductors. This model was expanded by Gibbs and coworkers [15] and applied to defect centers in GaP. For impurity centers with a Coulomb attractive potential, the model describes electron capture in excited-effective-mass states with binding energies greater than the thermal energy. As the sample is cooled, the capture rate in higher-lying Rydberg levels increases. If the relaxation to the ground state is independent of temperature, the cross section varies as

$$\sigma_T \sim T^{-2} \exp(E_c / KT) \quad \text{(Eq. 6)}$$

Here, E_c is the binding energy of the highest excited capture state. An example of the above is a radiative transition to the ground state. In this case, the inverse of the minority-carrier lifetime therefore varies as [13]

$$\frac{1}{\tau} = AN_t T^{-1.5} \exp(E_c / KT) \quad \text{(Eq. 7)}$$

Here, A is a constant; N_t is the trap density. The temperature dependence of the thermal velocity (v_{th}) produces the $T^{-1.5}$ dependence in Eq. 8.

When the cascade process is temperature dependent, such as for multiphonon emission, Eq. 8 is modified as

$$\frac{1}{\tau} = AN_t v_{th} T^{-2} \exp[(E_c - E_A)/KT] \quad \text{(Eq. 8)}$$

Here, E_A is the thermal activation energy of the cascade process.

In either case, the minority-carrier lifetime decreases exponentially with temperature. Figure 6 is a plot of the PL lifetime versus temperature for a devic grown at 720°C. We have seen that such devices have small concentrations of A, B, or C centers that influence the lifetime. We see that the lifetime behaviors follows Eq. 8 with two different activation energies over the measured temperature range. A detailed analysis of these data indicate that two excited states are active over the indicated temperature range and the behavior is described by the Lax model [14].

One can make an estimate of the binding energy and capture radius by using a simple Rydberg, effective mass model. Using these data, σ_p was calculated as 4.6×10^{-12} cm^2, and the simple model gives an order of magnitude agreement with the data.

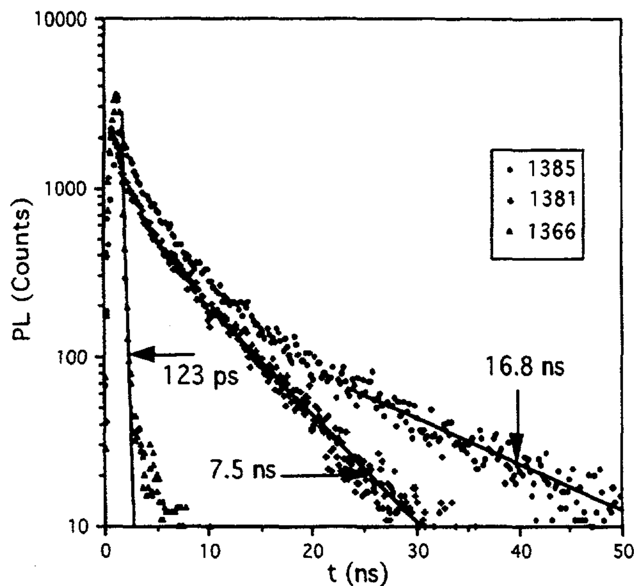

Figure 5: Time-resolved photoluminescence in three DH devices that are identical except for growth temperature. The growth temperatures are Curve 1: 660°C; Curve 2: 720°C; and Curve 3: 780°C. The A center concentration for the device of Curve 1 is about 4×10^{14} cm^{-3}. No A centers were detectable by DLTS in the devices of Curves 2 and 3.

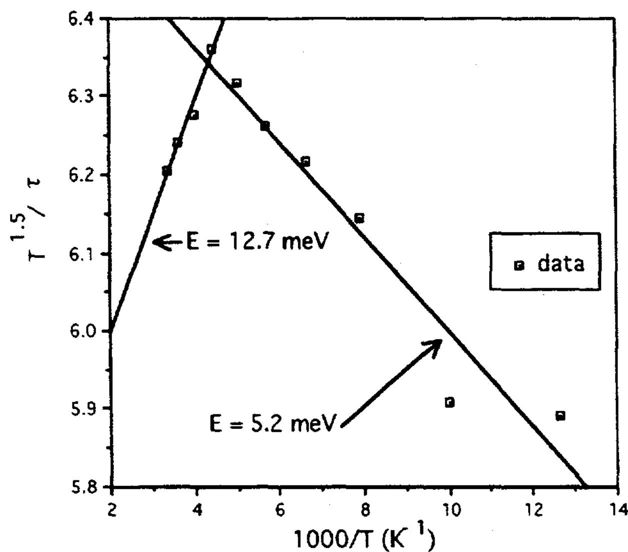

Figure 6: A plot of T^2/t versus inverse temperature for a device grown at 720°C.

CHEMICAL BASIS OF DOUBLE ACCEPTOR FORMATION

The A, B, and C centers are not found in GaAs, suggesting that the double acceptor contains both aluminum and oxygen. Wallis and coworkers [7] concluded that a deep acceptor is formed from an Al-O complex. We believe that the source of the oxygen is from residual contamination of most TMA sources. Because TMA exists as a dimer at room temperature, we can conceive of two possible configurations that are the source of the three traps. The oxygen may insert between an Al-C bond, forming an Al-O-C complex, or oxygen may bridge the two Al atoms in the dimer, forming an Al-O-Al complex. The Al-O bonds are quite stable, having a bond energy of about 400 cal/mole, and only at high growth temperatures are Al-O concentrations reduced in AlGaAs grown by MOCVD. This is consistent with our SIMS results and the lack of reported successful MOCVD-grown AlGaAs PV devices (and other minority-carrier devices) using TMA and low-growth temperatures. Our experimental technique does not distinguish among these different chemical models.

CONCLUSION

DLTS studies on n-$Al_{0.10}Ga_{0.20}As$ grown by MOCVD show the presence of three different centers that act like double acceptors. The binding energy of these centers corresponds to that found by other workers after the intentional addition of oxygen. The density of these centers decreases with increasing growth temperature. Oxygen is detectable by SIMS analysis for films grown at the lowest temperature of 660°C. These centers have a repulsive cross section for electrons. By contrast, they have a huge cross section for holes, with room-temperature cross sections greater than 1×10^{-12} cm^2. The temperature dependence of the hole lifetime is indicative of hole capture by Rydberg-like, excited states. This capture is followed by a phonon cascade process to the ground state, resulting in hole annihilation. The key to making high lifetime $Al_xGa_{1-x}As$ at lower growth temperature appears to be removing oxygen impurity from the contaminated starting materials used for MOCVD growth.

ACKNOWLEDGEMENT

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NEW INSTRUMENTATION FOR MEASURING SPECTRAL EFFECTS DURING OUTDOOR AND INDOOR PV DEVICE TESTING

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BACKGROUND

It is well known that the performance of any photovoltaic (PV) device is a function of the spectral response of the device and the spectral content of the optical radiation. In a PV device testing environment, the spectral characteristics of the radiation must be taken into account. The purpose of this work is to describe some instrumentation being developed at the National Renewable Energy Laboratory (NREL) to quantify spectral characteristics for both outdoor and indoor test environments.

THE ATMOSPHERIC OPTICAL CALIBRATION SYSTEM

For outdoor testing, reference cells, spectral corrections from concurrent spectral measurements, and spectral models driven by meteorological conditions have been used to adjust PV data for spectral changes. There are advantages and disadvantages to each of these. An alternative to these methods, being developed at NREL, is the patented Atmospheric Optical Calibration System (AOCS). The AOCS instantaneously measures certain optical properties of the atmosphere at the time each PV measurement is made. By parameterizing these optical properties, comparison can be made with standard optical properties at the time of the test. Rather than correct all of the PV data to existing spectral conditions, the data may be accepted, corrected, or rejected based on the magnitude of the AOCS parameter, Δ.

Briefly, measurements are made of the optical aerosol transmission of the atmosphere at 0.5-μm wavelength, the diffuse-to-global photon flux ratio on the horizontal plane over the range 0.4 to 0.7 μm, and the atmospheric precipitable water vapor from the ratio of direct beam irradiance at 0.862 μm (a water vapor window) to direct-beam irradiance at 0.942 μm (a water vapor absorption band). These measurements are compared with modeled optical conditions for a cloud-free atmosphere.

The principle of this technique is shown in Figure 1, a plot of atmospheric transmission at 0.5 μm ($T_{0.5}$) against the diffuse-to-global photon flux ratio (SHGH). The curved line represents modeled values averaged from a series of calculations using a spectral transmission model. The point at SHGH=0.33, $T_{0.5}$=0.67 corresponds to ASTM 891,892 standard outdoor test conditions. The ASTM standards also specify atmospheric precipitable water vapor (PWV) at 1.42 cm. Figure 1 lies in the PWV=1.42 cm plane with the PWV axis extending out of the origin. The dots and crosses represent actual measurements for air mass between 1.4 and 1.7 taken at NREL over a 4-day period. The AOCS parameter is a vector defined by

where

$\partial_1 = T_{meas} - T_{std}$

$\partial_2 = SHGH_{meas} - SHGH_{std}$

$\partial_3 = \beta\,(PWV_{meas} - PWV_{std})$

β = PWV weighting fraction

and extends from the standard conditions point (std) to any measured point (meas). If the length of Δ exceeds some predetermined value, Δ_{min}, the PV data are rejected; otherwise, they are accepted. A less conservative approach is to accept all PV data for $\Delta \le \Delta_{min}$ and do spectral corrections when Δ is within a range $\Delta_{min} < \Delta \le \Delta_{max}$.

Figure 2 shows PV total-area efficiency (TAE) data taken on an amorphous Si module at the same time the AOCS data of Figure 1 were taken. Without considering the water vapor component (β = 0), all data within the circle of radius Δ_{min} = 0.15 are accepted as indicated by the Xs; the squares represent rejected data. When the PWV component is added (β = 0.11), additional points are rejected. The results are summarized in the following table.

Table 1

AOCS parameters	Average TAE	Standard deviation on TAE	Number of accepted points	Airmass Range
No constraints	3.23	0.247	218	1-4
Δ=0.15 β=0	3.42	0.109	7	1.4-1.7
Δ=0.15 β=0.11	3.42	0.033	4	1.4-1.7

Note the reduction in standard deviation achieved by use of the AOCS.

SPECTRORADIOMETERS FOR PULSED SOLAR SIMULATOR MEASUREMENTS

Three instruments are under development for measurement of the spectra of pulse solar simulators: a diode-array system for

instantaneously capturing the entire spectra, an integrating charge amplifier system to measure the time-integrated spectra, and a pulse-storage system to measure time-resolved spectra. The diode array system can measure from 0.3 to 1.1 μm; the others from 0.3 to at least 1.8 μm. The data will be used to account for spectral effects in the pulse simulator illuminant compared with outdoor illumination.

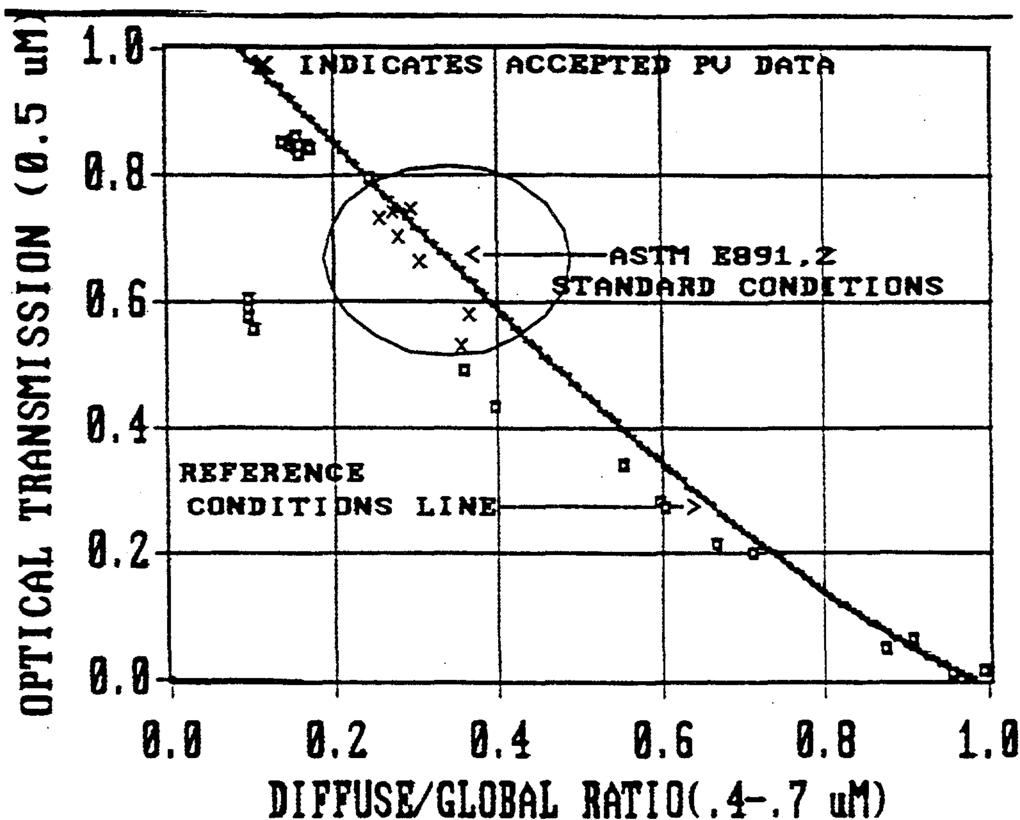

Figure 1. Optical transmission at 0.5 μm vs. SHGH in the PWV = 1.42 plane. The line represents values calculated from atmospheric transmission theory, the dot at (0.33, 0.67) ASTM 891,892 standard testing conditions, the circle the AOCS parameters limit (Δ) = 0.15.

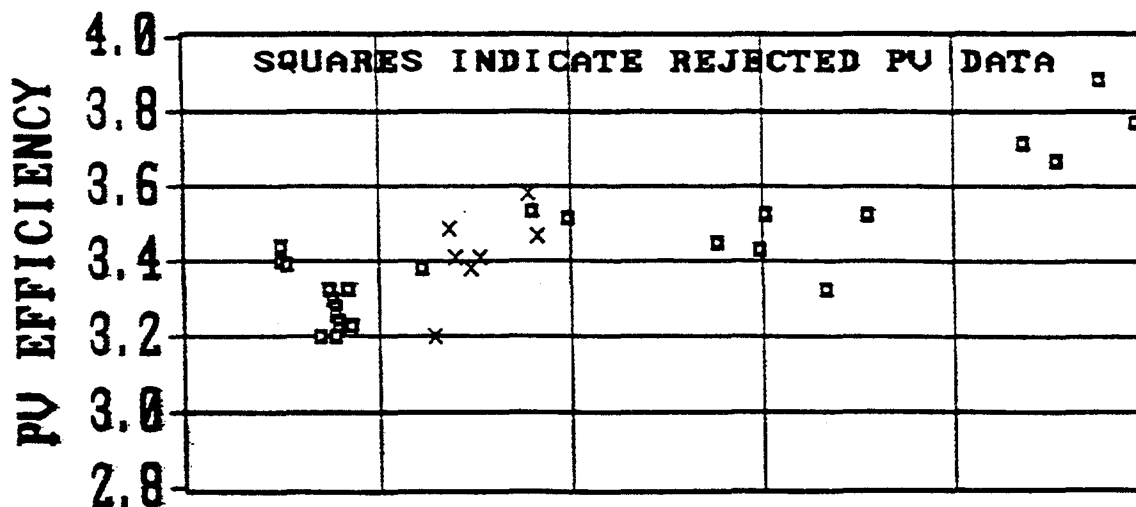

Figure 2. Amorphous Si efficiency vs. SHGH for the data of Fig. 1. The Xs represent data for Δ < = 0.15, the squares Δ > 0.15 and ß = 0 i.e., PWV component ignored.

The diode array spectroradiometer is an EG&G OMAIII that uses a 1024-element silicon detector array, allowing all wavelengths over the 0.285-1.1-µm wavelength range to be measured simultaneously. A representative spectral scan on a Spire pulsed simulator, normalized to unit area, from the OMA III system is shown in Figure 3, with integrated values compared with the ASTM E927 *standard specification for solar simulation for terrestrial photovoltaic testing* spectral distribution in Figure 4. The distribution defines the simulator as Class A.

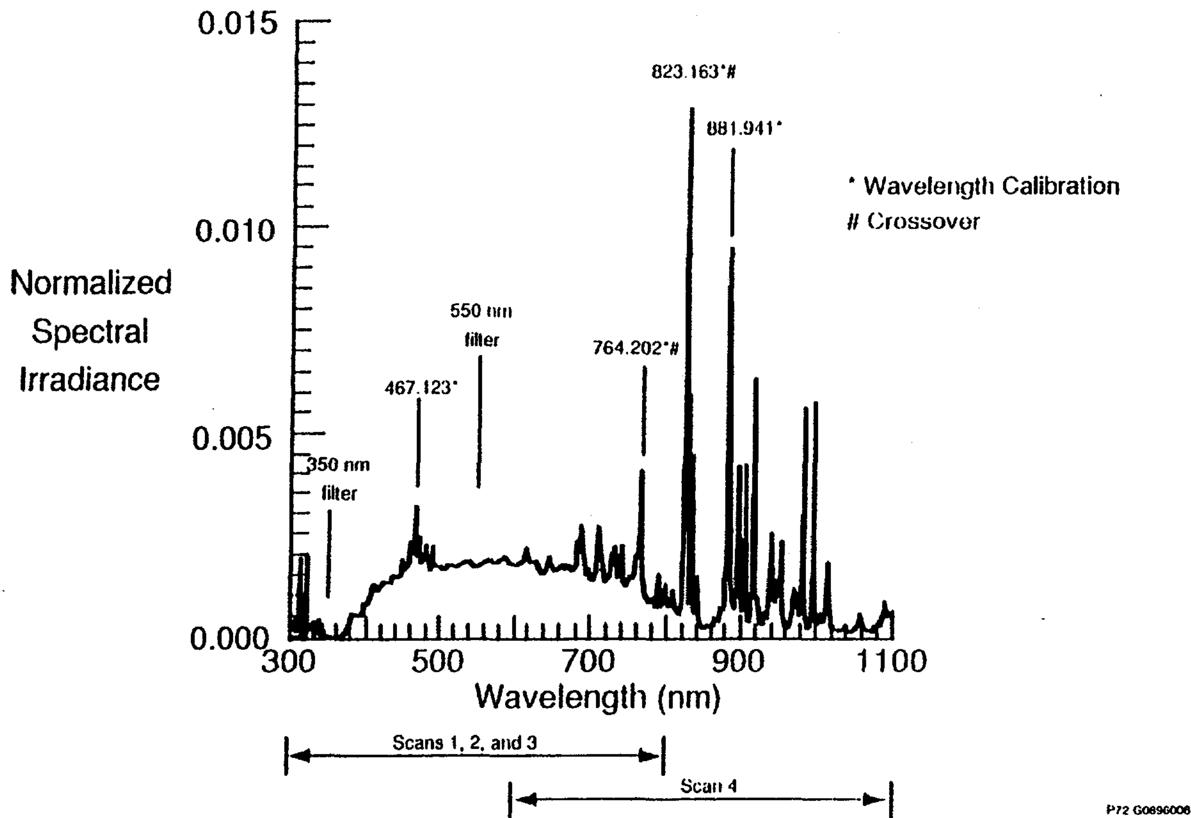

Figure 3. Representative spectra of Spire Pulsed Simulator measured with the OMA III Multichannel array system

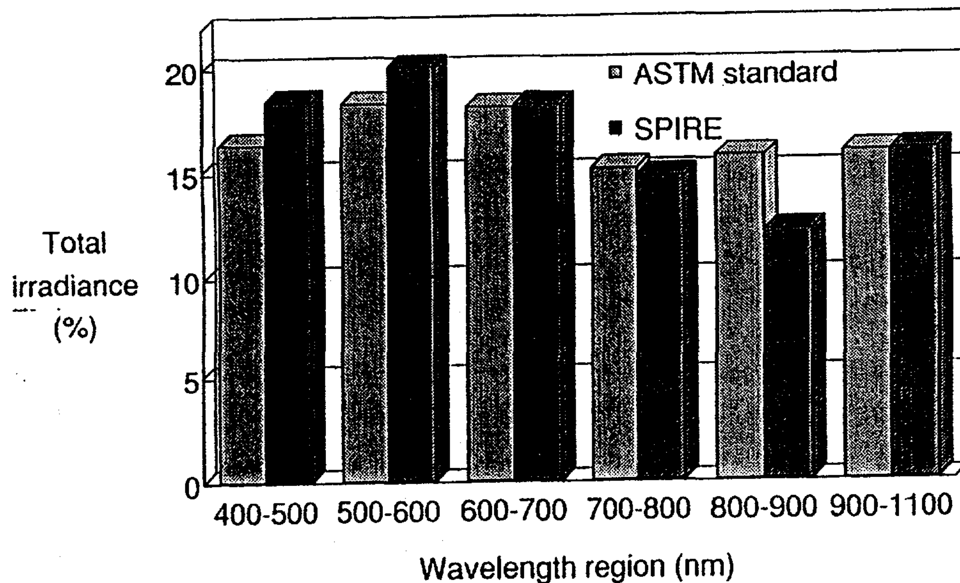

Figure 4. Comparison of integrated measured spectra of Spire simulator with ASTM927 standard values

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In order to measure the entire spectrum from 0.3 to 1.1 μm, four measurements were necessary: no filter, 0.350, and 0.550-μm order sorting filters for the 0.3-0.8-μm scans, and the 0.550-μm filter for the 0.6-1.1-μm scans. Custom software consisting of BASIC programs and MS-DOS batch files were developed to automatically process the data. The software automatically wavelength-calibrates each file to four Xe lines (0.4671, 0.7642, 0.8232, and 0.8819 μm) and merges the four files to create each spectrum, with intensity matching at three (0.350, 0.550, and 0.745-μm) crossover points. Merged-file data are then normalized to peak wavelength (for presentation purposes) and are finally normalized to the total energy in the 0.4-1.1-μm region.

The integrating charge amplifier system scans the spectrum one wavelength at a time using a conventional scanning monochromator. The integrating charge is calibrated against a NIST spectral-lamp standard by use of a chopper wheel that generates a light pulse of known time-integrated area. Comparisons of the integrated charge technique are being made with the OMA III to determine the effects of scattered light and stability of the OMA III system. Additionally, the charge amplifier system can be used with a Ge detector to extend the wavelength range to about 1.8 μm.

The pulse-storage system allows storage of the actual pulses. Time-resolved data are obtained from the pulse so that spectral changes throughout the duration of the pulse can be measured. This system uses the same monochromator system as the integrating charge system, but stores the time-resolved pulse rather than its integrated value. The three methods are being intercompared to determine bias errors for the measurements.

For further information see the references [1-2].

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GRAIN BOUNDARY AND DISLOCATION EFFECTS ON THE PV PERFORMANCE OF HIGH-PURITY SILICON

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ABSTRACT

To quantify the effects of grain size and dislocation defects on the minority charge carrier lifetime τ and photovoltaic (PV) efficiency of silicon, we grew high-purity, float-zoned (FZ) ingots with a range of grain sizes from single crystalline (dislocated and dislocation-free) down to 4×10^{-4} cm^2. In situ ingot cooling rates of 18° and 89°C min^{-1} were used. Bulk ingot τ ranged from less than 30 µs for the multicrystalline ingots to 2,500 µs for the dislocation-free crystals. Wafers from different positions in the ingots were used for τ measurements and the fabrication of mesa-isolated, 0.04-cm^2 diagnostic PV device structures. We found that τ decreased to 4 µs and normalized solar cell efficiency decreased to 0.6 for the smallest average grain areas (4×10^{-4} cm^2).

INTRODUCTION

Thin-layer multicrystalline silicon photovoltaic device structures that incorporate multiple light passes are expected to have less stringent requirements on minority charge carrier lifetime τ than those of conventional thick cells because light-generated carriers have a shorter path length to the surface contacts. It is important, however, to quantify the effects of grain size and crystallographic defects on τ and PV device efficiency to improve the accuracy of modeling grain size and defect level requirements for thin-layer silicon device structures with light trapping.

While a number of theoretical [1-5] and experimental [4, 6-12] studies of grain size effects on PV performance have been conducted, there is considerable variation in the findings. One reason for this may be that impurities and intragrain crystallographic defects often coexist with the grain boundary effects. In the present investigation, we attempt to eliminate impurity effects by using high-purity FZ growth procedures to generate lightly-doped (about 4 Ω-cm) Si ingots with varying grain sizes. The effect of grain size on τ was determined by measuring τ in various locations on wafers immersed in HF acid using a laser-excited, microwave photoconductive decay apparatus. Grain size was measured in the same locations. The effect of grain size on PV cell performance was determined by fabricating arrays of 0.04-cm^2 mesa-isolated diagnostic solar cells on the same wafers after a light Secco etch [13]. The total number of grains within each 2-mm x 2-mm cell was counted to arrive at an average grain area, and the PV performance characteristics of each cell were determined.

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EXPERIMENTAL

Growth of FZ ingots with a range of grain sizes was accomplished by initiating growth from a fine-grained, 22-mm-diameter seed cut along a diameter of a 100-mm-diameter, chemical vapor deposited (CVD), polycrystalline Si log (Fig. 1). Growth was carried out in a 99.9995% minimum purity argon atmosphere, and two zone passes were used to further purify the polycrystalline feed rods. As FZ growth progressed, the grains widened. Wafers cut at various positions along the ingot contained a range of grain sizes because of the increase of average grain size with ingot length and the tendency for grains near the periphery of the ingot to grow larger. Fig. 2 shows NaOH-etched wafers removed 4, 8, 16, and 32 mm from the seed, with corresponding average grain sizes of 0.16, 0.21, 0.58 and 0.83 mm as determined by counting the number of grain boundaries crossing a line of known length. Because grain size was not uniform and shapes were irregular,

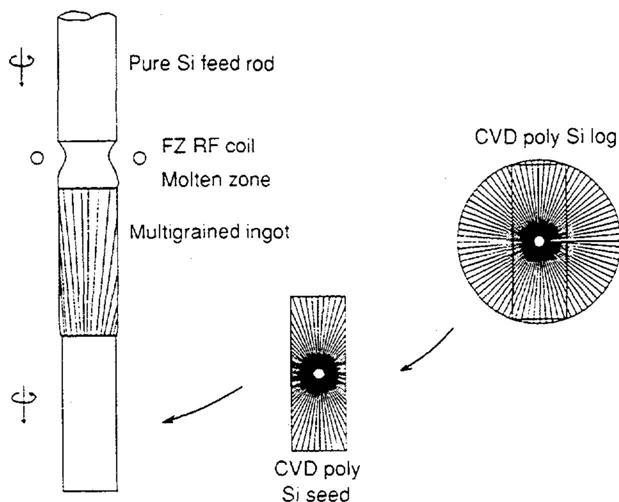

Fig. 1. Schematic of process for growing high-purity, multigrain silicon with various grain sizes.

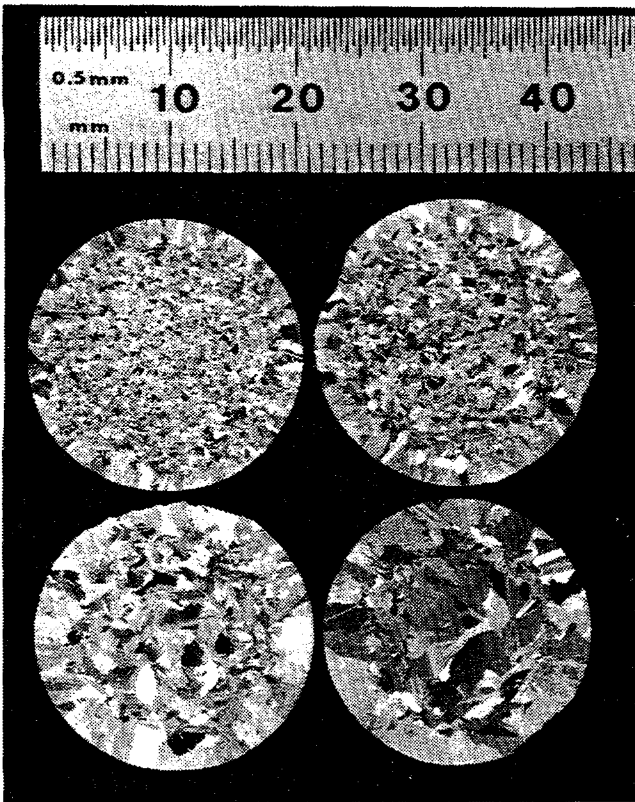

Fig. 2. Grain structure at (right to left and top to bottom) 4, 8, 16, and 32 mm from the seed attachment point.

we felt that a better measure of grain size would be obtained by counting the number of grains in a known area (ignoring straight boundaries that are obvious twins or stacking faults) and dividing that area by the number of grains to obtain an average grain area. The use of grain area here is also justified because most of the grains are axially columnar in the ingot, extending over the entire thickness of the wafer sample. This is the procedure used for the data to be presented subsequently.

Dislocation-free and dislocated single-crystal [100] and [111] ingots were also grown for comparison with the multicrystalline material. Dislocation densities ranged from 4 x 10^3 to 2 x 10^5 cm^{-2}. All ingots contained less than 0.3 ppma oxygen and less than 0.5 ppma carbon as measured by Fourier-transform infrared (FTIR) spectrometry. Gallium doping was used to obtain ~4 Ω-cm, p-type resistivity. Two different in situ ingot cooling rates were used, 18° and 89°C min^{-1}, to compare cooling rate effects on the PV cell efficiency and τ of multigrain wafers.

Before wafering the ingots, bulk lifetimes were measured by the American Society for Testing and Materials (ASTM) F28-75 (reapproved 1981) photoconductive decay method [14]. The dislocation-free control ingot had a 2,500 μs τ. Dislocated single-crystal bulk τ's ranged from 500 to 1000 μs, and the multigrained ingots exhibited 20 μs < τ < 100 μs.

After sawing and lapping to about 0.8 mm thickness, the wafers were etched in a HNO_3: 47% HF: glacial CH_3COOH mixed acid solution with composition 3:1:2 for 2.5 min. Then, they were heated in sulfuric acid for 1 hour at 200°C followed by H_2O rinsing and immersion in a 47% HF solution held in a thin, transparent, sealable τ measurement cell. The cell was placed in a LEO Giken Wafer-τ measurement apparatus. Pulsed illumination was provided by a 904-nm diode laser, and the change in photoconductivity was sensed by reflected 9.6 GHz microwaves. The surface recombination velocity s was determined to be approximately 50 cm s^{-1} for representative dislocation-free, dislocated, and multicrystalline samples by doing the wafer τ measurement at several different thicknesses and using the equation

$$1/\tau_e = 1/\tau + 2s/d \quad (1)$$

where τ_e is the effective or measured lifetime, τ is the true bulk lifetime, and d is the wafer thickness.

The same procedure was used for preparing wafers from the sample set. Effective τ_e values were measured at predetermined intervals along the diameter of each sample wafer and were corrected for s to arrive at sample τ values. The correction was typically negligible for the low τ_e values of most of the multicrystalline wafers. After lifetime measurements, the wafers were lapped and underwent a chemical-mechanical polish procedure with a colloidal silica slurry (both on one and the same side) to a thickness of 300 μm. A light (5 minutes) Secco etch was used to reveal grain boundaries and dislocations on the polished surface prior to diagnostic solar cell fabrication.

Junction diffusion was carried out at 850°C for 20 minutes using solid-source wafers and a special quartz holder to provide uniform n^+ layers in the p-type sample wafers. Photolithography was used to define Ti/Pd/Ag grids and an etched moat around each 2-mm x 2-mm (0.04 cm^2), mesa-isolated cell. Aluminum back contacts were used. No texturing, surface passivation, or antireflection (AR) coatings were used, so that the cell parameters would more closely reflect only the Si material variations (grain size and dislocation density). Also, by not using oxide surface passivation, we were able to maintain a relatively low maximum cell process temperature of 850°C. The cells made in this manner from the dislocation-free FZ control wafers had the following parameters measured under a Spectrolab XT10 solar simulator: open-circuit voltage V_{oc} = 0.533 V, short-circuit current density J_{sc} = 22.23 mA/cm^2, fill factor FF = 74.3%, and efficiency Eff = 8.8%. All measurements for the experimental cells were also made under the XT10 simulator and normalized to these values. After AR coating, the parameter values for a control cell (measured under standard test conditions with a Spectrolab X25 solar simulator) were as follows: V_{oc} = 0.545 V, J_{sc} = 31.32 mA/cm^2, FF = 78.4%, and Eff = 13.4%. These values were not used in the normalizations but are listed for additional information. We point out that the grid coverage for the mesa cell masks we used in this study is greater than 10%. This is not a major concern for our relative, normalized data analysis.

After cell fabrication, the number of grains in each characterized cell was counted, ignoring twins and stacking faults. The average grain area was determined by dividing the cell area (0.04 cm^2) by the number of grains. Counting was done on 40X photomicrographs of the mesa cells. One example is shown at the bottom of Fig. 3. At the top of Fig. 3, an electron-beam induced current (EBIC) image of the same mesa cell is shown. It provides justification, in most cases, for ignoring the straight twin and stacking fault boundaries since they are seen to generally be much less electrically active than the grain boundaries. Our earlier studies of grain boundaries in Si sheets

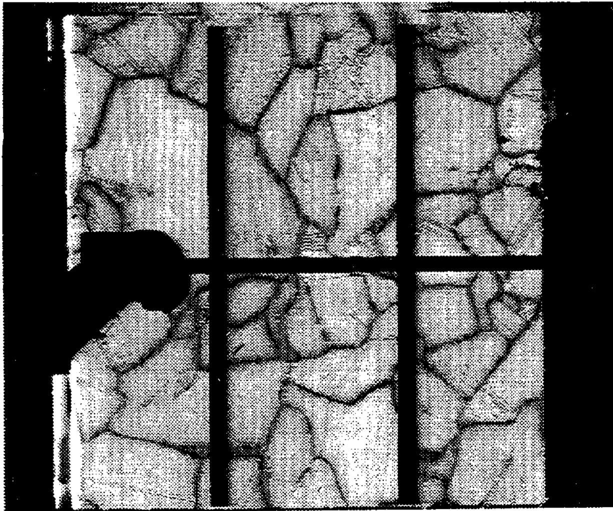

Fig. 3. Photomicrograph showing one 2-mm x 2-mm mesa cell out of a wafer-wide array of mesa cells on a sample wafer that was 6 mm from the poly seed end of an ingot cooled at 18°C min^{-1} (bottom) and an EBIC image of the same mesa cell (top).

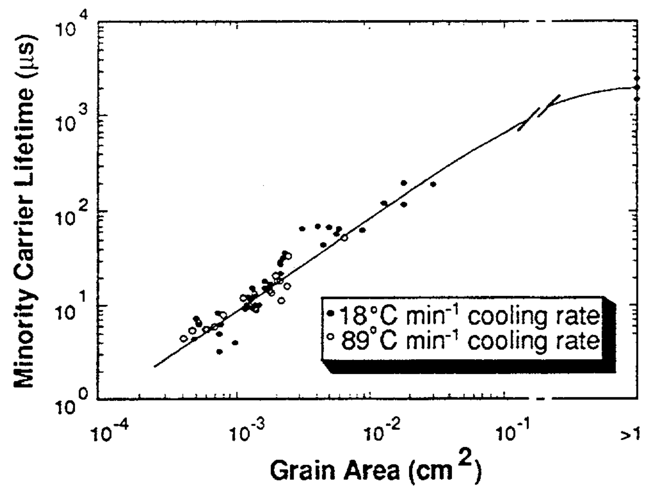

Fig. 4. Dependence of τ on average grain area in high-purity multicrystalline silicon.

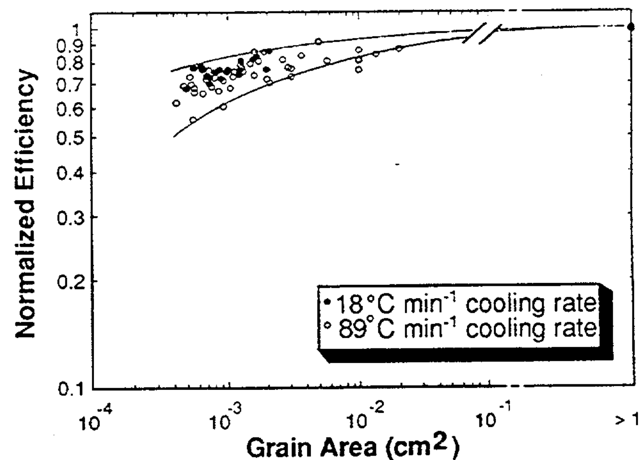

Fig. 5. Dependence of normalized cell efficiency on average grain area in high-purity multicrystalline silicon

[15, 16] also support this approach. Dislocation counting on the dislocated single-crystal cells was done under a microscope because the photomicrograph did not provide adequate resolution.

RESULTS AND DISCUSSION

Figure 4 shows the observed dependence of τ on grain area. Even for large grains (0.02 cm^2 area), τ is an order of magnitude lower (200 µs) than it is for dislocation-free single crystals (2000 µs). This indicates that, for large-grained (grain area larger than about 0.02 cm^2) material, τ is mostly determined by the intragrain dislocation density. Grain boundaries are not very detrimental when the average grain size is larger than the minority carrier diffusion length. On the log-log plot, a linear decrease of τ with grain area is seen from 200 µs at 0.02 cm^2 to 4 µs at 5×10^{-4} cm^2 grain area. There is considerable scatter in the data. However, it does not appear to be related to crystal cooling rate. More likely, it is related to variations in electrical activity of different grains and grain boundaries. The EBIC image of Fig. 3 (top) supports this postulate, since there are differences in contrast for different grain boundaries and even along the same grain boundary. In an EBIC image, dark regions are areas of enhanced charge-carrier recombination. In the τ measurement geometry, the grain boundaries could give rise to spatial mobility variations. But since the mobility is time-independent, τ_e should still reflect carrier recombination.

Over the same range of grain sizes, there is also a monotonic decrease in normalized (to the dislocation-free wafers) solar cell efficiency. The decrease of efficiency is about 40%. Again, there is considerable scatter to the data. Upper and lower bounds of the data range are drawn in the plot, which is shown in Fig. 5. Most of the decrease in normalized cell

efficiency with decreasing grain area is attributable to the decrease in normalized J_{sc} (about 21%), while contributions from the decrease in normalized FF (about 10%) and V_{oc} (about 9%) play smaller roles. The observed relative dependencies of J_{sc} and V_{oc} on grain area agree with theoretical analysis, e.g. [4], in that J_{sc} is expected to exhibit a stronger dependence on diffusion length L than V_{oc} does when L is less than the cell thickness. Most of the data scatter in Fig. 5 is attributable to fluctuations in FF and probably reflects the difficulty of adequately contacting the small grid pads during cell measurements.

There does appear to be an identifiable difference in normalized efficiency data for the slowly cooled (18°C min^{-1}) ingot. It appears to retain somewhat higher efficiency values with decrease in grain size, whereas the fast-cooled (89°C min^{-1}) ingot has cells that span both the high and low bounds of the data. While there are major differences in dislocation density from grain to grain and cell to cell, this was not seen to correlate with either ingot cooling rate or position of data within the bounds of Fig. 5.

On the other hand, we did see a trend of efficiency decrease with increasing dislocation density for the dislocated single-crystal wafers. The effect, shown in Fig. 6, was relatively

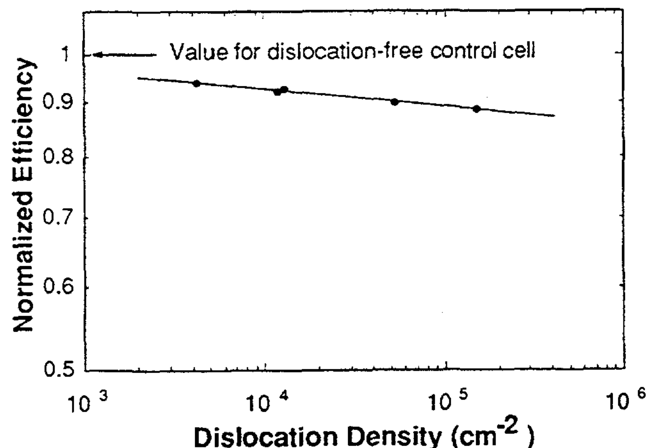

Fig. 6. Dependence of normalized cell eficiency on dislocation density in high-purity single-crystal silicon.

small - about a 12% drop in normalized efficiency at the largest dislocation densities of ~1.5×10^5 cm^{-2}. It is difficult to achieve much larger dislocation densities in FZ Si because a loss of crystal structure typically takes place at higher densities. It is also difficult to obtain grain areas smaller than 5×10^{-4} cm^2 by FZ growth (and most other ingot melt growth methods).

By combining the data from Figures 4 and 5, we can deduce the dependence of normalized efficiency on τ. The shaded region in Fig. 7 shows this dependence. The best fit curve for τ versus grain area and the two bounding curves for normalized cell efficiency versus grain area, were used to determine the shaded region in Fig. 7. The decrease of efficiency with τ is small for $\tau > 20$ µs (which corresponds to an L value on the order of cell thickness, 300 µm) but is substantial for $\tau < 10$ µs (which corresponds to an L value equal to about half the cell thickness).

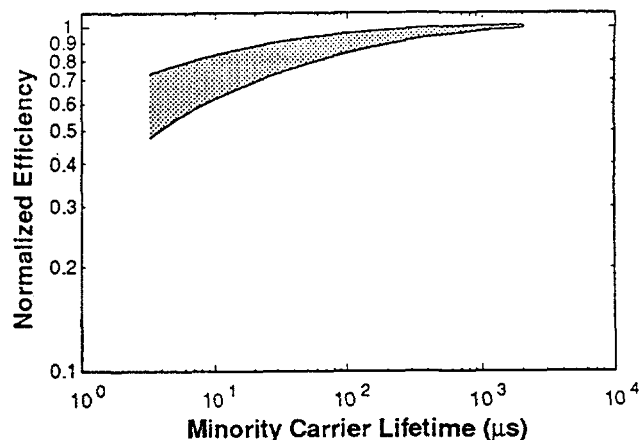

Fig. 7. Dependence of normalized cell efficiency on lifetime in high-purity silicon obtained by combining data from Figures 4 and 5.

SUMMARY AND CONCLUSIONS

We used high-purity FZ growth procedures and fine-grained silicon seeds cut from CVD-grown polycrystalline Si logs to generate Si ingots with varying grain sizes for a study of grain area effects on τ and PV cell efficiency in high-purity multicrystalline silicon. Dislocated and dislocation-free crystals were also grown for comparison. Lifetimes were measured on wafers cut from the ingots, and diagnostic arrays of mesa-isolated solar cells were fabricated and characterized. Correlations were made between average grain area, lifetime, single-crystal dislocation density, and solar cell characteristics. Our main findings were as follows:

(1) τ decreases with decreasing grain area from 200 µs at 2×10^{-2} cm^2 grain area to 4 µs at 5×10^{-4} cm^2 grain area in high-purity Si.

(2) Normalized solar cell efficiency decreases with decreasing grain area in high-purity Si and is about 60% of the value for dislocation-free wafers at 5×10^{-4} cm^2 grain area.

(3) Normalized solar cell efficiency monotonically decreases with decreasing τ in high-purity silicon. The value at 5 µs is about 60% of that at 10^3 µs. The decrease is small for τ greater than 20 µs.

(4) τ decreases with increasing dislocation density in single-crystal wafers and is about 88% of the value for dislocation-free wafers at 1.5×10^5 cm^{-2} dislocation density.

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Si THIN LAYER GROWTH FROM METAL SOLUTIONS ON SINGLE-CRYSTAL AND CAST METALLURGICAL-GRADE MULTICRYSTALLINE Si SUBSTRATES

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ABSTRACT

A simple, vertical-dipping, liquid-phase epitaxy (LPE) method for growth of Si layers from Cu/Si solution at temperatures less than 950°C has been shown to be a promising technique for thin crystalline Si photovoltaic (PV) applications. Solar cells with more than 15% AM1 efficiency were fabricated on 5-μm-thick layers grown from Cu/Si solution on (111) Czochralski (CZ) substrates. To extend the application of this technique to low-cost substrates, we grew thin (5-40 μm) Si layers on cast multicrystalline metallurgical-grade (MG) substrates from Cu/Si solution as well as from Al/Si, Al/Cu/Si, Bi/Si, Ga/Cu/Si, and Sn/Si solutions. The conditions of growth, morphology, solvent incorporation characteristics and problems that arise with the use of multicrystalline Si substrates are discussed. A diagnostic solar cell with efficiency equal to 0.42 and open-circuit voltage equal to 0.89 of the values for a single crystal control cell was obtained, without any light-trapping scheme, on a 15-μm-thick layer grown on a MG Si substrate.

INTRODUCTION

Thin layers of reasonably large-grain multicrystalline silicon offer an opportunity for Si PV device structures that utilize much less of the high-purity active silicon material than do conventional cells (5 to 50-μm thickness versus 100 to 400-μm thickness). Such cells are expected to have less stringent requirements on minority charge carrier lifetime τ or diffusion length L, because light-generated carriers have a shorter path length to the surfaces. Because of the limited optical absorption capability of silicon, multiple passes of light via textured surfaces and/or back surface reflection schemes will probably be required to absorb most of the incident photons with such thin active silicon layers. In this paper, we describe our use of liquid-phase epitaxy (LPE) or metal solution growth, especially growth from copper/silicon solutions, as a means of achieving thin Si layers for PV applications. Some PV device results using LPE growth on single-crystal and cast MG multicrystalline substrates are presented.

In previous publications [1-3], we detailed a number of reasons why Cu is an attractive candidate for metal solution growth or (LPE) growth of Si thin layers. These are summarized below:

(1) The high solvent power of copper for silicon (about 0.05 wt. % Si $^{\circ}C^{-1}$ near 940°C; this compares, for example, to about 0.007 wt. % Si $^{\circ}C^{-1}$ for tin solvent)

(2) Low growth temperature (typically 875°-950°C)

(3) Low solid solubility of Cu in Si (the solubility of Cu in Si at 900°C is 1×10^{17} atoms cm^{-3} compared to 1.5×10^{19} atoms cm^{-3} for Al, 2×10^{19} atoms cm^{-3} for Ga, and 4×10^{19} atoms cm^{-3} for Sn) [4]

(4) Minimal effect on Si resistivity because Cu isn't a doping element

(5) Minimal effect on PV efficiency at the expected Cu concentrations in the grown layers (according to Davis et al.[5], 1×10^{17} atoms cm^{-3} Cu content is required for solar cell degradation)

(6) Demonstrated ability of Cu/Si alloy to retain impurities when used to purify silicon by electro-winning[6], CVD bulk growth[7], or bulk melt refining[8].

Although growth of thin Si layers from Cu/Si solution on single-crystal (111) substrates is relatively straightforward, some new problems arise with the use of cast multicrystalline MG Si substrates. These include: (1) rough surfaces from growth rate differences of various grain orientations, (2) possible impurity contamination from the MG substrates, (3) solvent sticking to the grain boundaries (but not the twin boundaries) because of enhanced dissolution at the boundaries when the substrate is subjected to partial melt back for surface native oxide removal, and (4) electrical properties associated with dopant incorporation and grain size effects. Some success in dealing with these problems has been made, and we report the current status of the work in this paper.

THIN-LAYER SINGLE-CRYSTAL LPE GROWTH

We used an induction-heated vertical graphite hot zone and a vertical dipping technique to conduct LPE growth. Details of the experimental arrangement were described previously [2,3]. A 100-mm-diameter quartz tube serves as the chamber enclosure, and the induction heating coil is external to the chamber. The graphite hot zone components are heated by induction from a 360-kHz radio frequency (RF) generator and are arranged to

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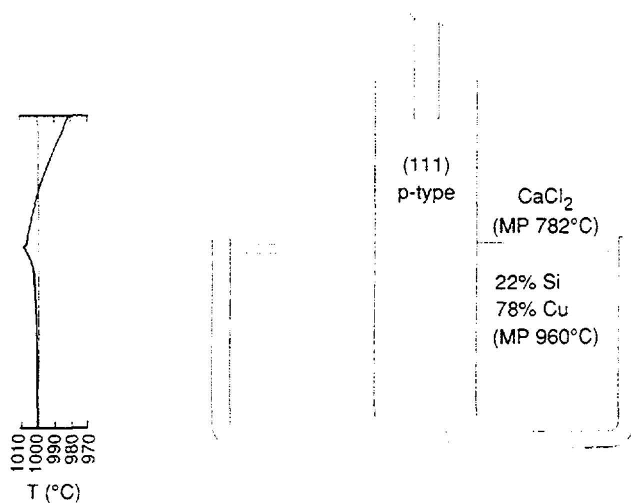


Fig. 1. The crucible region and a corresponding vertical axial temperature profile at a temperature somewhat above the growth temperature.

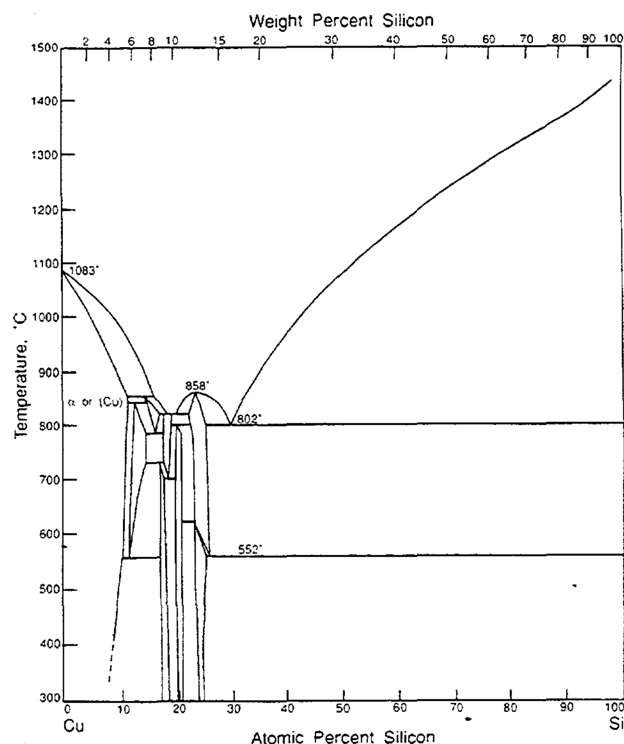


Fig. 2. Phase diagram of the Cu-Si system

provide nearly isothermal conditions in the solution, but with the top of the solution slightly hotter than the bottom as shown in Fig. 1. Crucibles were made of either quartz or high-density graphite. In some cases, a 99.995%-pure $CaCl_2$ liquid layer was used over the metal/silicon solution. Although not necessary to the growth process, the $CaCl_2$ layer seems to help stabilize the temperature near the solution surface and provide a gettering role for surface oxides. The apparatus has an open pull port that also serves as the exit path for 99.9995%-pure argon gas that is continuously purged through the growth system. Our second growth system is similar to the one just described, but it has a water-cooled metal chamber with an internal 10kHz induction coil and a more massive hot zone.

Our work with single-crystal substrates was conducted primarily in the Cu/Si solvent system, although some growth from tin, gallium, and copper/gallium solutions was also carried out for comparison. The Cu/Si phase diagram (see Fig. 2) offers a wide temperature range for solution growth at compositions containing more than 30 at.% Si. Growth basically proceeds by saturating Cu with Si at some temperature above the 802°C eutectic temperature, elevating the temperature slightly, immersing the substrate, ramping the temperature downward a predetermined amount at a slow controlled rate, and finally removing the substrate and grown layer from the solution. We used solutions composed of 18-22 wt. % Si in Cu, and operating temperatures between 870°C and 960°C. We also conducted single-crystal Si LPE growth from 9 wt. % Si solutions in Ga at a hot-zone temperature near 1030°C, and 1.6-2.3 wt. % Si solutions in Sn at hot-zone temperatures above 1100°C.

After melting the Cu and Si to form a liquid solution (sometimes capped with liquid $CaCl_2$), the substrate is lowered through the open pull port, thermally equilibrated above the solution, and then immersed. The temperature of the solution is gradually reduced, under computer control, approximately as shown in Fig. 3. Partial substrate dissolution and native oxide removal occurs first, and then new thin-layer growth begins. After growth, the substrate is withdrawn through the pull port, and a new substrate is positioned for growth. The laminarly

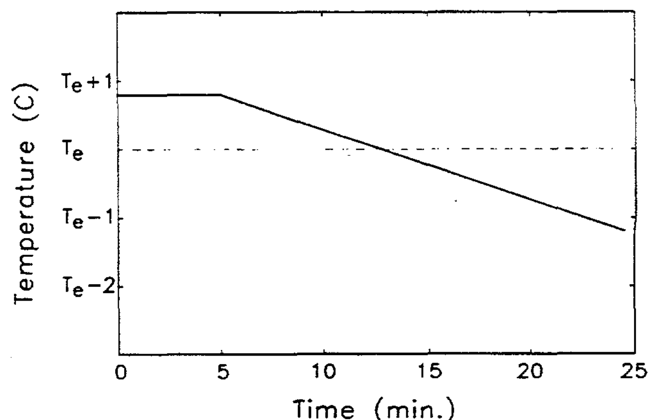


Fig. 3. Typical cooling profile for Si thin layer growth from Cu/Si solution. T_e is the equilibrium temperature at which neither growth nor dissolution occurs.

purged open pull port allows many substrates to be coated sequentially. We used procedures for single-crystal growth from Ga or Sn solutions essentially similar to those we use for growth from Cu solutions. A number of other studies of Si growth from Ga or Sn solutions have been reported, including those in [9,10], and therefore we did not put extensive effort into growth from these systems. LPE growth [11] and characterization [12] of Si from In solution for PV use have also been reported recently.

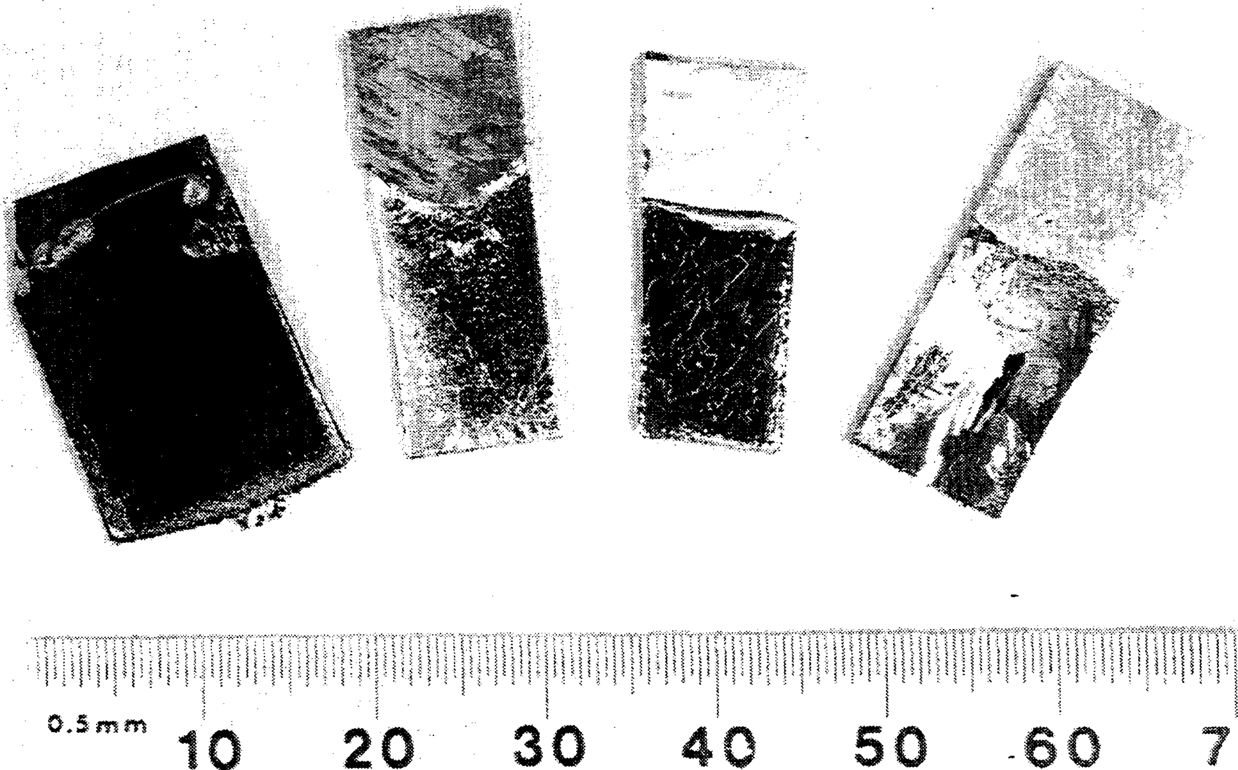


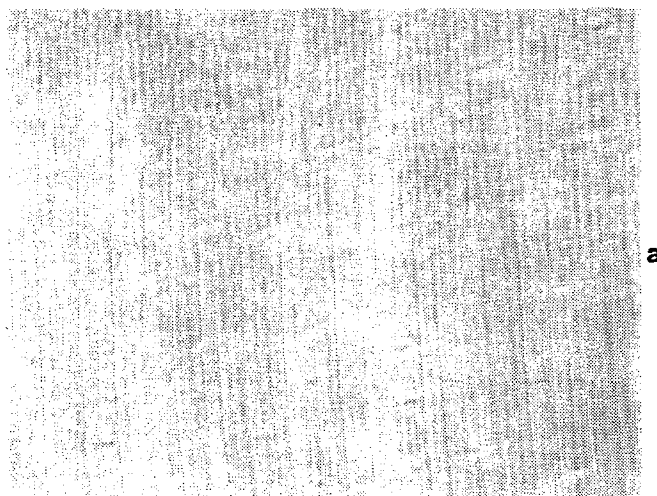
Fig. 4. Examples of thin-layer Si growth by LPE (from left to right: (111) single crystal growth from Cu/Si solution; growth on cast MG Si from Cu/Si solution; growth on cast MG Si from Al/Si solution; growth on cast MG Si from Sn/Si solution)

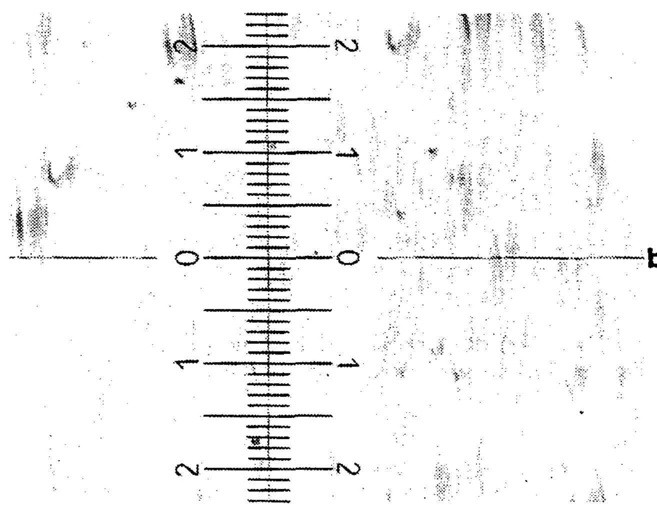
Characteristics of Single Crystal LPE Si Layers

Smooth layer growth is favored by slower cooling rates (using longer times if necessary to achieve thick layers). Cooling rates less than 0.1°C min^{-1} and corresponding growth rates less than approximately 1 μm min^{-1} appear to be sufficient. Uniform, smooth, single-crystal films as large as 4 cm^2 with thicknesses between 1 and 50 μm have been grown from Cu solution on (111) substrates (an example is shown at left, Fig. 4). The surface morphologies, as viewed by Normarski differential interference contrast (DIC) microscopy, of LPE Si layers grown under several different conditions are shown in Figue 5. At 0.01°C min^{-1} cooling rates, quite smooth thin layers are obtained as shown in Fig. 5a. The surface lines are due to slip/stick motion of the solution meniscus when the grown layer is slowly withdrawn from the solution. A thicker (25 μm) layer grown at 0.02°C min^{-1} from Cu/Ga/Si solution exhibits only slightly more topography (Fig. 5b). This layer was grown without any partial dissolution of the substrate. It is also possible to grow textured, near-(111) single-crystal epitaxial Si layers by performing growth at a more rapid cooling rate of 0.2°C min^{-1} on slightly misoriented substrates (Fig. 5c), but significantly faster rates will lead to morphological roughening of the grown layer with concomitant solvent entrapment.

Rapid cooling (faster than about 0.2°C min^{-1}) or poor temperature control (fluctuations greater than 0.1°C) can lead to solution entrapment and inclusions in the grown layer, as we reported earlier [1]. In the Cu/Si growth system, the solution inclusions are cupro-silicon alloys as determined by qualitative scanning electron microscopy (SEM) analysis. The amounts of Si and Cu vary. Such inclusions are difficult to remove from the grown layer because they are not easily affected by acids other than HF/HNO_3 mixtures that would also attack the silicon. We grew some single-crystal Si layers on (111) CZ substrates from Ga/Si and Sn/Si solvents using generally the same procedures as used for growth from Cu/Si solution to study inclusions. We found that solution entrapment and inclusion formation is similar in all three systems if the cooling rate exceeds about 0.2°C min^{-1}, or the growth rate exceeds several μm min^{-1} at the growth temperatures used [3]. An example of solution entrapment in a Si LPE layer grown from Ga/Si is shown in the photomicrograph of Fig. 6.

Inclusion-free Si layers (like those shown in Fig. 5) grown from Cu/Si solution have a very low bulk Cu content, $< 1 \times 10^{16}$ atoms cm^{-3}, as measured by secondary ion mass spectroscopy (SIMS) depth profiling. This is an order of magnitude less than the level that would cause cell degradation[5]. Whole wafer epitaxy is easily achieved. Stacking fault densities in the grown layers are on the order of 1×10^2 to 2×10^4 cm^{-2}. They are sometimes visible on the as-grown layer as shown in Fig. 5b, or they can be revealed by brief (5 s) mixed-acid etching and can be used to geometrically determine the film thickness, because they are usually point nucleated at the substrate interface (film thickness = $(2/3)^{1/2}a$, where a is the length of the stacking fault at the film surface). This equation is only true for layers grown on (111) substrates.





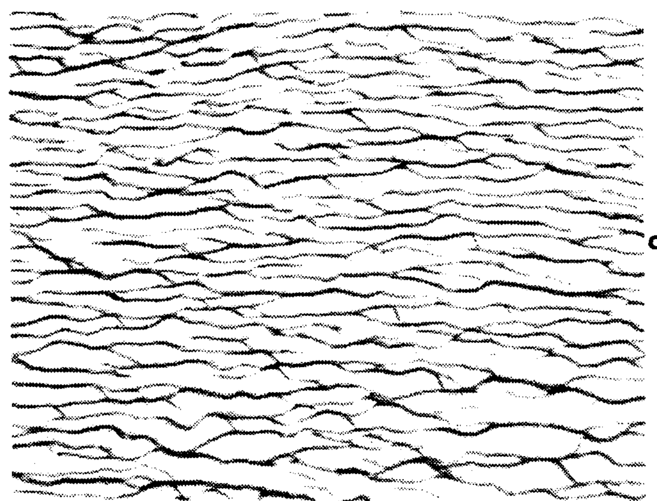


Fig. 5. LPE layers grown at different cooling rates and thicknesses on near-(111) CZ substrates: (a) 0.01°C min^{-1} and 5 μm thick from 20 wt. % Si/80 wt. % Cu solution; (b) 0.02°C min^{-1} and 25 μm thick from 10 wt. % Si/50 wt. % Cu/40 wt. % Ga solution; (c) 0.2°C min^{-1} and 20 μm thick from 22 wt. % Si/78 wt. % Cu solution. The Normarski photomicrograph width is 1.5 mm.

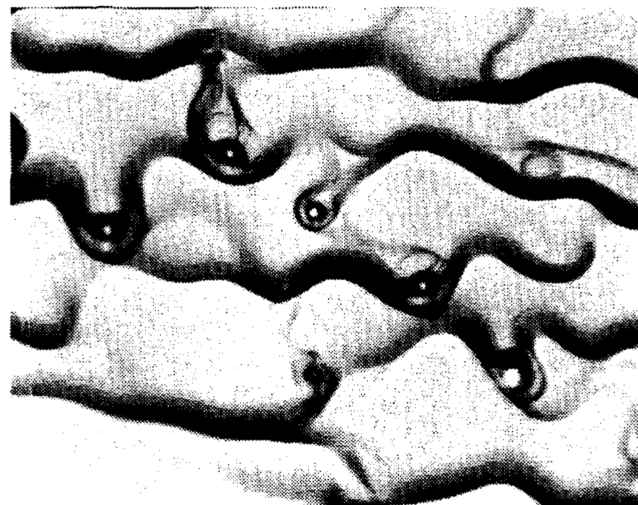


Fig. 6. Normarski DIC photomicrograph showing solvent inclusions in an Si layer grown from Ga/Si solution. The maximum photo dimension is 0.6 mm.

Solar Cells on LPE Layers Grown on Single-Crystal Substrates

A potential application of LPE-grown silicon is for PV devices. To test whether Si layer growth from Cu solution has a significant degradation effect on solar cells, we fabricated 1 cm^2 n^+-on-p cells on two samples. One was a commercial (111) p-type CZ control wafer; the other was a CZ wafer from the same lot with an ~ 5-μm-thick Si layer grown from Cu solution. Conventional phosphorus diffusion from a solid source was used to form the n^+ junctions in both cases. Both cells had antireflection coatings. The current-voltage curves, areas, short-circuit current densities (J_{sc}), open-circuit voltages (V_{oc}), fill factors (FF), and efficiencies (Eff) for the two cells are shown in Fig. 7. Growth of the thin silicon layer did not have an appreciable degradation effect on the cell performance, because the cell fabricated on solution grown material had an efficiency about 97% of that for the control cell (15.3% and 15.7%, respectively). PC-1D [13] cell modeling showed (see Fig. 8) that the diffusion length of the 5 μm LPE layer must be at least 50 μm for the overall cell performance to degrade less than 0.5% absolute. A minority-carrier diffusion length of 109 μm was measured on the finished device, and this is consistent with the modeling results.

If Cu-Si alloy solution inclusions are incorporated in the grown layer, PV performance degrades significantly. Arrays of 2-mm by 2-mm diagnostic n^+-on-p solar cells (without back-surface fields, passivation, or antireflection coatings) were fabricated on Cu solution-grown Si layers with low (~ 8 cm^{-2}) and high (~ 110 cm^{-2}) Cu-Si inclusion densities. In these cases, the efficiencies were 80% and 37% as large as those of the CZ control cell. Partial shorting of the n^+-p junction by Cu-Si inclusions is the likely degradation mechanism, and the importance of conducting growth in a fashion that prevents inclusions (or having a means of removing them after growth) is evident. We tried a variety of acid systems in a search for one that would preferentially remove Cu/Si without attacking LPE Si. So far, none has been found. However, it is relatively easy to avoid the inclusions by using proper growth conditions.

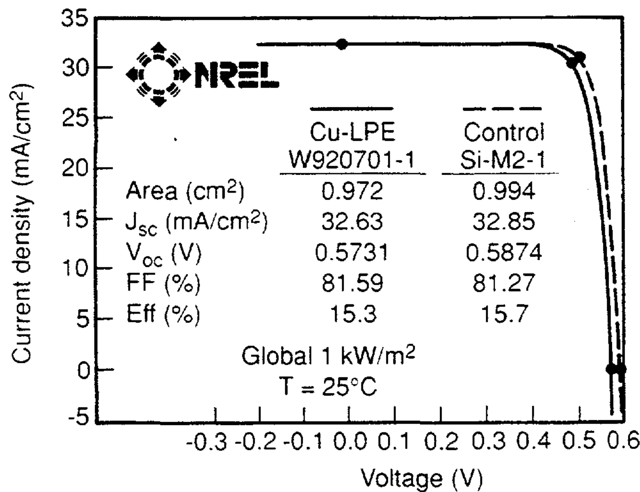


Fig. 7. PV cell data for a CZ-grown control cell and for a cell with an ~ 5-μm-thick Si layer grown by LPE from Cu solution on a CZ wafer.

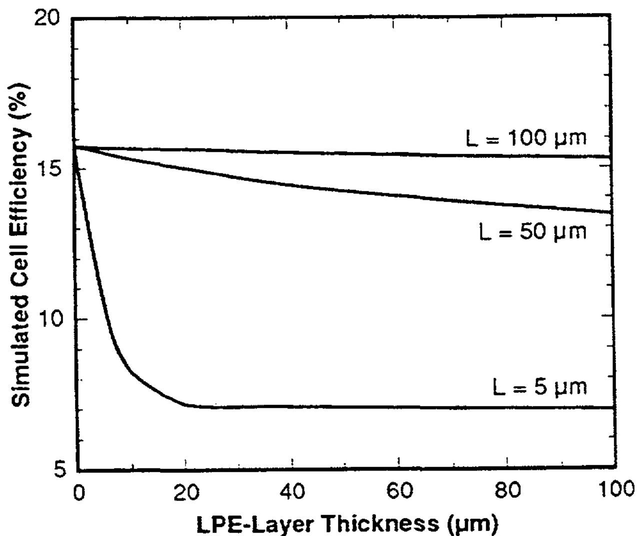


Fig. 8. Simulated cell efficiency versus LPE-layer thickness for different hypothetical LPE-layer diffusion lengths, L, with an assumed substrate diffusion length of 250 μm and a total cell thickness of 300 μm

LPE GROWTH ON CAST MG-Si MULTICRYSTALLINE SUBSTRATES

We acid-cleaned pieces of arc-furnace MG silicon, melted them in a quartz crucible, and cast them into 100-mm-diameter ingots. The ingots were wafered, and smaller segments cut from the wafers were lapped and degreased for use as LPE substrates. An ingot cross section, NaOH-etched to show grain morphology, is shown in Fig. 9. These multicrystalline substrates generally have grains about 100 μm to several mm in width. Growth procedures with cast MG substrates were generally similar to those for single crystal substrates.

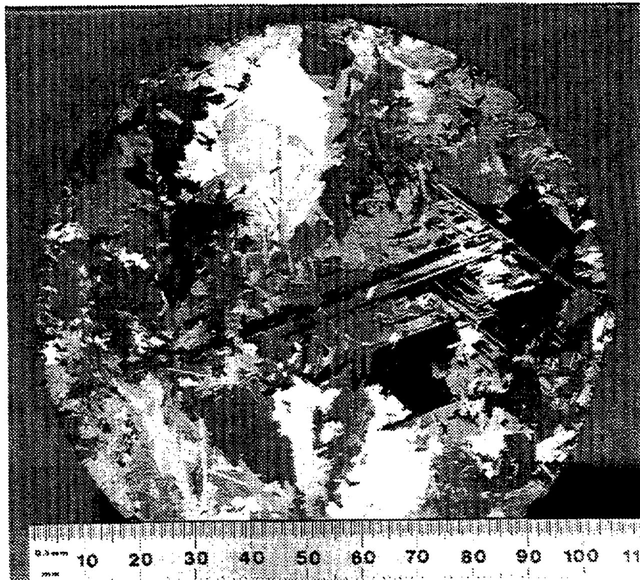


Fig. 9. NaOH-etched cross section of a cast MG Si ingot

LPE Growth on Cast MG Si from Cu/Si Solution

A Cu/Si solution consisting of 18 wt. % electronic grade Si in 99.9995%-pure Cu was maintained at about 870°C by computer control with a stability better than 0.1°C. After a substrate was dipped into the solution for 5 minutes, the temperature was ramped down with various rates for a total temperature drop of 2° to 3°C.

We found that grain surfaces of different orientations have similar growth rates at very slow cooling rates (<0.02°C min^{-1}). Thus a uniform growth thickness was achieved, although the surface morphology is different from grain to grain when the film is thick (> 10 μm)– especially for higher growth rates. Fig. 4 (second from left) shows a thin Si layer grown on cast MG Si from Cu/Si solution.

Partial substrate dissolution is mostly responsible for impurities entering the solution, because high purity starting materials were used for the crucible charge. However, partial dissolution is presently helpful to remove the native oxides on the substrate surface. Nevertheless, the ability of the Cu/Si alloy to retain impurities by melt refining makes it possible to grow high-purity, thin-layer Si on these low purity substrates. SIMS analysis (Fig.10) indicates that the detrimental impurities Fe, Ti, V, Cr, Al, and Cu are below SIMS detection limits in the bulk of the film. The detection limits are governed by background noise levels that are on the order of 2×10^{16} cm^{-3} but vary with each element. They are distinguished from sample signals by noting their response to a change of the aperature. At 5×10^{17} cm^{-3}, the boron concentration is somewhat high although the solution was not intentionally B-doped. The resultant resistivity of the film is in a range of 0.05 to 0.1 Ω-cm, measured by the three-probe voltage breakdown method. Spreading resistance measurement shows that the resistivity increases through the film thickness from the substrate to the top film surface, which is an indication that boron is gradually depleted in the melt.

Fig 10. SIMS data for a LPE Si film grown on a MG Si substrate from Cu/Si solution with partial substrate dissolution. Fe, Al, Cu, Cr, V, and Ti concentrations are all below background noise levels.

<u>LPE Growth on Cast MG Si from Other Metal Solvents</u>

Solvent entrapment in the grain boundaries seems to be caused by preferential excessive dissolution along grain boundaries during initial substrate partial dissolution. This creates deep trenches that later trap the solution. We tried several other solvent systems and saw similar solution trapping behavior. Examples of growth from Al/Si and Sn/Si solutions are included in Fig. 4. A magnified view of a layer grown from Al/32.5 wt. % Si is shown in Fig. 11. Smooth or rippled growth is seen on various grain orientations, but some portions of the grain boundaries show as thick dark lines due to an accumulation of Al/Si solution. Differences in Al/Si accumulation may be related to the relative orientations of the adjacent grains. The morphology for growth on cast MG Si from Cu/Si solution is very similar. Al/Cu/Si solution gives the smoothest growth with the fewest inclusions in the Si films grown on cast MG-Si multigrained substrates of the solvents we have tried so far. We have been able to remove trapped Al- and Sn-based solutions by acid etching. A problem with growth from Al/Si solutions is heavy Al contamination in the LPE layers. SIMS analysis showed greater than 10^{19} Al in the grown layers. The

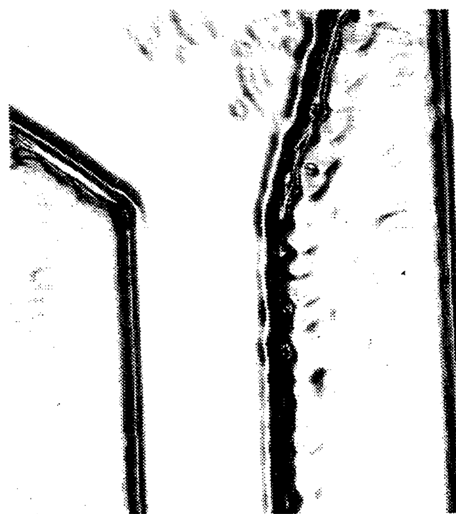


Fig. 11. Photomicrograph (Normarski DIC) showing surface morphology of an as-grown Si film on a cast MG Si substrate from Al/Si solution. A 2-mm-wide region is shown.

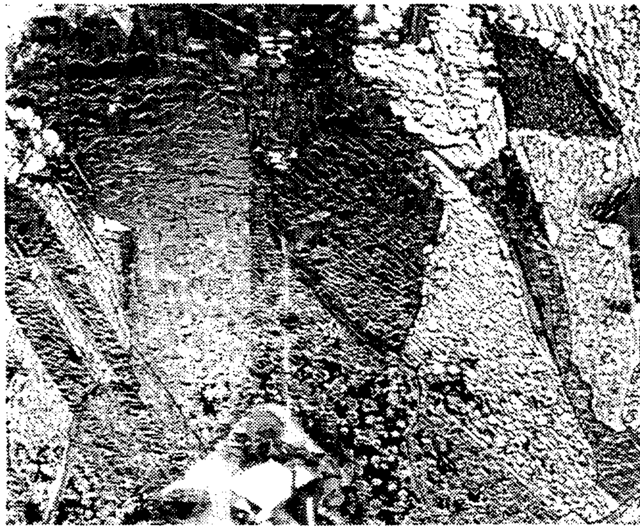


Fig. 12. Surface morphology of a Si film grown on a cast MG Si substrate from Sn/Si solution. An 8-mm-wide region is shown.

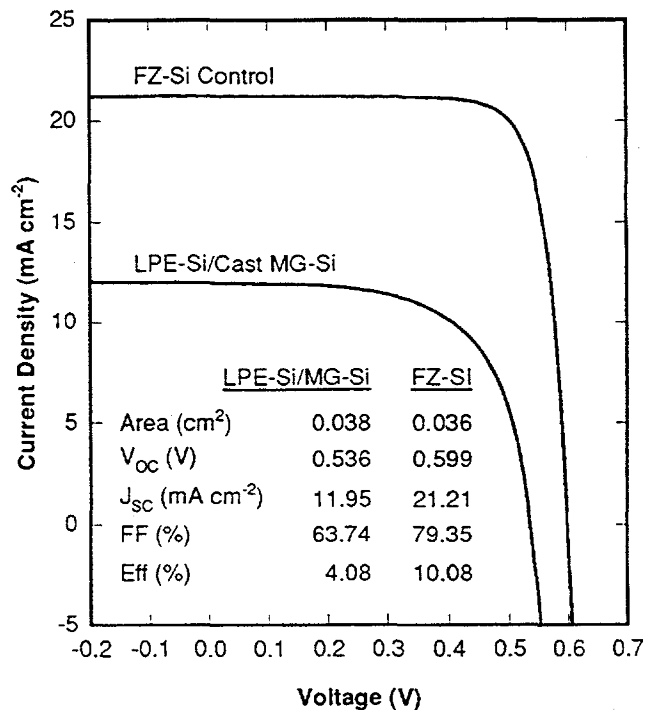


Fig. 13. Current-voltage curve and characteristics of a 2-mm × 2-mm solar cell in an LPE layer grown on a cast MG Si substrate from Al/32.5 wt. % Si solution. The active LPE layer thickness is ~ 15 µm, and the FZ control cell thickness is 250 µm.

corresponding 0.01 Ω-cm resistivity is not optimal for conventional solar cell structures.

Growth from Sn/1-2 wt. % Si solutions on cast MG substrates at 0.2°C min^{-1} cooling rate above 1100°C is interesting because there is a strong tendency for the surface of the growth on each grain to consist of (111) platelets (see Fig. 12). Because the grains are randomly oriented, the various tilts of the (111) planes provide a surface texturing effect, and the grown layer looks much like a NaOH-etched wafer from cast silicon ingots. However, Sn was incorporated at a level of ~ 5×10^{19} and other metals (Fe, Al, Ti) were detected at detrimental levels in the films.

It may be possible to avoid the solution entrapment along grain boundaries if other methods can be used to remove native oxides so that growth without dissolution can be used. A Bi/1-wt%-Si solution was tried for this purpose. Thin (a few µm), very uniform films were grown on single-crystal substrates without partial dissolution. But the film thickness was limited by the small solute (Si) content, even though growth was conducted over the large temperature range of 700°-350°C, and we did not pursue the Bi/Si system for growth on low-cost substrates. The Ga/Cu/Si and Al/Cu/Si systems yielded fast and inclusion-free layer growth on single-crystal substrates without partial substrate dissolution, but smooth growth without dissolution on cast MG Si substrates has not yet been achieved. This may be partially due to the rougher surface finish of the MG Si substrates.

Solar Cells on LPE Layers Grown on Cast MG Si Substrates

We have only made one attempt, so far, to fabricate diagnostic solar cells from LPE layers grown on cast MG Si substrates. The batch included layers grown from Cu, Al, and Sn solution. Inadequate solution removal (especially for the Cu/Si-grown layers) and rough film surfaces (especially for the Sn/Si-grown layers) precluded most cells from having good characteristics. Despite the heavy p-type doping associated with growth from Al/Si solution, we were able to obtain a functioning device. An array of small (0.038 cm^2) solar cells was fabricated on the ~ 15-µm-thick LPE layer after n^+ junction diffusion using $POCl_3$. The diffusion was not optimized for the low LPE layer resistivity, and no light trapping schemes were employed. No passivation, grid optimization, or antireflection coatings were used.

The total-area AM1 characteristics of the best cell we obtained are tabulated in Fig. 13, along with the current versus voltage curve. The same parameters are also shown for a float-zoned (FZ) Si control wafer processed along with the LPE film. An efficiency equal to 0.42 and V_{oc} equal to 0.89 of the values for the single-crystal FZ control cell were obtained. The Losses were mainly in J_{sc} and fill factor. The relatively good V_{oc} implies that the basic LPE material quality may be useful for PV devices. The loss in J_{sc} may be largely caused by the limited thickness of the active layer, and possibly would be improved by the use of multiple light pass geometries and/or increased layer thickness (up to 50 µm).

Cells made on Sn/Si-grown layers performed very poorly, probably because of the relatively high residual metal content in the LPE layers. Also, the rough texture may have allowed some substrate regions to remain uncoated with LPE silicon.

Cells made on layers grown from Cu/Si solution have higher J_{sc} (14 mA cm^{-2}), possibly because the doping is more appropriate (10^{17} cm^{-3}). But because Cu/Si alloys are difficult to remove with acids, the solution trapped in the grain boundaries probably caused the low observed Voc's (~0.21 V). We believe that this can be improved by further progress in the growth technique which will eliminate the dissolution step. Further work on both the LPE material, and the cell fabrication procedures are needed to make an assessment of this PV approach.

SUMMARY AND CONCLUSIONS

We have described LPE growth of thin Si layers from a number of metal solvent systems on both single-crystal (111) and cast MG multicrystalline substrates. Copper has been successfully used as a solvent for solution growth of 1-50-μm-thick, single-crystal silicon on (111) substrates of up to 4-cm^2 total area and has many favorable features for use as a solvent. The amount of copper incorporated in the LPE films is $< 1 \times 10^{16}$ atoms cm^{-3} and, at this level, is not expected [5] to interfere with solar cell performance. This was verified by fabricating PV devices on ~ 5-μm-thick Si layers grown on single crystal substrates. A cell efficiency of 15% absolute or 97% of that from CZ control cells was obtained. A diffusion length of 109 μm was measured on the finished cell, implying a diffusion length in the LPE layer longer than 50 μm. Thus, it appears feasible that practical PV devices may eventually be attainable with Si films grown from Cu solution, without a need for high-temperature (1430°C) recrystallization.

However, Cu-Si precipitates or inclusions may be present, especially in thicker films. Adequate thermal control (± 0.1°C) is needed to avoid them. Growth rates < 1 μm min^{-1} appear to be sufficient for inclusion-free growth. Si layers grown from Ga and Sn solution also exhibited similar solution inclusions. When potentially low-cost multicrystalline substrates are used, solution entrapment along grain boundaries can be problematic. A number of approaches were described to address this problem. We demonstrated a diagnostic solar cell with efficiency equal to 0.42 and open-circuit voltage equal to 0.89 of the values for a single-crystal control cell, without any light-trapping scheme, on a 15-μm-thick layer grown on a MG Si substrate. Cost-effective substrates and good control over solution incorporation are necessary for effective use of LPE technology for PV applications.

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§§§

VALIDATION OF AN IN-LINE EVAPORATION PROCESS FOR LARGE-SCALE PRODUCTION OF $CuInSe_2$-BASED SOLAR CELLS

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ABSTRACT

The validation of an in-line manufacturing process for the fabrication of $CuInSe_2$-based solar cells (including the quaternary $Cu[In,Ga]Se_2$) has been demonstrated. The validation involves a fixed substrate (molybdenum-coated soda-lime glass) onto which the deposition of the compound is achieved via a method of variable metal fluxes. These variable metal fluxes in nature emulate the fluxes as seen by a mobile substrate in an in-line two (or three)-source coevaporation system that evaporates the metals at a constant rate/flux.

The importance of this in-line approach is based on its feasibility for large-area depositions and its efficient utilization of materials. These intrinsic advantages could have a great impact in the large-scale production of photovoltaic modules for terrestrial or space applications.

The objectives of the present study are (1) to determine which geometrical configuration of the in-line system yields the best device-quality materials and, (2) demonstrate that such a system can produce device-quality absorber materials that can be used for the fabrication of solar cells with efficiencies exceeding 10%.

Polycrystalline thin films obtained by this approach have been characterized by electron probe for microanalysis (EPMA) and electron microscopy (SEM). Solar cells have been characterized by I-V and external quantum efficiency curves (QE).

INTRODUCTION

Fabrication of $CuInSe_2$ (CIS) absorbers in large-scale is an essential issue for the advancement of this technology for both terrestrial and future space applications. This paper explores physical vapor deposition (PVD) as a viable technique for the large-scale production of CIS-based absorbers that can be used to make solar cells with state-of-the-art conversion efficiencies.

In the laboratory, small-area CIS-based photocells have achieved total area efficiencies close to 14%, and several potential large-scale manufacturing growth techniques are currently under investigation. Selenization via H_2Se gas [1] has already shown the potential of producing devices with efficiencies exceeding 10%, but the usage of the highly toxic H_2Se gas makes this technique less desirable. Selenization via selenium vapor [2,3] looks more attractive from a safety point of view but the technique still has to prove the capability of producing devices with efficiencies exceeding 10%. Reactive co-sputtering from planar metal targets in an $Ar+H_2Se$ atmosphere has been demonstrated [4] and devices with 4% efficiency were obtained. In this approach, one of the main problems was the contamination of the targets due to the reactive nature of the working gas.

The idea of an in-line co-evaporation system is not new [5,6]. Our intentions in this paper are (a) to expand this concept to $Cu[In,Ga]Se_2$ (CIGS) absorbers; (b) to give details on the design parameters for both systems (CIS and CIGS); and (c) to find the optimum physical configuration that will yield the best device-quality materials. This will be done through the emulation of a moving substrate coated from two or three metal sources evaporating at a constant rate.

BACKGROUND: THREE-SOURCE EVAPORATION IN-LINE SYSTEM

The first two evaporation sources are separated by a distance "d" from each other, and at a distance "h" from the substrate; the third source is at a distance "n*d" from the first one, and at a distance "k" from the substrate (see Fig. 1). Our design of the in-line evaporation system involves a substrate moving in the X direction (from x_0 to x_1) at a constant speed. The size/length of the substrate aperture is given by x_1-x_0. The following calculations will yield an expression for the spatial distribution of the deposited materials along the X-axis (substrate location), e.g., the distribution the substrate will "see" as it moves along the X-axis.

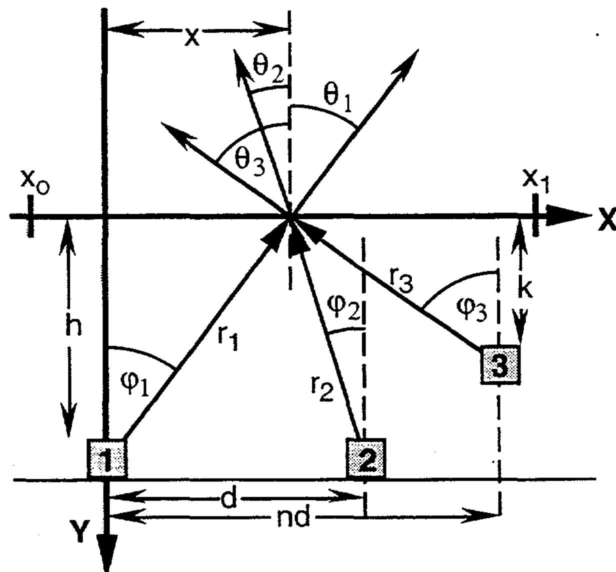

Fig.1. Schematics of the In-Line System

The infinitesimal mass deposited per unit area [7] of each source is given by

$$dM_1/dA=(M_{e1}/\pi*r_1^2)*\cos\varphi_1*\cos\theta_1 \quad (1)$$

$$dM_2/dA=(M_{e2}/\pi*r_2^2)*\cos\varphi_2*\cos\theta_2 \quad (2)$$

$$dM_3/dA=(M_{e3}/\pi*r_3^2)*\cos\varphi_3*\cos\theta_3 \quad (3)$$

where M_{e1}, M_{e2} and M_{e3} are the total masses of evaporated materials 1, 2 and 3.
Because the substrate surface is parallel to the evaporating surfaces we have

$$\varphi_1=\theta_1 \quad \varphi_2=\theta_2 \text{ and } \varphi_3=\theta_3 \quad (4)$$

From the geometry of the in-line system we have

$$\cos\varphi_1=\cos\theta_1=h/r_1 \quad (5)$$

$$\cos\varphi_2=\cos\theta_2=h/r_2 \quad (6)$$

$$\cos\varphi_3=\cos\theta_3=k/r_3 \quad (7)$$

Also,

$$r_1^2=h^2+x^2 \quad (8)$$

$$r_2^2=h^2+(d-x)^2 \quad (9)$$

$$r_3^2=k^2+(n*d-x)^2 \quad (10)$$

With (1) to (10) we obtain

$$dM_1/dA=M_{e1}*h^2/\{\pi*(h^2+x^2)^2\} \quad (11)$$

$$dM_2/dA=M_{e2}*h^2/\{\pi*[h^2+(d-x)^2]^2\} \quad (12)$$

$$dM_3/dA=M_{e3}*k^2/\{\pi*[k^2+(n*d-x)^2]^2\} \quad (13)$$

These last three equations represent the spatial distribution of the evaporants from three independent sources. The shape of the different curves is determined by the design parameters "d" "h" "k" "n", and on the values of M_{e1}, M_{e2}, and M_{e3}. As an illustrative example, Fig. 2 shows the generic shapes of these curves for given values of the design parameters "d" "h" "k", and "n", along with the experimental substrate temperature profile. The values of "x_0" and "x_1" for this graph were taken as -16 and +20, respectively, and M_{e1}:M_{e2}:M_{e3}=1:0.25:0.75. The (-) and (+) signs stem from the chosen set of X-Y axis in Fig. 1. It should be noted that these curves are indeed the so-called "cosine" distributions of ideal evaporation point sources, where the peak of each curve indicates the relative position of that source. The integral of equations (11), (12) and (13) from x_0 to x_1 represent the total amounts of materials evaporated onto the substrate. In Fig. 2, material 1 is Cu, material 2 is Ga and material 3 is In. The flux for Se is not shown in Fig. 2, but for our experimental runs, we have set it to three times the flux of Cu-plus-In-plus-Ga at any time with a minimum rate of 10 Å/s. This value ensures enough of a Se over pressure for the formation reaction of the compound.

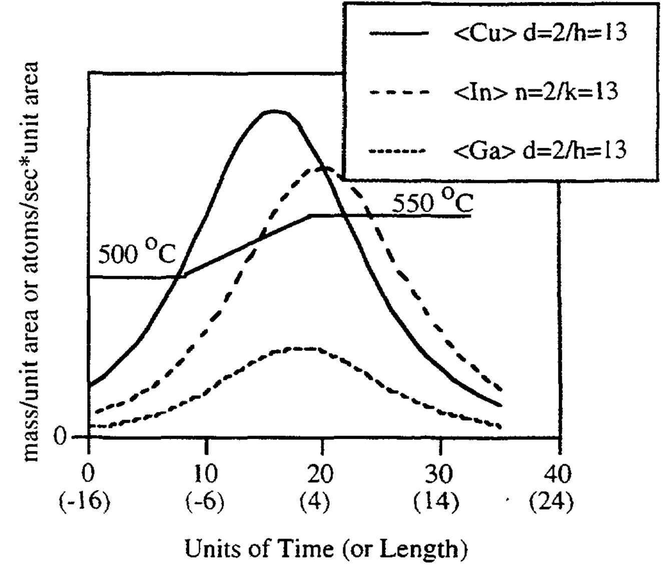

Fig. 2. Metal Flux Profiles and substrate temperature profile used in experimental runs.

2-Source In-Line Evaporation System (CIS only)

In this case, we take material 1 to be Cu and material 2 to be In. Material 3 is not considered. From the spatial distributions (eqns. 11 and 12), we can obtain an expression for the metal flux ratio (Cu to In):

$$dM_1/dM_2=(M_{e1}/M_{e2})*\{[h^2+(d-x)^2]/(h^2+x^2)\}^2 \quad (14)$$

This is the general form of the Flux Ratio (FR) that the substrate will see as it moves along the X-axis. Fig. 3 shows the shape of the flux ratio (Cu to In) for a given set of design parameters "d" "h". The values of "x_0" and "x_1" for this graph were taken as -16 and +20, respectively.

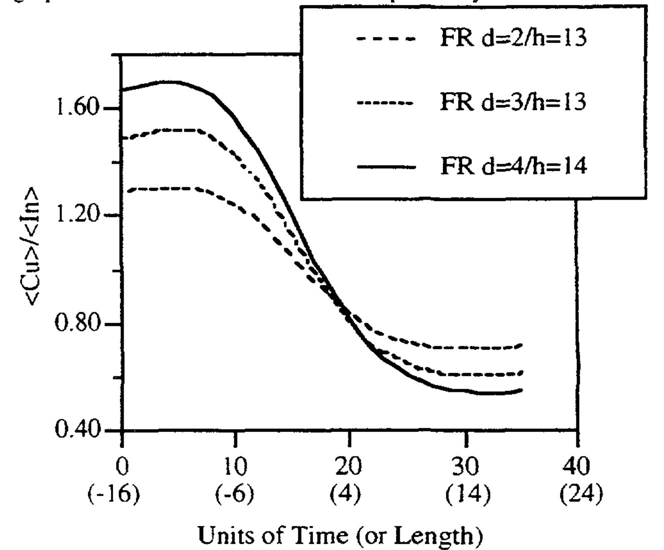

Fig. 3. Flux Ratio (FR) Profiles for 2-Source System

3-Source In-Line Evaporation System (CIGS)

In this case, we take material 1 to be Cu, material 2 to be Ga and material 3 to be In. In a similar way, from equations 11, 12, and 13, we can derive expressions for the metal flux ratios. These expressions are not shown, but Fig. 4 displays the generic shape of the metal flux ratios for a set of design parameters h=13, k=13, d=13, n=2, x_0=-16, and x_1=+20.

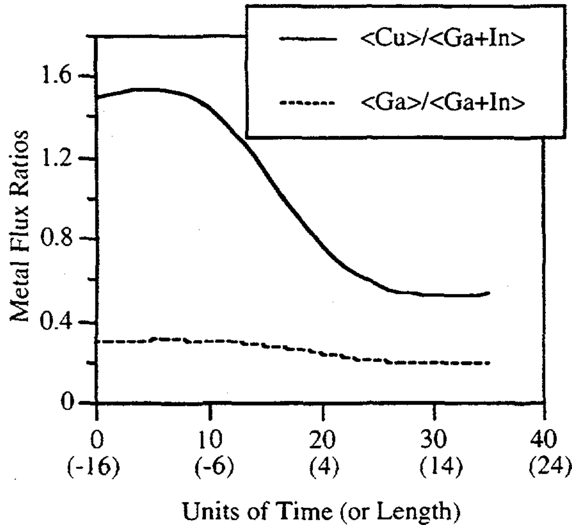

Fig. 4. Flux Ratio Profiles for 3-Source System

COMPUTER VALIDATION OF THE IN-LINE SYSTEMS

To validate either set-up (2- or 3-source evaporation in-line system), we can make a time-space analogy in which distance along the X-axis is replaced by real time. In this case, we will emulate the spatial profile of an evaporant source by a time-dependent function of the same form as the spatial distribution. In a 2-source system the equations for each individual evaporant source have the form

$$CuFlux=k_1*h^2/[h^2+(t+x_0)^2]^2 \quad (15)$$

$$InFlux=k_2*h^2/\{h^2+[d-(t+x_0)]^2\}^2 \quad (16)$$

for a 3-source system:

$$CuFlux=k_1*h^2/[h^2+(t+x_0)^2]^2 \quad (17)$$

$$GaFlux=k_2*h^2/\{h^2+[d-(t+x_0)]^2\}^2 \quad (18)$$

$$InFlux=k_3*k^2/\{k^2+[n*d-(t+x_0)]^2\}^2 \quad (19)$$

where t is time in minutes and k_1, k_2, and k_3 are constants related to the constant evaporation rates/masses. Fig. 2, 3, and 4 show the different curves associated with these time-dependent equations. The computer program written in Quick Basic converts the time-dependent fluxes (units of atoms/sec*unit area) into evaporation rates (units of Å/s) that are sent to the deposition controller (Inficon Sentinel III) via an IEEE 488 interface. The total thickness for evaporated copper has been set to about 3000 Å, which yields absorbers with a thickness of approximately 2.5 µm. The program terminates the Cu, In and Ga depositions when $t+x_0=x_1$. It is important to note that, in this type of configuration, film composition can be adjusted in three ways (assuming a fixed substrate temperature profile):

(1) by adjusting k_1, k_2, and k_3
(2) by changing the values of x_0 and x_1
(3) by changing the values of h, k, d and/or n.

In an actual in-line system k_1, k_2, and k_3 are related to the fixed evaporation rates from the sources, and the difference x_1-x_0 would be the length of the substrate holder/carrier aperture. The speed at which the substrate travels is emulated by the time it takes to complete a deposition. For the purpose of this current study, we have taken the simplest case of a 1-to-1 space-time analogy for which the emulated speed would have a value of 1 in/min (this implies that all design parameters are in inches units of length).

Experimental

To determine the optimum design parameters, we have carried out a set of experiments in which we have used different values for the design parameters. Fig. 3 shows the experimental metal flux ratio profiles for the depositions in the 2-source in-line case and Fig. 4, the metal flux ratios for the 3-source case. The Se flux profile is not shown in the figures, but, as previously mentioned, for the purpose of these experiments we have set the Se flux equal to three times the flux of Cu-plus-Ga-plus-In at any time with a minimum rate of 10 Å/s. The substrate temperature profile used in all experimental runs is shown in Fig.2. Upon completing the deposition the film is cooled from 550°C to 350°C in 20 min in a 10 Å/s Se vapor.

Devices were made by depositing a thin CdS layer on the absorber via a chemical bath deposition (CBD) technique described elsewhere [5,6], followed by annealing for 10 min at 200°C in an argon atmosphere. The window material used is ion-beam-sputtered ZnO (sputtering pressure of 10^{-4} Torr with argon as the working gas). The ZnO window is a bilayer in which the first 900 Å are deposited at room temperature in an $Ar+O_2$ atmosphere from an intrinsic ZnO target. The second layer is 0.5-µm thick n-type ZnO and is deposited at a substrate temperature of 100°C from a 2 %wt Al_2O_3-doped ZnO target. To reduce resistive losses, a Ni top-contact grid with 5% shadowing is electrodeposited. The finished devices also incorporate a MgF_2 anti-reflection coating.

Summary of Results

The polycrystalline thin film-absorber materials obtained by this emulation of the in-line coevapoartion systems have been characterized by electron probe for microanalysis (EPMA) and devices have been characterized by current-voltage (I-V) and external quantum efficiency (QE) measurements.

The following tabulated values represent the best from among several devices, and were obtained for global irradiation of 1000 W/m^2 and at a temperature of 25^oC. Efficiency values reported are <u>total area</u> conversion efficiencies.

2-source in-line system:

d	h	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
2	13	450	36.58	72.22	11.9
3	13	427	39.44	64.55	10.9
4	14	440	34.80	69.79	10.7

Table1. Summary of I-V data for CIS devices

3-source in-line system:

k1:k2:k3 [d=2:h=13 n=2:k=13]	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
1:0.25:0.75	559	31.52	72.30	12.7

Table 2. Summary of I-V data for CIGS devices

Summary of EPMA analysis (at%)

ID	Acc. Volt.	Cu	In	Ga	Se
best CIS	10 kV	23.85	26.45	0	49.71
	20 kV	24.59	25.37	0	50.03
best CIGS	10 kV	21.20	23.45	4.27	51.08
	20 kV	21.70	22.07	4.98	51.24

Table 3. Summary of compositional analysis for the best CIS absorber (11.9% efficiency device) and for the best CIGS

The external quantum efficiency is shown in Fig. 5 for the best CIS and CIGS devices. The shift in the wavelength cut-off has to do with the change in band gap associated with the CIGS absorber.

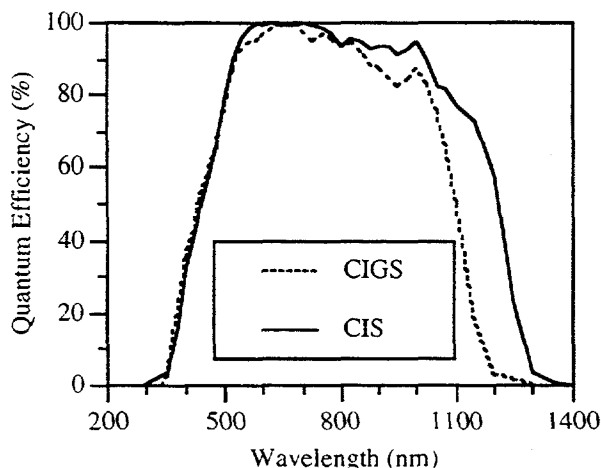

Fig. 5. Relative Quantum Efficiency for CIS and CIGS devices made following the in-line metal fluxes.

All films fabricated by these processes are characterized by large uniform grains (see Fig. 6). This type of morphology is very desirable for photo voltaic devices because larger grains translate into fewer losses due to grain boundaries. We believe the enhancement of grain size, as compared to morphologies obtained by the bi-layer process, is due to the higher substrate temperatures used and the initial higher Cu content in the flux (see J. Tuttle *et al.* in these proceedings).

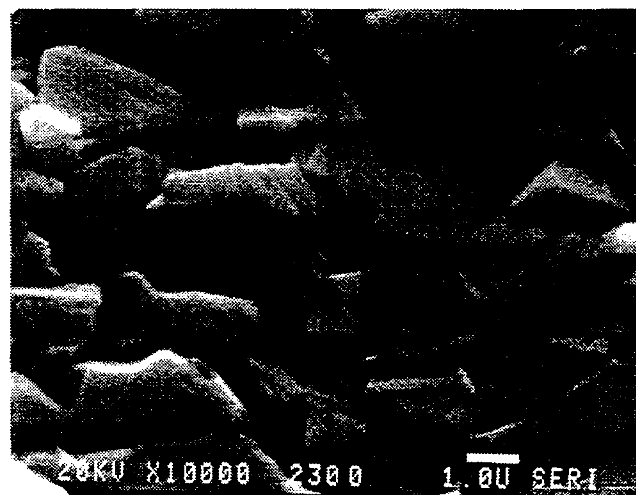

Fig.6. SEM of CIS film at 10,000 magnification. The white line represents 1 μm.

IN-LINE SYSTEM ENGINEERING DESIGN CONSIDERATIONS

The present study has been carried out for spatial distributions of point-evaporation sources (effusion cells and electron-beam deposition sources). Nevertheless, the study can be extended to line-evaporation sources that are trough-like in shape (evaporation boats), as long as the boats are placed transverse to the direction of the substrate motion (see Fig. 7).

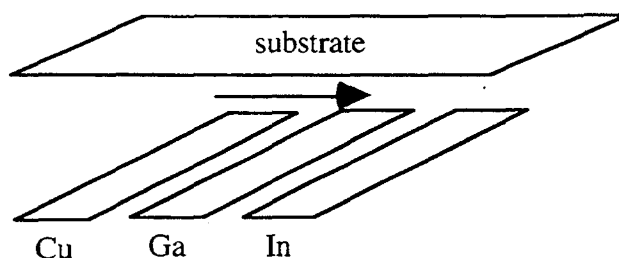

Fig. 7. Schematics of an in-line evaporation system that uses trough-like evaporation boats

An important design consideration is the supply of Se vapor for the formation of the compound. The particular cases we have studied call for a substrate aperture of 1m (3 ft); therefore, we recommend placing two Se sources: one before the first evaporant source and one after the last source (both halfway between the source and the extreme of the substrate aperture). This configuration will ensure enough of a anion over pressure for the formation reaction. Furthermore, as the development of CIS technology continues and studies on the role of S in the matrix is better understood, the anion source configuration we have discussed is flexible enough to

implement any changes for the production of $CuInS_2$, $CuIn(Se,S)_2$ and/or $Cu(In,Ga)(Se,S)_2$ absorbers.

The high substrate temperature (500°-$550^{o}C$) used in this validation study represents probably the greatest challenge for a substrate heater design. In reality, these high temperatures are very undesirable for vacuum evaporation not only because of the high electrical power needed but also due to temperature non-uniformity on the substrate itself.

Our experiments emulate the fabrication of a 1m (3 ft) long absorber in 36 min. In this regard, we can say that the only limitation in substrate speed for these proposed in-line systems will be the compound formation reaction rate. This aspect has not been covered here, but it is obvious that from a manufacturing point of view that output yield has to be increased.

CONCLUSIONS

We have explored the feasibility of an in-line coevaporation system for the production of CIS or CIGS absorbers that can be used to manufacture solar cells with efficiencies exceeding 10%. We have also shown the feasibility of incorporating an additional cation (Ga) to expand the band gap of the absorber and hence produce high voltage-low current solar cells. These higher voltage-lower current devices are more desirable in manufacturing since module resistive losses should be lower.

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AN UNCERTAINTY ANALYSIS OF THE SPECTRAL CORRECTION FACTOR

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ABSTRACT

Whenever a photovoltaic device is evaluated with respect to a reference spectrum, there is a spectral mismatch error. The photocurrent can be corrected for this error with a spectral correction factor, as is routinely done for primary and secondary terrestrial reference cell calibrations at laboratories throughout the world. The spectral correction factor has also been used to accurately measure the performance of cells and modules of any technology with respect to an arbitrary set of reference conditions. This uncertainty analysis considers the sensitivity of the spectral correction factor, and thus the measurement to which it applies, to choices of integration limits and uncertainties in the source irradiance and spectral response measurements from which it is derived. The uncertainty analysis involves Monte Carlo simulations of wavelength-dependent random errors and addition of systematic (bias) errors to the calculation's factors. It is demonstrated that error can be reduced or increased by reducing the wavelength range of the irradiance or spectral response measurement. The uncertainty in the spectral correction factor for standard lamp calibrations is found to exceed that for outdoor global normal calibrations. Correction factor sensitivities to resolution in spectral response data, and temporal instability of a Xenon arc-lamp solar simulator are discussed. That correction factor uncertainty rises with correction factor magnitude is verified.

INTRODUCTION

The spectral correction factor, M, (Equation 1) was originally formulated as the error in the photocurrent when measuring solar cell performance with respect to a reference spectrum [1]. For its derivation, see also Reference 2.

$$M = \frac{\int_{\lambda_1}^{\lambda_2} E_s(\lambda)\cdot S_t(\lambda)d\lambda}{\int_{\lambda_1}^{\lambda_2} E_s(\lambda)\cdot S_r(\lambda)d\lambda} \bullet \frac{\int_{\lambda_1}^{\lambda_2} E_{ref}(\lambda)\cdot S_r(\lambda)d\lambda}{\int_{\lambda_1}^{\lambda_2} E_{ref}(\lambda)\cdot S_t(\lambda)d\lambda} \qquad \text{(Eq. 1)}$$

Dividing the measured photocurrent by the spectral mismatch correction factor reduces the error in the photocurrent when measuring a solar cell under any light source $E_s(\lambda)$ with respect to a reference spectrum, $E_{ref}(\lambda)$, shown in Figure 1 [3]. The limits of integration ($\lambda 1$ and $\lambda 2$) for all four integrals should be the same and encompass the entire range of the reference spectrum (305 nm to 4045 nm for the global reference spectrum). However, applying the spectral mismatch correction factor can also introduce error, as the irradiance and responsivity data that it uses contain random and bias errors from various sources. Emery [4] has studied the sensitivity of the correction factors to these error sources; this paper expands upon that work and uses wavelength-dependent error estimations.

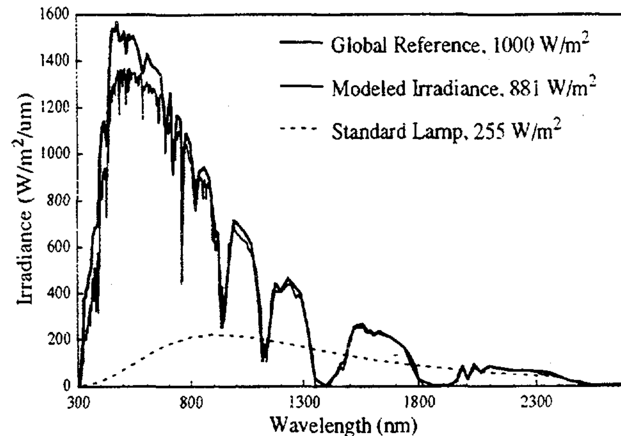

Figure 1. Spectral irradiance of the global reference spectrum [8], the modeled spectrum derived from a typical direct normal spectral irradiance measurement taken October 26, 1992 at NREL, and the spectrum of the F275 NIST standard lamp

The wavelength range of the integration to compute the spectral correction factor is effectively limited to the responsivity ranges of the test cell $S_t(\lambda)$ and reference detector $S_r(\lambda)$ (photovoltaic or thermal) (see Figure 2). It can also be limited to 300-1100 nm by the range of Si-based spectroradiometers that many PV laboratories use. NREL supplements the Si spectroradiometer measurement with data from a Si/PbS spectroradiometer for indoor simulator-based calibrations and with a comprehensive atmospheric transmittance model [5, 6] for outdoor calibrations. Using integration limits smaller than the range of the test and reference cell responsivities effectively removes part of the spectral correction factor, causing errors that depend on the spectral response range of the test device, reference device, and the light source. If the ranges removed contain substantial uncertainties, the removal could reduce the uncertainty. This question has been explored by Emery [7], and is explored further here.

ALGORITHMS AND METHODS

To integrate spectral response and irradiance data numerically for the spectral response factor, a modified trapezoidal method described in the ASTM standard E 892-87 [4] is used. The midpoint of each trapezoid is used to linearly interpolate a point from the spectral response data. Half of the beginning and ending

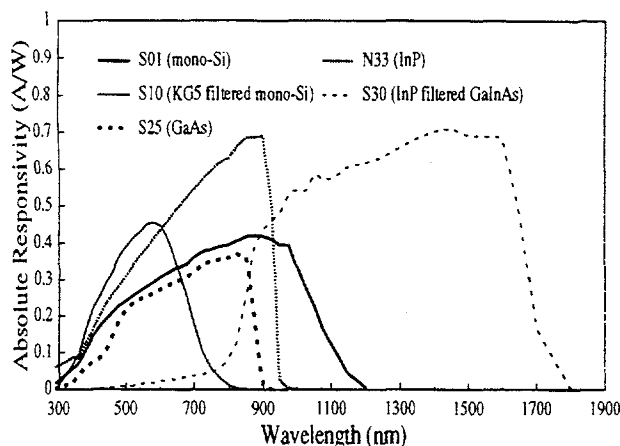

Figure 2. Spectral responsivity of solar cells considered in this analysis

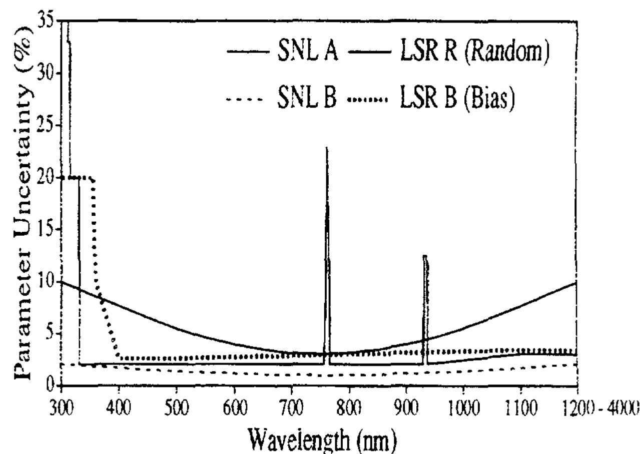

Figure 3. Measured source irradiance error estimation functions. SNL A and SNL B are from the Sandia analysis [10]. LSR R and LSR B pertain to the spectroradiometer and are derived from Reference 12. The peaks correspond to uncertainty in the spectroradiometer measurement due to potential wavelength error near deep absorption bands in the solar spectrum.

trapezoids are added to the result to approximate the error caused by irradiance or response beyond the wavelengths of the data sets. All measurements described in this analysis translate to the global normal spectrum in the standard.

Monte Carlo analysis is used to compute the effect of random errors in source irradiance and device spectral response upon the spectral correction factor. The error source is a pseudo-random number generator with a Gaussian distribution centered at zero with amplitude such that 95 % of the numbers generated are within the error limits established by the error estimation function. The simulated errors are applied to each wavelength-specific number in the data set. Bias errors are simulated by simply adding or subtracting the error estimate to the data. Random errors are symmetrically applied; bias errors are either added or subtracted (table column headings with a "-" preceding the error estimation function name). The error source irradiance estimation functions for outdoor calibrations with natural sunlight are shown in Figure 3. Random errors are combined by adding their squares and taking the square root of the sum. Bias errors are treated the same way. To combine random and bias errors together to conclude a single uncertainty, the square of the total bias error is added to the square of twice the random error, and the square root is taken, as summarized by Abernethy and Benedict [9]

The SNL A and SNL B error estimation functions are those used in the Sandia analysis [10]. The spectral response random error estimation function is (SR R) 2.5%, wavelength independent, and based on repeated measurements of the same sample over 3 years [11]. The bias error (SR B) is derived from [11] but a region between 850 and 1600 nm is estimated at ± 5.0% due to varying intensities of sharp peaks in the spectrum of the Xenon arc lamp source in the equipment.

The estimate of the uncertainties in the irradiance of the standard lamp are derived from a report by Myers [12] and shown in Figure 5. Estimates of uncertainty caused by the locally used lamp power supply and the current monitoing meter are added to the estimates from NIST for the random error pertaining to the lamp itself. Uncertainty in lamp-to-cell distance was not included as a random error because it affects the entire spectrum. The numbers in Myers' chart for noise equivalent power (NEP), wavelength repeatability, and temperature control are not included because they pertain to spectroradiometer calibrations. Twice the error from the root-sum-square method is used as the limit for the random number generator. The bias error is derived similarly, using the numbers from Myers' report, but using a distance uncertainty of 0.2 mm for 0.8 mm because it is reasonable to be able to place the solar cell's space charge region within 0.5 mm of 0.5 meters from the lamp filament. As for the source random error estimate, wave accuracy and temperature control of the spectroradiometer are not relevant. Additional information about the uncertainty in standard lamp spectra can be found in [13].

The LICOR spectroradiometer random (LSR R) and bias (LSR B) error estimates are derived from the Myers report as well. The random errors listed for the spectroradiometer calibration due to NEP, Temperature control, and wave repeatability are treated as bias errors and added by root-sum-square to the bias errors of the standard lamp to which it is calibrated. However, an exception is made for wavelengths less than 355 nm. The bias error is estimated at 20% because successive spectroradiometer calibration files and measurements using the spectroradiometer indicate that the actual errors are much smaller than that allowed by Myers' tabular analysis. This could have been achieved by averaging multiple measurements during calibration. NEP's influence on solar measurements was computed by comparing the manufacturer's NEP specification of 0.7 W/m^2 / µm [12] to the global reference spectrum irradiance at various wavelengths. Errors computed were 7.6% at 305 nm and fell to nearly zero at 330 nm. Additional error is contributed by the wavelength repeatability of the instrument. Its manufacturer allows 0.5 nm error for each wavelength, so when scanning a spectral region where the intensity varies sharply, this can contribute a large error. In the ultraviolet region, this error is substantial, ranging from 50% at 305 nm to 2% at 330. It has peaks at 762.5 and 934 nm due to absorption bands there. Elsewhere, 2%

is assumed. Temperature control has little effect on the readings until 1100 nm, where Myers estimates it at 1.0%. These three error sources are combined to produce the error estimation function denoted "LSR R." The wavelength accuracy and repeatability of the spectroradiometer also become an issue when measuring spectra with sharp peaks, such as arc lamps used in solar simulators.

SENSITIVITY OF SPECTRAL CORRECTION FACTOR FOR OUTDOOR CALIBRATIONS TO CHOICE OF INTEGRATION LIMITS

NREL's outdoor calibration system is described in [14]. When computing the spectral correction factor, the source spectral irradiance data from 305 to 4000 nm are estimated via an improved version of the atmospheric transmittance model described in [5], using measured data from 350 to 936 nm and meteorological information collected during each cell measurement. The modeled spectrum closely matches the measured spectrum between 350 and 1100 nm. The accuracy of the model from 300 to 350 nm and 1100 to 4000 nm can be inferred by comparing the measured total irradiances with the integrated modeled irradiance, which is typically within ± 3.0%. The spectroradiometer measurement uncertainty is high between 300 and 350 nm as shown in Figure 3, but this wavelength region is not used by the model.

For reference cell calibrations performed outdoors under natural sunlight, the reference device is a thermal detector (pyranometer, pyrheliometer, or cavity radiometer) with a $S_r(\lambda)$ that is nearly independent of wavelength. For thermal detectors with a quartz dome, the responsivity is weighted by the transmission of quartz. The spectral responsivities of thermal detectors is rarely known and assumed to be a constant. The method referred to here utilizes a cavity radiometer. The Calibration Value (Equation 2) is computed from the measured photocurrent (I_{sc}) the total irradiance measured by the reference device (E_{tot}), and the spectral correction factor M (Equation 1).

$$CV = \frac{I_{sc}}{E_{tot} \cdot M} \qquad \text{(Eq. 2)}$$

Truncating the integrals in the numerator and denominator of Equation 1 could be motivated by lack of irradiance or spectral response information or desire to remove from the spectral correction computation wavelength regions with higher levels of uncertainty. But this also removes information about the reference spectrum and might contribute error as well. To evaluate the effect of this technique, several actual calibration measurements of cells of different materials are considered. For each device listed, sets of data gathered during 2 or 3 days of outdoor measurements are used. The variation among each set of corrected measurements is assumed to be caused in part by errors in each spectral correction. Reduction in the variation is interpreted as indicative of reduction in the spectral correction error.

Figure 4 shows that integration range truncation can reduce the random error in the spectral mismatch correction factor in some cases, but not others. The random error does not change drastically when using a smaller integration range. However, while the spectral correction factor standard deviation remains small when truncating the integral, the spectral correction factor computed changes significantly for some cells. The uncorrected data for S10, while it shows a smaller standard deviation, produced a calibration value 2.0% lower than that computed when the spectral mismatch correction factor was used. S25's correction factor for the 300-1100 nm integration limits was 2.2% lower than that calculated without truncation. Reducing the integration limits for spectral mismatch correction factor calculation may introduce significant errors in M and different results for the calibration value.

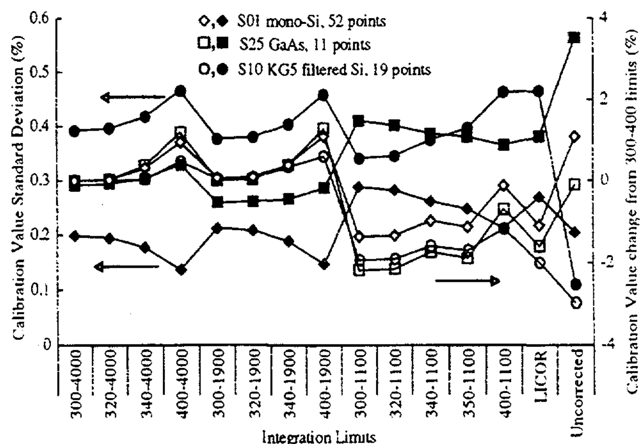

Figure 4. Effect of integration limits choice on variability of corrected calibration number for three reference cells. The column marked "LICOR" uses the measurement from the spectroradiometer, without modeling, from 350 to 1100 nm in 2 nm steps with 4 nm bandwidth.

SENSITIVITY OF SPECTRAL CORRECTION FACTOR TO MEASURED IRRADIANCE AND SPECTRAL RESPONSIVITY UNCERTAINTY FOR OUTDOOR CALIBRATION

A LICOR LI-1800 spectroradiometer with a 5° field of view [15] measures the spectral information for NREL's outdoor direct normal calibrations. Various estimations of its error are considered to evaluate that error's likely impact on calibration accuracy. Two error distributions are similar to those used in the Sandia analysis [10], and two are derived from the uncertainties estimated by Myers [12] (Figure 3) and described above.

First, these estimates are applied by Monte Carlo analysis to five natural sunlight calibrations to determine the effects of random errors with these magnitudes. For the random error case, these errors are applied to the modeled irradiance (see Table 1). To examine the effect of bias errors, these estimations are applied to the measured irradiance before applying the model, and to the modeled irradiance derived from the measured irradiance information without any error applied (see Table 2).

These results indicate that the spectral correction factor is quite insensitive to the random errors in spectral responsivity and irradiance. The random error analysis showed a worst case error of 0.11% in the second column of Table 1. The first column is included to compare the two error estimation assumptions. The

worst case bias error estimation is 0.25%, based on simulations of spectroradiometer error applied before applying the model in columns 3, 4, and 5 of Table 2. The first two columns are included to compare the analysis results of different error estimations. Combining the bias and random errors computed here produces a 95% confidence interval uncertainty of ± 0.33%.

Table 3 compares the result of this analysis with calculations and assumptions made in earlier analyses. Results differ due to variations in assumptions about the nature of the uncertainties involved. However, this estimate is much smaller than that made in the Sandia analysis [10]. Table 3 shows that for the bias error, this difference is largely due to different assumptions about the nature of the spectrally dependent uncertainties involved.

The integration limits analysis (see Figure 4) shows that the total error has a standard deviation of about 0.4%, still within the conclusions of [10]. Other error sources in the calibration contribute to its variation and may be the reason it exceeds the uncertainty shown above.

Table 1. Uncertainty in the spectral correction factor caused by simulated random uncertainty in measured spectral irradiance and device responsivity for a typical outdoor direct normal calibration measurement on October 26, 1992.

Irradiance Error Function:	SNL B	LSR R	
Spectral Response Error Function:	SNL B	SR R	
Device Calibrated	% Standard Deviation		M
S01 (mono-Si)	0.030	0.052	1.0124
S10 (KG5 filtered mono-Si)	0.049	0.080	0.9673
S25 (GaAs)	0.036	0.071	1.0060
S30 (InP filtered GaInAs)	0.062	0.105	1.0583
N33 (InP)	0.035	0.067	1.0069

SENSITIVITY OF SPECTRAL CORRECTION FACTOR TO UNCERTAINTIES ASSOCIATED WITH STANDARD LAMP SOLAR CELL CALIBRATION METHOD

Calibrating a reference cell using a standard lamp involves a large spectral correction factor since the lamp's spectrum differs greatly from the global reference (see Figure 1). However, the calculation is simplified (Equation 3) because a reference detector is not used. The nominal spectral irradiance of the lamp, $E_{lamp}\lambda$, is provided with the lamp.

The uncertainty analysis considers the lamp spectral uncertainties and device spectral response uncertainties shown in Figure 5. The lamp bias error estimate includes the effects of uncertainty in lamp to cell distance. The lamp irradiance declines with the square of the distance between the lamp filament and the space-charge region of the solar cell being calibrated. Setting this to exactly 0.5 meters is not a simple task.

The lamp spectrum uncertainty's effect on the spectral correction factor is evaluated with Monte Carlo analysis for random errors (see Table 4) and by multiplying by a wavelength-dependent bias error simulation (see Table 5). The largest random error likely to be encountered for a standard lamp measurement is 0.78%, according to Table 4. The largest bias error expected is 2.62%, from Table 5. These error estimates are taken from the 2nd and 3rd columns, corresponding to uncertainty estimates derived in this paper. A device nonlinearity uncertainty of 0.5% should be added (assuming an attempt to correct is made) since the standard lamps' irradiance is about one quarter sun at 0.5m.

$$CV = I_{sc} \cdot \frac{\int_{\lambda_1}^{\lambda_2} E_{ref}(\lambda) \cdot S_t(\lambda) d\lambda}{\int_{\lambda_1}^{\lambda_2} E_{lamp}(\lambda) \cdot S_t(\lambda) d\lambda} \quad \text{(Eq. 3)}$$

These estimates exceed those made by Sandia [10], which concludes an uncertainty of 1.30% for this method. Tables 4 and 5 indicate that the method applied here produces similar error estimates for the assumptions made in the Sandia analysis, but that different estimations of error in this analysis produce the larger result.

Table 2. Uncertainty in the spectral correction factor caused by simulated bias uncertainty in measured spectral irradiance for an outdoor direct normal calibration measurement on October 26, 1992 (* Indicates error estimation applied before model applied)

Irradiance Error Function:	-SNL A	LSR B	LSR B*	LSR B*	-LSR B*	
Spectral Response Error Function	SNL A	SR B	None	SR B	SR B	
Device Calibrated	% Bias Error in M					M
S01 (mono-Si)	1.49	-0.21	0.06	0.09	0.05	1.0124
S10 (KG5 filtered mono-Si)	0.98	-0.41	0.10	0.10	0.18	0.9673
S25 (GaAs)	1.84	-0.36	0.01	0.02	0.08	1.0060
S30 (InP filtered GaInAs)	-1.63	0.07	0.17	0.17	-0.25	1.0583
N33 (InP)	1.82	-0.28	0.04	0.06	0.06	1.0069

Table 3. Comparison of spectral correction factor assumptions and estimations. The method total column indicates the uncertainty estimatin that includes spectral correction a spectral correction factor, uncertaintyies and other error sources involved in the

Reference:	Bias	Random(σ)	Method total	Conditions, notes
This Report	0.25%	0.11%	-	NREL outdoor method
1987 RR [11]	0.20	0.20	0.72	NREL outdoor method
Osterwald [14]	0.0	0.20	1.00	NREL outdoor method
Sandia [10]	2.61	0.29	2.7	NREL outdoor method, wavelength dependent errors, includes Isc and Etot uncertainty
1987 RR [11]	0.20	0.18	1.09	X25 simulator
Emery [4]	0.01%	0.21%	0.97%	Simulator calibration, best case
Heidler [16]	0.54	0.03	2.3	AEG Simulator, mono-Si

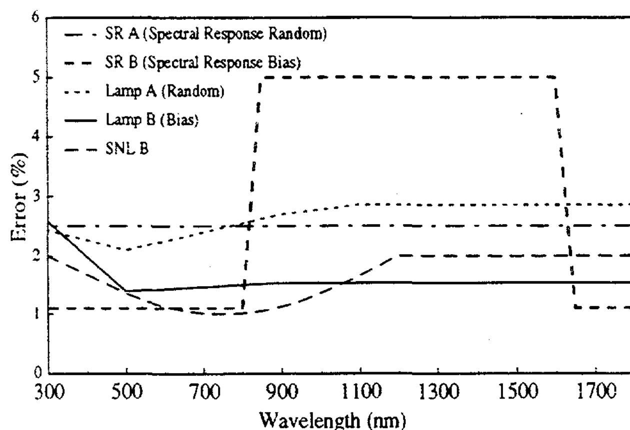

Figure 5. Error estimation functions for standard lamp calibration procedure

Table 4. Uncertainty in the spectral correction factor due to uncertainty in standard lamp spectral irradiance data and other uncertainties of the procedure

Irradiance Error Function	SNL B	LAMP R	LAMP R	
Spectral Response Error Function	SNL B	SR R	None	
	Standard Deviation			
Device Calibrated	% Random Error in CF			CF
S01 (mono-Si)	0.34	0.73	0.57	5.570
S10 (KG5 filtered mono-Si)	0.28	0.58	0.48	13.382
S25 (GaAs)	0.32	0.77	0.58	7.020
S30 (InP filtered GaInAs)	0.43	0.67	0.55	2.058
N33 (InP)	0.34	0.78	0.60	7.441

Table 5. Effect of wavelength dependent bias errors in irradiance and spectral response on spectral correction factor calculations.

Irradiance Error Function	-SNL B	LAMP B	LAMP B	
Spectral Response Error Function	SNL B	SR B	None	
Device Calibrated	% Bias Error in CF			CF
S01 (mono-Si)	1.22	-2.62	-1.48	5.570
S10 (mono-Si under KG5)	1.27	-1.43	-1.44	13.382
S25 (GaAs)	1.16	-2.30	-1.46	7.020
S30 (GaInAs under InP)	1.64	-1.66	-1.50	2.058
N33 (InP)	1.17	-2.10	-1.46	7.441

Table 6: Propagation of errors in test and reference cell spectral response to spectral correction factor as it depends on the resolution of the spectral response data.

Test Cell & Error	Test Cell resolution	Ref Cell & Error	Ref Cell resolution	Source & Error	variation in M 2σ, %
L746, 5%	20 nm	S04, 5%	20 nm	X25, 5%	0.42
L746, 5%	20 nm	S04, 5%	40 nm	X25, 5%	0.81
S02, 5%	40 nm	S04, 5%	20 nm	X25, 5%	0.56
S02, 5%	40 nm	S04, 5%	40 nm	X25, 5%	0.88
S02, 10%	40 nm	S04, 10%	20 nm	X25, 5%	1.09
S02, 10%	40 nm	S04, 10%	40 nm	X25, 5%	1.74

Monte Carlo perturbation analysis with rectangular and wavelength independent simulated error distributions was conducted to compare the propagation of random errors in spectral response to the spectral correction factor for the same calibration

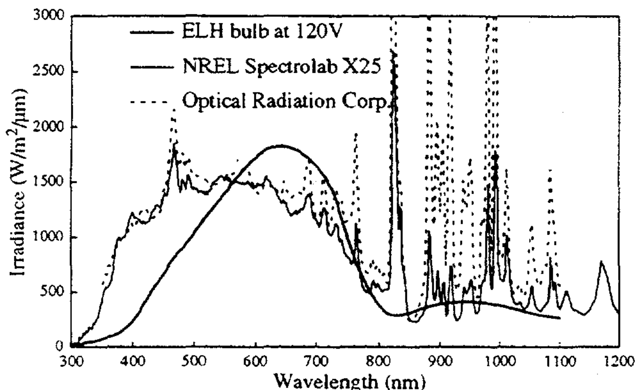

Figure 6. Spectral irradiance of three solar simulators

SPECTRAL CORRECTION FACTOR UNCERTAINTY DEPENDENCE UPON RESOLUTION IN SPECTRAL RESPONSE DATA

Monte Carlo perturbation analysis was conducted to compare the propagation of random errors in spectral response to the spectral correction factor when the resolution of the spectral response data changes. Unlike other Monte Carlo analysis in this paper, the errors applied were rectangular in distribution and had no wavelength dependence. Correction factors are computed for a single junction amorphous silicon and a monocrystalline silicon cell calibrated to the global reference spectrum with NREL's Spectrolab X25 solar simulator and a mono-Si reference cell. Table 6 summarizes the results.

This analysis shows that halving the resolution of the spectral response data enables the random error in responsivity measurement to have a much larger effect on the spectral correction factor uncertainty. The resolution in the spectral response data used for the analysis elsewhere in this paper is 20 nm from 360 to 700 nm and 25 nm from 700 to 1100 nm.

Table 7: Sensitivity of the error in the spectral correction factor to the magnitude of the spectral correction factor from Monte-Carlo analysis for various commonly used solar simulators.

Test Cell & Error	Ref Cell & Error	Source & Error	M mean	M 2* standard deviation, %
a-Si, ±5%	mono-Si, ±5%	Spectrolab X25; ±5%	1.0800	0.42
±10%	±10%	Spectrolab X25; ±5%	1.0800	0.83
±5%	±5%	ELH at 120 V; ±5%	1.1792	0.72
±10%	±10%	ELH at 120 V, ±5%	1.1792	1.43
±5%	±5%	ORC, ±5%	0.8567	0.57
±10%	±10%	ORC, ±5%	0.8567	1.32

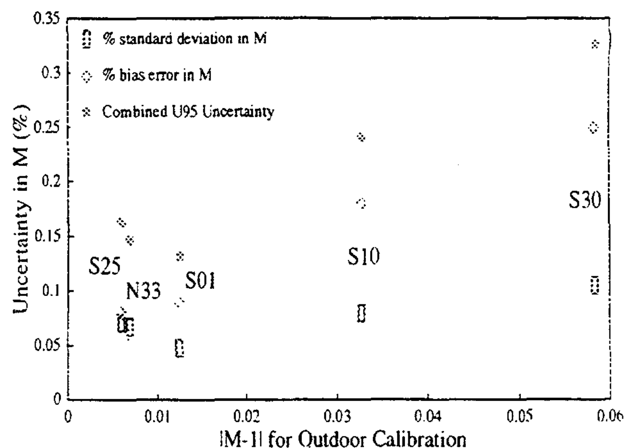

Figure 7. Correction factor uncertainty's dependence on correction factor magnitude for outdoor calibration

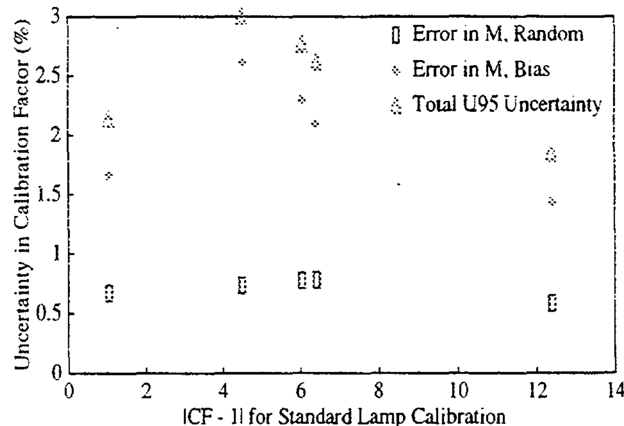

Figure 8. Correction factor uncertainty's dependence on correction factor magnitude for standard lamp calibration

SENSITIVITY OF THE SPECTRAL CORRECTION FACTOR TO THE MAGNITUDE OF THE SPECTRAL CORRECTION FACTOR

Because each spectral response and irradiance data set appears in both numerator and denominator, systematic bias errors in any of the four sets are expected to cancel out [2]. But because different function products apply in the numerator and denominator, and bias errors are not wavelength independent, errors can propagate to the result. Thus, the spectral correction factor uncertainty may increase with spectral correction factor magnitude. The worst bias and random uncertainties for each calibration considered in outdoor and standard lamp calibrations in Tables 1-6 are plotted against the spectral correction factor magnitude to evaluate this expectation (Figures 7 and 8).

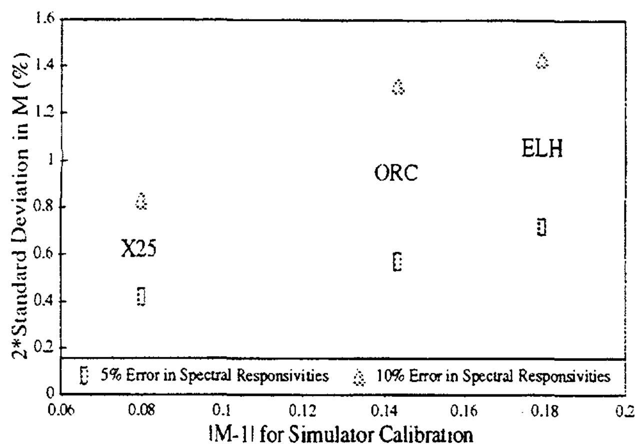

Figure 9. Spectral correction factor error dependence on spectral correction factor magnitude for simulator calibration

made on various simulators. Spectral irradiance plots for the simulators listed can be found in References 3 (Optical Radiation Corporation) and 17 (X25 and ELH). The data is presented in Table 6 and Figure 9.

The graphs show that for the outdoor calibration, the variation in spectral correction factor rises as the factor itself rises. But in the standard lamp case, the correction factors are very large, and there is no apparent correlation.

OTHER SPECTRAL RESPONSE FACTOR SENSITIVITIES

The spectral irradiance of the light source for standard lamp calibrations is provided with the lamp. For outdoor calibrations, it should be measured while the cell being calibrated is measured [7]. But this is impractical when making simulator-based calibrations. Emery [17] shows that the spectral correction factor for NREL's Spectrolab X25 solar simulator changes less than about 1.5% over 100 hours of operation for a poorly matched reference and test cell combination, and that the change is smaller for better matched combinations. Thus, periodic measurements of a simulator's spectrum may be sufficient to control drift error in M due to simulator spectrum drift.

Spectral responsivity can depend on the cell bias voltage during measurement [18]. Spectral response measurements at NREL are generally made with the cell at approximate one-sun bias, but other laboratories may not do this. This work has assumed the quantum efficiency is independent of bias. Thus, some uncertainty is present for outdoor calibrations with natural sunlight levels not exactly one sun, and standard lamp calibrations, with light intensities near one quarter sun.

CONCLUSIONS

This analysis has shown by using carefully derived estimations of wavelength-dependent bias and random errors, that the uncertainty in the spectral mismatch correction factor for outdoor direct normal solar cell calibrations concurs with earlier claims and is significantly smaller than that for the standard lamp calibration method. The estimation in spectral mismatch error presented here differs from that presented by Sandia [10] for accurate reference cells for a wide variety of photovoltaic technologies primarily due to different assumptions about the magnitude and nature of the error estimations applied. Under global sunlight, the spectral irradiance measurement will have an additional error source because of the non-ideal cosine angular response [15, 19].

Reduction of error in the spectral correction factor for outdoor and simulator-based calibrations can be achieved by minimizing the factor itself. Such reduction can be achieved by choosing reference cells similar to test cells or test sources similar to reference spectra.

To verify that use of the spectral correction factor reduces error, NREL conducts periodic reference cell calibration checks, comparing simulator-based calibrations to ones made outdoors. Spectral mismatch correction factor error can dominate the differences between calibrations of the same devices with the same reference detector on different light sources.

ACKNOWLEDGMENTS

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SECOND CONTROLLED LIGHT-SOAKING EXPERIMENT FOR AMORPHOUS SILICON MODULES

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ABSTRACT

Dual-junction and triple-junction amorphous silicon modules from three manufacturers were subjected to light soaking at 1-sun intensity at 50°C, loaded to the maximum power point, for 1000-2000 hours, with annealing to 70°C in the dark after 1000 hours. Performance characterization was done periodically, both under a pulsed solar simulator and outdoors. Aperture-area efficiencies as high as 9.1% were obtained after 1000 hours of light-soaking. The power output after 1000 hours of light soaking and subsequent partial annealing ranged from 77% to 92% of the initial power output. The recovery in power due to annealing was 4%-6.5%. For a-Si/a-Si-type modules, stabilized performance was reached before 1000 hours. The validity of the results is discussed in detail.

INTRODUCTION

The stabilized efficiency for amorphous silicon modules is important because of the impact that efficiency has on the cost for power and energy from such modules. In 1991, we conducted controlled light-soaking tests on dual-junction and triple-junction amorphous silicon modules fabricated in 1990 by three manufacturers to assess the progress made in module stabilized efficiencies at that time [1]. The present experiment was designed to provide information on the stabilized performance under outdoor operating conditions of the latest-type modules manufactured from late 1991 through December 1992. One objective was to simulate module performance under actual operating conditions in a typical environment in the United States. Such a typical environment would result in approximately 50°C module temperature for most of the year and up to 70°C during the summer months [2]. About 1200-1400 hours at 1000 W/m^2 is a reasonable estimate for one year of outdoor exposure in terms of light-induced degradation [1]. Consequently, we subjected the modules to 1000 hours of 1000 W/m^2 illumination at 50°C, while loaded near their maximum power point, and then raised the temperature in steps to 70°C to allow recovery in power output. We wanted to see whether the 70°C annealing would affect the long-term performance or only improve the performance for a short time. Subsequently, we subjected the modules to another 1000 hours of illumination at 50°C. Another objective was to determine the time required to reach stabilization for modules of various designs. A final objective was to study the effect of lower exposure temperatures than 50°C.

SAMPLE DESCRIPTION

The following groups of modules were subjected to extended light-soaking. In the subsequent text, these modules will be called "test modules."

2-1. Solarex. Five triple-junction (a-Si/a-Si/a-SiGe), 795-cm^2 aperture-area modules fabricated in 1992 with i_1 layer thicknesses in the 60-80-nm range, i_2 layers in the 300-400-nm range, and i_3 layer in the 160-190 nm range. The bandgaps are 1.74/1.74/1.44 eV. The p-i-n/p-i-n/p-i-n layers are deposited on tin-oxide-coated glass by direct-current glow discharge. All three p-layers are a-SiC:H. The modules have a single glass sheet, plastic frames, and contain 30 cells. The back reflector is sputtered (80-nm) ZnO/Ag. The back encapsulation is polyurethane.

2-2. USSC. Six dual-junction modules, dual-bandgap (a-Si/a-SiGe), 918-921-cm^2 aperture area, fabricated November 1991 through April 1992, with the i_1 layer thickness of 150 nm and the i_2 layers of 250 nm. The bandgaps are 1.76/1.45 eV. The p-layers are microcrystalline Si:H. The i_2 bandgap is the value at the minimum. The SiGe layers are profiled. The semiconductor layers are deposited by radio frequency glow discharge on stainless steel with a textured ZnO/Ag back reflector. The modules have indium oxide/Ag-grid front electrodes. The front encapsulation is Tefzel and ethylene vinyl acetate (EVA). The modules are not framed but have a black tape border. Two modules have 6 cells in series; the remainder consist of only a single cell.

2-3. USSC. Two triple-junction (a-Si/a-Si/a-SiGe) modules, 900-912-cm^2 aperture area, fabricated in November 1991. The intrinsic layer thicknesses are 100/350/250 nm; the bandgaps are 1.76/1.70/1.45 eV. Each module contains a single cell. The modules are otherwise of the same construction as those in group 2-2.

2-4. USSC. One dual-junction, same-bandgap (a-Si/a-Si) production module, 985-cm^2 aperture area, fabricated in October 1991, containing 6 cells. The intrinsic layer thicknesses are 150/350 nm; the bandgaps 1.76/1.70 eV. The modules are otherwise of the same construction as those in group 2-2.

2-6. Fuji Electric. Two dual-junction, same-bandgap (a-Si/a-Si) 1200-cm^2 modules with 30 cells in series. The a-Si is deposited on soda-lime glass coated with type-U tin oxide by Asahi Glass Co. The p-layer is boron-doped SiO_x. An undoped SiO_x buffer layer is also used [3]. The modules have no frame.

2-7. USSC. Six dual-junction, (a-Si:H/a-SiGe:H), 903-924-cm^2 aperture-area modules, having 1.75/1.4-eV bandgaps. Five consist of a single cell and one has 6 cells in series. They were

fabricated in June and November 1992. Otherwise, the modules are of the same structure as those in group 2-2.

2-8 **Solarex.** Five triple-junction (a-Si/a-Si/a-SiGe), 795- and 900-cm^2 aperture-area modules fabricated in October through December 1992 with i_1 layer thicknesses in the 60-80-nm range, i_2 in the 337-450-nm range, and i_3 layer in the 160-190-nm range. The i_1 and i_2 layers of these modules were deposited from 10:1 hydrogen-diluted silane. The bandgaps are 1.74/1.74/1.44 eV. Otherwise, the modules are of the same structure as those in group 2-1.

There were control modules (not subjected to light-soaking) for groups **2-1**, **2-2**, and **2-3**.

TEST CONDITIONS AND PROCEDURES

The initial module efficiencies were obtained by measurements outdoors under prevailing conditions on clear days in Golden, Colorado, March through May 1992 (with the incident intensity determined using pyranometer measurements and a crystalline silicon reference cell with a KG-5 filter), and indoors on a Spire 240A pulsed solar simulator. Subsequently, the control modules were kept in the dark at room temperature. The test modules were light-soaked at 1000-W/m^2 intensity (as determined by a crystalline silicon reference cell over 350-1100-nm wavelength region; ±10% error band) using an argon plasma light source (Vortek arc lamp), at a module temperature of 50°C, and were operated near their maximum power point using fixed resistors. The light-soaking was done in an environmental chamber with the chamber temperature adjusted such that thermocouples on the back of the modules measured 50°C (±5°C) with the light source on. The relative humidity in the chamber was very low (<15%). The light-soaking test started on May 5, 1992, for all groups except 2-7 and 2-8. Subsequent performance measurements at periodic time intervals were done on the Spire solar simulator at a module temperature of 25°C. After a total of 1000 hours of light soaking, the light-soaked test modules and the control modules, which were kept in the dark, were again measured outdoors on a clear day in Golden, Colorado, in August 1992, and also indoors on the Spire solar simulator.

After the above light-soaking was completed, the test modules were exposed in the dark to 60°C for a total of 240 hours and then to 70°C for an additional 10 hours, at which time no further recovery in power output was noted. Periodic efficiency measurements were taken during this temperature exposure on the Spire solar simulator at a module temperature of 25°C. Following this temperature exposure, some modules were remeasured outdoors under prevailing conditions in January 1993, and all were again measured on the Spire solar simulator. These data are shown as "recovered" in **Table 1**. The control modules were measured outdoors only after the test-module annealing exposure.

The test modules (except groups 2-1 and 2-2) that had

Table 1. Average Aperture-Area Efficiencies under Various Conditions, as Measured under the Spire Solar Simulator and Outdoors, and the Ratio of these Measurements (± indicates the 1s population value)

Sample Group	Condition	Indoor %	Outdoor %	Ratio indoor/outdoor
2-1 SX (average of five modules)	initial	9.69±0.04	9.13±0.11	1.061
	1000-h	7.58±0.21	7.73±0.24	0.981
	recovered	7.95±0.19	[7.59±0.19]	[1.047]
2-2 USSC (average of six modules)	initial	8.13±0.32	8.00±0.36	1.023
	1000-h	6.66±0.56	6.83±0.43	0.975
	recovered	6.94±0.55	[6.84±0.37]	[1.015]
2-3 USSC (average of two modules)	initial	7.75±0.08	7.33±0.17	1.057
	1000-h	6.67±0.28	[7.03±0.34]*	[0.947]
	recovered	6.93±0.24	NA	NA
	2000-h	6.62±0.15	6.49±0.25	1.020
2-4 USSC (single module)	initial	7.17	6.69	1.072
	1000-h	5.56	5.87	0.947
	recovered	5.92	NA	NA
	2000-h	5.69	5.65	1.007
2-6 Fuji (average of two modules)	initial	9.88±0.28	9.86±0.33	1.002
	1000-h	8.61±0.40	8.80±0.45	0.983
	recovered	9.10±0.31	NA	NA
2-7 USSC (average of six modules)	initial	9.55±0.47	9.30±0.16	1.027
	1000-h	7.17±0.49	7.17±0.92	1.000
2-8 SX (average of five modules)	initial	9.92±0.27	8.54±0.34	1.162
	1000-h	7.96±0.22	7.76±0.07	1.026

* High control module reading; NA = not available; [ ] questionable values

Table 2. Degradation in Percent of Initial Power under Various Conditions as Measured under the Spire Solar Simulator and Outdoors

Sample Group	Condition	Indoor %	Outdoor %
2-1 SX	1000-h	21.8	15.3
	recovered	17.9	[16.9]
2-2 USSC	1000-h	18.1	14.6
	recovered	14.6	[14.5]
2-3 USSC	1000-h	13.9	[4.1]*
	recovered	10.6	NA
	2000-h	14.6	11.5
2-4 USSC	1000-h	18.4	12.3
	recovered	17.4	NA
	2000-h	20.6	15.5
2-6 Fuji	1000-h	12.9	10.8
	recovered	7.9	NA
2-7 USSC	1000-h	24.9	22.9
2-8 SX	1000-h	19.8	9.1

* High control module reading; NA = not available
[ ] questionable values

previously been light-soaked for 1000 hours and annealed to 70°C were light-soaked for an additional 1000 hours at a module temperature of 50°C. Periodic efficiency measurements were made for these test modules on the Spire solar simulator at module temperatures of 25°C. Groups 2-7 and 2-8 were added to the test when the light soaking was resumed after the first 1000 hours and only subjected to a total of 1000 hours of light-soaking. Following the light soaking,

the modules and their controls were remeasured outdoors, under prevailing conditions in April 1993, and indoors on the Spire solar simulator.

RESULTS

The initial, 1000-hour, "recovered," and 2,000-hour average aperture-area efficiencies, as measured indoors and outdoors, and the ratio in efficiencies as measured under the solar simulator and outdoors for the three sample groups, are shown in **Table 1**. For those groups containing more than one module, average efficiency values and their standard deviation are reported. Shown in **Table 2** are the degradation in percent of the initial power as measured under indoor and outdoor test conditions. The outdoor efficiency data in Tables 1 and 2 are not corrected for temperature to 25°C but represent the efficiency at the prevailing module temperature.

In **Figure 1**, we show the average aperture-area efficiency of the seven groups of modules as a function of illumination time as measured under the solar simulator. The validity of that data is discussed in the next section. The data points up to 1000 hours of illumination have been used to generate stretched exponential curves [4]. The same-bandgap Fuji group has the highest initial efficiency, stabilizes after about 1000 hours, and has the highest stabilized efficiency. The two triple-junction Solarex groups have nearly the same initial efficencies, nearly as high as the Fuji group, but show different degradation behavior; the last fabricated group stabilizes earlier and at a higher level than the older group. Of the two USSC dual-junction, different-bandgap groups, the earlier fabricated one has a lower initial efficiency but both groups are projected to have the same stabilized efficiencies; the projection for the last fabricated group is uncertain because of the wide spread in the data points. The degradation behavior for the later dual-junction USSC group is similar to the earlier triple-junction Solarex group. The dual-junction and triple-junction different-bandgap USSC groups have similar stabilization times; about 2000 hours. The dual-junction, same-bandgap USSC group stabilized in about 1000 hours, but degraded about 18% compared to the 13% for the Fuji group.

WHAT IS THE VALIDITY OF THE EFFICIENCY AND DEGRADATION RESULTS?

There are a number of issues: 1) Is the selected temperature during light-soaking correct, and what are the effects of differences in temperature? 2) What are the effects of differences in spectra between the Vortek light source used in the test and sunlight? Is the effect different between same-bandgap and different-bandgap modules? 3) What is the error introduced by illumination spectrum and temperature during the efficiency measurements? and 4) Are the results from the controlled exposure test representative of actual

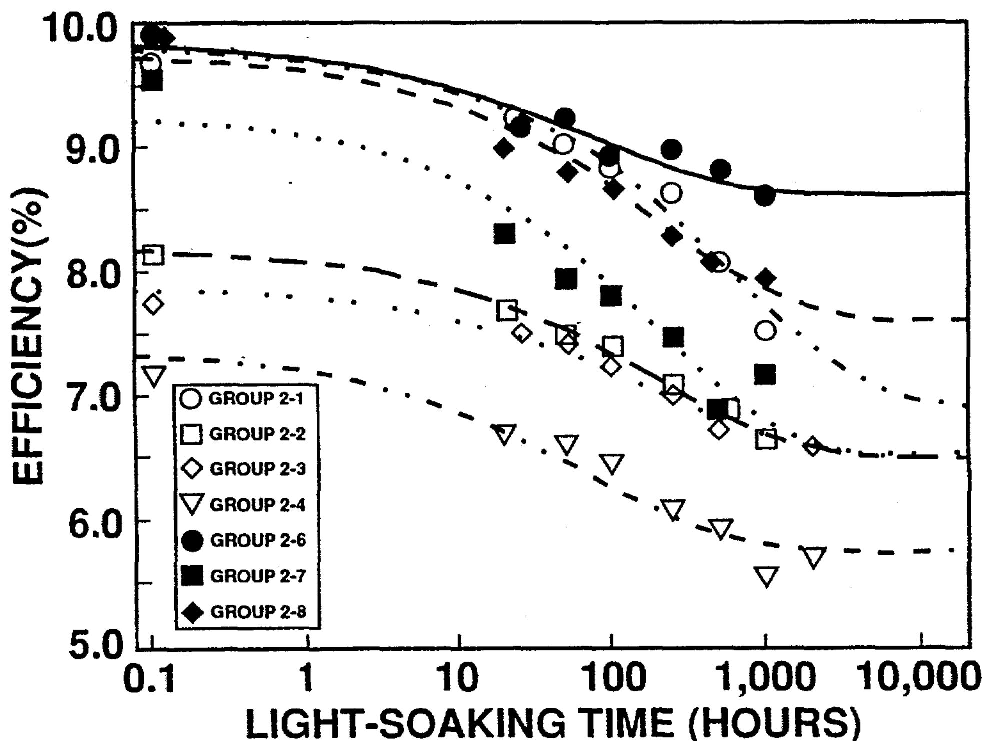

Figure 1. Average Aperture-Area Efficiency based on Solar Simulator Data versus Light-Soaking Time for Seven Groups of Modules.

outdoor exposure?

1) The stabilized performance is significantly affected by the temperature during exposure. NREL outdoor stability data on dual-junction USSC modules show that the degradation during winter months is higher than during summer months. That is, performance actually improves during summer months from that obtained during winter months. In Colorado, differences of 7 percentage points of degradation have been observed between summer and winter. Thus, in cooler climes, more degradation than observed in this 50°C test can be expected. The degradation increases by 2.5 to 4 percentage points for each 10°C lower temperature than the 50°C in our test [NREL unpublished data].

The modules that underwent the light-soaking test #1 [1] were subsequently deployed outdoors from April to August, 1992. The performance was periodically monitored on the Spire simulator. It was found that a remarkably fast adjustment of the stabilized performance occurred to a new, lower, stabilized level. This adjustment occurred for all three types of modules (same-bandgap dual-junction on glass and on stainless steel, and triple-junction on glass), albeit to different degrees. It was speculated that some of this adjustment might have been due to other causes (e.g., corrosion) rather than due to Staebler-Wronski-type degradation. However, we found by annealing at >140°C that the degradation encountered was reversible. This finding suggests that rapid adjustments of the stabilized state do indeed occur, and that the stabilized level essentially establishes itself within a relatively short time (~100 h) according to the actual temperature and illumination under operating conditions. This suggests that the constant 50°C condition of our test may noticably underestimate the degradation observed under real outdoor conditions in Colorado even during summer months.

2) The Vortek argon arc lamp has more energy in the 700-900-nm range than has AM1.5 sunlight. As a result, in triple-junction devices, the bottom layer is subjected to more than twice the number of photons as it would receive under outdoor conditions. On the other hand, the top and middle layers receive only 50% and 60%, respectively, of the AM1.5 radiation [5]. However, a comparative study of degradation of Solarex triple-junction modules outdoors and under sodium lamps found that the conditions used in the NREL light-soak test lead to the slowest and least degradation [6]. Consequently, the degradation conditions used in the NREL light-soak test may actually underestimate the degradation encountered under outdoor deployment.

According to our analysis of experimental data, the *stabilized* performance depends on the light-intensity (I): _(stable) =1 - $AI^{1/8}$, where A = fractional power loss at 1-sun intensity. This results for dual-junction (a-Si/a-Si) modules in a 1% higher output when exposed to the Vortek argon arc lamp as compared to sunlight exposure on the basis of light intensity alone [7]. On the other hand, it is estimated that for triple-junction (a-Si/a-Si/a-SiGe) modules the Vortek lamp results in 2% greater degradation than does sunlight. Thus, it appears that the maximum error introduced by the light-soaking spectrum not corresponding to the AM1.5 sun spectrum is on the order of ±2% for the stabilized value.

3) The Spire solar simulator efficiency data are used *purely for comparison purposes* to study the relative degradation in performance. Because the intensity and temperature are kept constant at 1000 W/m^2 and 25°C, respectively, the variations from one performance measurement to the next are minimized. However, the Spire 240A solar simulator appears to introduce errors in the current and fill-factor measurements (especially for triple-junction modules that consist of only a single cell) that are not related to the differences of its spectrum as compared to that of AM1.5.

For the purpose of assessing the actual efficiency, the outdoor data are preferred to the solar simulator data. The outdoor measurements were made under prevailing conditions in Colorado; thus, intensity, spectrum, and temperature may vary from one measurement to the next. Based on the open-circuit voltage, the active-layer temperature during winter measurements varied from 23°C to 40°C. It is difficult to correct all outdoor data for temperature, intensity, and spectral effects, because the temperature coefficients change with light-soaking. According to the manufacturers of the modules tested here, the temperature coefficients for power output *in the undegraded state* are negative, up to -0.1%/°C depending on the type of module. However, dual-junction amorphous silicon arrays deployed in the field have been reported to posses positive temperature coefficients for the power output in the stabilized state ranging from +0.001%/°C to +0.01%/°C, depending on the incident light intensity [8].

The absolute (random and systematic) error range for multijunction a-Si module efficiency measurements is ±10% with the solar simulator used, but the random errors from one measurement to the next are quite small for the simulator measurement (~ ±1%-2%) as seen from the consistency in the periodic measurement results of test and control modules. Thus, for the purpose of this study (i.e., assessing degradation and determining when stabilized performance is reached), meaningful results are found despite as much as ±8% of systematic uncertainty in the aperture-area efficiencies obtained from solar simulator measurements [9]. The error range for sunlight measurements is ±14% [10].

4) The controlled experiment does not simulate the effects of humidity or temperature cycling that may affect performance of modules in actual outdoor service. All degradation appears to be related to light-induced changes within the modules rather than to corrosion or similar effects. We derive this conclusion from the fact that control modules did not show any significant long-term degradation, and environmental conditions in the test chamber are kept constant and are generally benign.

DISCUSSION

The data represent the best stabilized amorphous silicon multijunction module performance measured to date at NREL.

We have established that light-soaking for 1000 hours under the controlled conditions (1000 W/m2, 50°C) leads to stabilization in the case of a-Si:H/a-Si:H dual-junction modules. a-Si:H/a-SiGe:H dual-junction modules seem to stabilize essentially within 2000 hours. In the case of the triple-junction modules, stabilization did not occur after 1000 hours of exposure. It has been previously reported that a-SiGe:H alloys may degrade more compared to a-Si:H [11]. It has also been reported, that in these modules, stabilized performance is further reduced by a light-induced shunting effect [12]. Based on data fittting with stretched exponential curves, stabilization for triple-junction modules is occuring only after 2000 to 20,000 hours.

After 1000 hours of light-soaking, annealing at 60°C and 70°C leads to a rapid partial recovery (3.9%-6.5%) in power-output as measured with a simulator. In this case, the simulator data are

believed more useful than the outdoor data, because the outdoor data showed a reduction rather than an increase in efficiency after annealing. About 50% of the recovery occurred within 10 hours after keeping the test modules in the dark at 60°C. Increasing the temperature to 70°C did not lead to any further significant recovery. This is similar to the earlier results [1].

The time scale for annealing at 60°C (10 hours half-time†) is considerably shorter than the time scale for light-induced degradation at 50°C (>100 hours half-time). Consequently, even after 100 hours of additional light soaking, the beneficial effects of the prior annealing step are still noticeable.

The initial performance under the solar simulator is generally higher than that under outdoor conditions. The difference is particularly pronounced for groups 2-1, 2-3, 2-4, and 2-8. After light soaking, some modules show higher performance under sunlight conditions, but the difference between indoor and outdoor data is less than 5% in all cases. The annealed outdoor data for groups 2-1 and 2-2 are questionable because they show no recovery as a result of the annealing. The wide error band in outdoor data may have swamped the relatively small recovery (4%-5%). The degradation as measured outdoors (11%-25%) is consistently lower than that measured under the solar simulator (13%-25%) and is considered a truer measure of the degradation. Group 2-6 contained a module with the highest initial (10.1%) and 1000-hour (9.1%) outdoor efficiencies, and it also had the lowest degradation (9.6%). Unfortunately, that module was damaged after the annealing step. The highest stabilized efficiency for a USSC module was 8.1% (Group 2-7) and for a Solarex module 7.8% (Group 2-8).

† half-time: the time required to achieve 50% of the total recovery or degradation.

CONCLUSIONS

1. The power output of some same-bandgap multijunction modules stabilizes after 1000 hours under conditions of 1000 W/m^2 illumination at 50°C when loaded near the maximum power point; for different-bandgap dual-junction modules, stabilization occurs within 2000 hours; and for triple-junction modules, stabilization occurs between 2000 and 20,000 hours.

2. A highest stabilized module efficiency was 9.1% (aperture area). This stabilized efficiency is an improvement over 1990 modules, when the highest efficiency was 7.2%.

3. The magnitude of the average light-induced degradation is 11%-23% (outdoor measurement) for 1000 hours of light soaking under controlled conditions.

4. There is some (4%-6.5%) recovery in the power output upon annealing in the dark at temperatures of 60°-70°C.

5. The recovery observed upon annealing appears to delay, but not arrest, further degradation in modules that were not stabilized.

6. The observed degradation is inferred to be light-induced. No indications for any other degradation mechanisms were observed.

7. The test results provide a reasonable assessment of stabilized efficiency and light-induced degradation at 50°C for modules made in 1992. There are indications that the test may overestimate the stabilized values compared to those established under prevailing outdoor Colorado summer conditions.

8. The test has established that multibandgap multijunction modules manufactured to date show neither lesser degradation nor improved stabilized performance compared to same-bandgap dual-junction modules.

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EFFECTS OF PROCESSING ON THE ELECTRONIC DEFECT LEVELS IN $CuInSe_2$

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ABSTRACT

The effects of $CuInSe_2$ preparation and processing on the electronic defect levels are investigated. Heat treatments in selenium are correlated with the electro-optical and structural characteristics of single-crystal and polycrystalline material properties and device parameters. High-resolution photoluminescence and deep-level transient spectroscopy studies are used to identify the energy levels associated with the chemical defect states dominating the $CuInSe_2$. The effects of Se heat treatments on existing and process-generated defect states (deep and shallow) are identified and correlated with the junction characteristics. Atomic force microscopy provides information on the nanoscale and microscale structural differences among the films as a function of the processing procedures.

INTRODUCTION

Although the conversion efficiencies of the $CuInSe_2$-based solar cells have now exceeded 13%[1,2], the defect structures of this semiconductor and its device interface properties remain areas of interest for understanding device performance and improving materials properties. The factors limiting minority-carrier properties are deduced from various studies, and the main contributors to lifetime losses in $CuInSe_2$ are point and chemical defects, grain boundaries, and impurities. The performance of $CuInSe_2$-based solar cells depends upon the defect chemistry and, consequently, on the methods used to produce and process the semiconductor and device. This paper provides an integrated and comparative study of the electronic defect levels in vacuum-deposited, sputtered, and post-selenized $CuInSe_2$ as functions of thermal, surface, and chemical processing. Thin film results are correlated with those on single-crystal control samples. Scanning tunneling microscopy (STM) and atomic force microscopy (AFM) are used to provide information on the micro- and nanoscale features of the polycrystalline thin films. Nanoscale investigations are used to provide first-time, direct evidence for the electronic defects associated with inherent and chemically-induced electronic defect levels.

EXPERIMENTAL DETAILS

The chemical compositions of n- and p-type films and crystals were determined using electron microprobe and Auger electron spectroscopy quantitative analysis techniques. The films were produced by the methods commonly used for device production. The crystals were grown by modified Bridgman methods. The crystals and film samples were Se-treated in closed quartz tubes (10^{-6} torr vacuum) with elemental Se as the source. These samples were inserted in a programmed furnace for the heat treatments, with temperatures up to 625°C for crystals and 400°C for polycrystalline thin films. X-ray data before and after treatment were consistent with results reported elsewhere for this semiconductor. Photoluminescence (PL) measurements were performed at room and low temperatures (5 K), and microchannel plate photon counting detection was used to provide time responses to the sub-100 ps level. Deep-level transient spectroscopy (DLTS) and capacitance-voltage (C-V) spectroscopy were used to determine the defect electronic levels for pre- and post processed samples. For these measurements, Schottky devices were fabricated by depositing Al dots (2000-Å thickness) on the surface of the p-type samples. The nanoscale investigations were carried out using an air-ambient AFM and vacuum-ambient spectroscopic STM. The spatial resolution of the AFM for these investigations was approximately 5 nm using a 10-μm scanning unit, and atomic resolution was obtainable on the STM.

RESULTS AND DISCUSSION

The dependence of the electrical and optical properties of $CuInSe_2$ on thin-film composition has been the focus of several previous studies. The processing of the material and the device has significant effects on the conductivity, optical absorption, and junction characteristics. These changes in composition and properties relate directly to the more fundamental electronic defect structure, population, and configurations. In this study, these defect levels are identified, along with their role in determining the electrical characteristics of the material.

Electronic Defect Studies

The results of the PL studies of this paper identify a correlation between the measured carrier concentrations and the dominant defect contributions. In p-type films and crystals having higher carrier concentrations (i.e. $N_a > 5 \times 10^{17}/cm^3$), the defect transition at 0.945 eV, corresponding to the Se_{Cu}-V_{Cu} transition, dominates the PL emission spectra. [The defect notation used here is A_B, where A is a particular species and B is the normal element at that position. V designates a vacancy, and i designates an interstitial.) Films and crystals with lower carrier concentrations (i.e., $N_a < 2 \times 10^{16}/cm^3$) are dominated by emissions from the low-energy 0.92-eV and 0.89-eV emissions, corresponding to the In_{Cu}-V_{In} and In_{Se}-V_{Cu} transitions, respectively. Another general correlation to the electrical characteristics is that the intensity of the In_{Cu}-V_{In} transition also increases with the carrier mobility. These concentration regions have significance for the processing procedures (thermal and selenization) used for the semiconductor. In addition, correlations in the controlling aspects of the defect configurations can be reported between single crystals and polycrystalline thin films. Figure 1 compares the PL emission spectra for two single-crystal samples having nearly identical initial compositions, before and after processing by Se diffusion. The relative concentration of the dominating defect levels has been altered as a

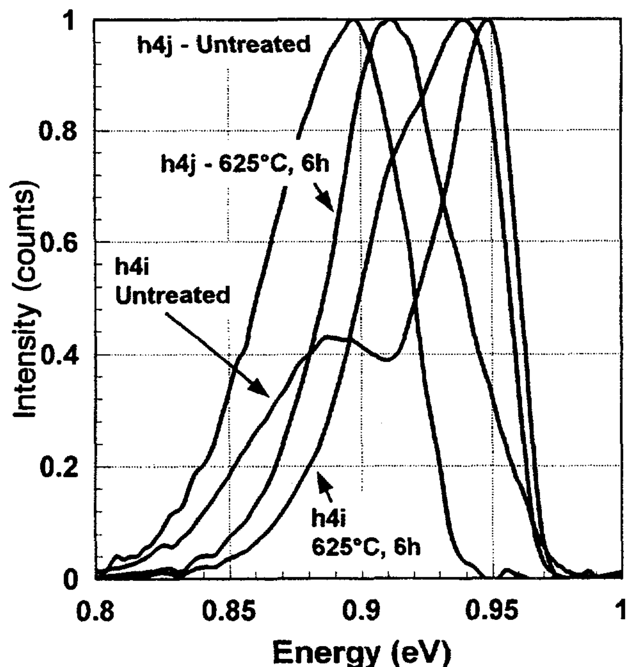

Fig. 1. PL emission from two $CuInSe_2$ single-crystals of identical composition, before and after Se diffusion at 625°C.

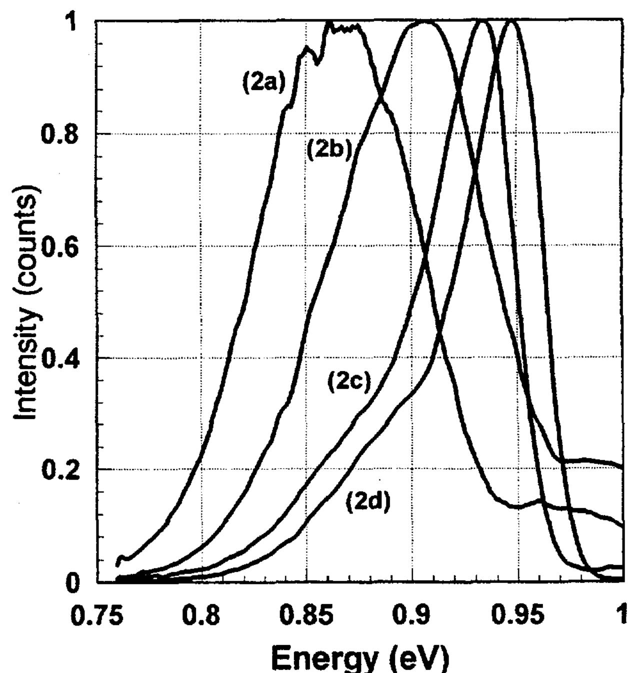

Fig. 2. PL emission from $CuInSe_2$ film before heat treatment (2a) compared to its emission after heat treatment at 300°C (2b), 350°C (2c), and 400°C (2d). Progressive shift associated with gradual change in defect chemistry is observed.

result of the processing in Se at 625°C. (It should be noted that the crystals are typically processed at higher temperatures to provide results similar to those of the thin films. It is postulated that this is primarily because of enhanced diffusion and incorporation of the Se and other species along the grain boundary defects.) The defect configuration (and majority-carrier conversion to p-type) changes abruptly after processing. The V_{Cu} and Se_{Cu} defects dominate in the higher concentration (after treatment) regime, but the original defect transitions are still observable in the PL data—even after treatment for long periods at higher temperatures [3,4]. The energy position of the Se_{Cu} level is sometimes interpreted to be associated with oxygen at a Se site (O_{Se}), but the nanoscale STM results presented later in this paper support the conclusion that this transition is due to the selenium[5]. This change does not depend significantly upon the conditions of treatment over the temperature range 300°-400°C for films and up to 625°C for crystals. However, the defect configurations for the polycrystalline films are controlled by the processing. The correspondence between the final defect configuration and the heat treatment is shown in Fig. 2. The characteristic of Fig. 2 is that of a typical n-type film. The progressive change in the relative concentration and type of defect levels as the film changes from n- to p-type is observed with the temperature level (shown here at 300°, 350°, and 400°C) in the Se atmosphere. The defect configuration and dominance depend critically on the temperature.

The final dominating electronic transitions identified in these PL studies do not depend on the initial compositions of the films. This important result is illustrated in Fig. 3, which presents data on a nearly stoichiometric (barely Cu-rich) and an initially Cu-deficient film. Similar final PL signatures are obtained for the same processing treatments. These results are consistent for films prepared by various techniques, including three-source co-deposition, selenization of In/Cu precursors deposited by sputtering or evaporation or sputtered films. In all cases, Se_{Cu}, Se_{In}, In_{Cu}, and Se_i are the dominant defects after the Se treatment. The relative degree of dominance depends upon the length and the level of the thermal treatment and not the initial composition or preparation method.

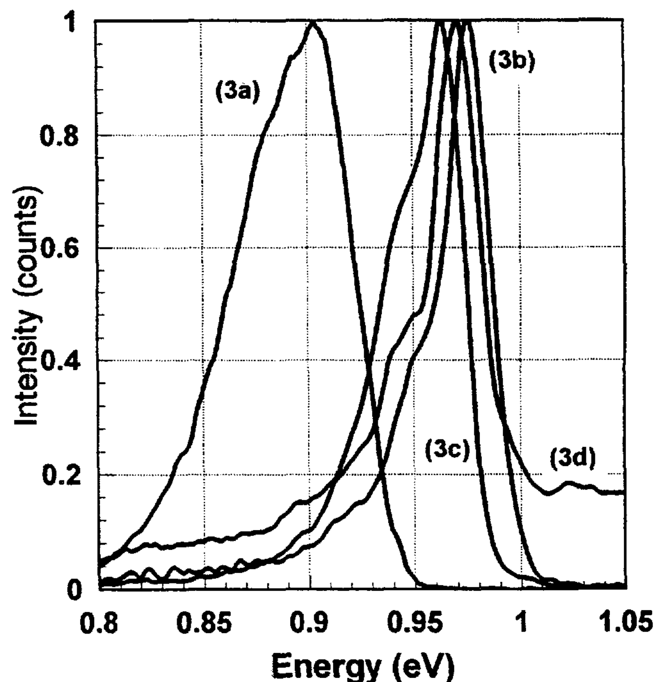

Fig. 3. PL emission from stoichiometric (3a) and Cu-rich (3b) $CuInSe_2$ films before and after the heat treatment in Se atmosphere (3c and 3d), respectively

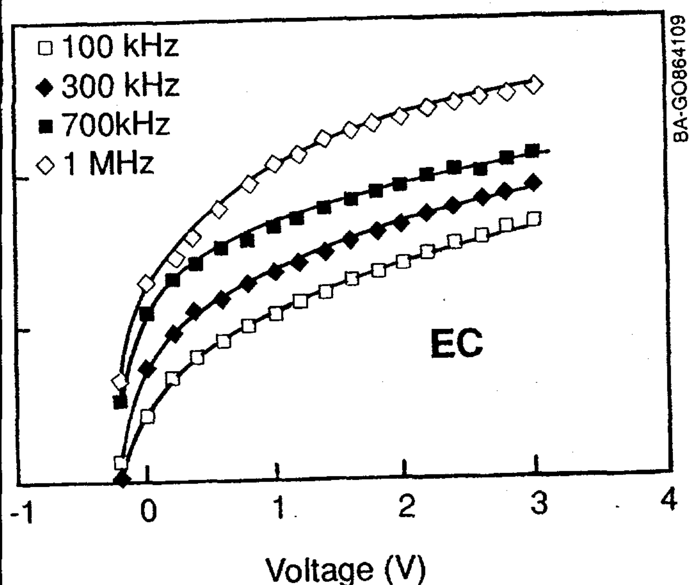

Fig. 4. C^{-2} vs. V dependence (as a function of frequency) of an Al/p-type, thin-film CIS Schottky barrier before processing.

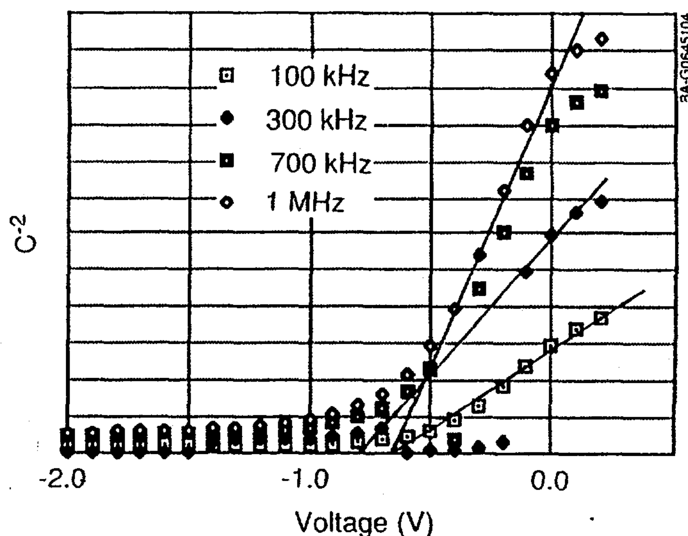

Fig. 5. C^{-2} vs. V dependence (as a function of frequency) of an Al/p-type, thin-film CIS Schottky barrier after the Se heat treatment.

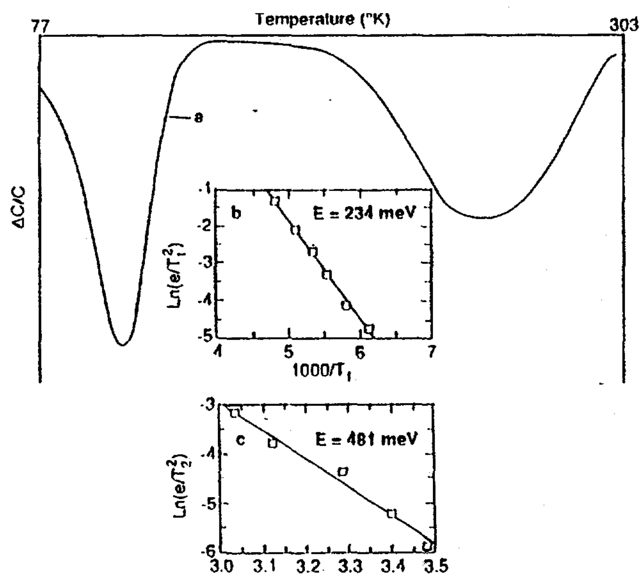

Fig. 6. Deep-level transient-spectroscopy and Arrhenius graphs for an Al/p-type, CIS thin-film Schottky barrier before receiving the Se heat treatment.

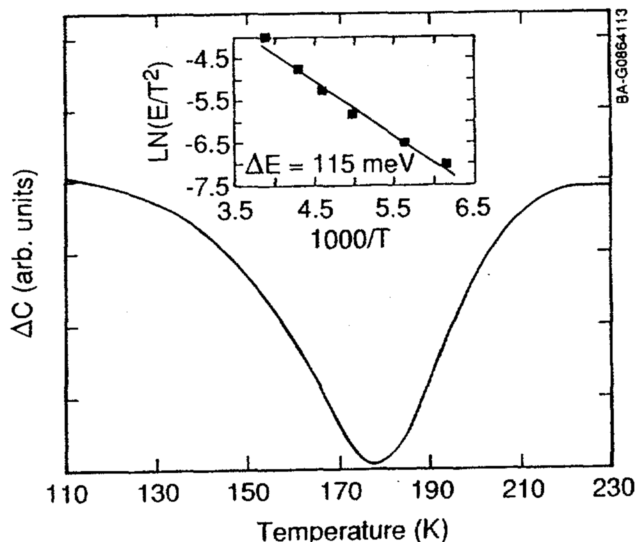

Fig. 7. Deep-level transient-spectroscopy and Arrhenius graph for an Al/p-type, thin-film CIS Schottky barrier after receiving the Se heat treatment.

The modification in the defect configuration in the $CuInSe_2$ films as a function of the processing treatment is determined from the junction characteristics and DLTS measurements. Figure 4 presents C^{-2}-V characteristics for an Al Schottky barrier structure as a function of Se and heat treatment. For the unprocessed structure, an interfacial layer of multiple interface states dominates the junction region. This interfacial region is present for both Schottky barriers formed on thin films and crystals. After processing the structures in Se at elevated temperature, the characteristics become linear (Fig. 5), with the slopes increasing with frequency. This indicates a high density of a single interface state. These data are further confirmed by the DLTS results in Figs. 6 and 7. Before heat treatment (Fig. 6), several deep defect levels are observable. The effect of the Se heat treatment (Fig. 7) is to lower

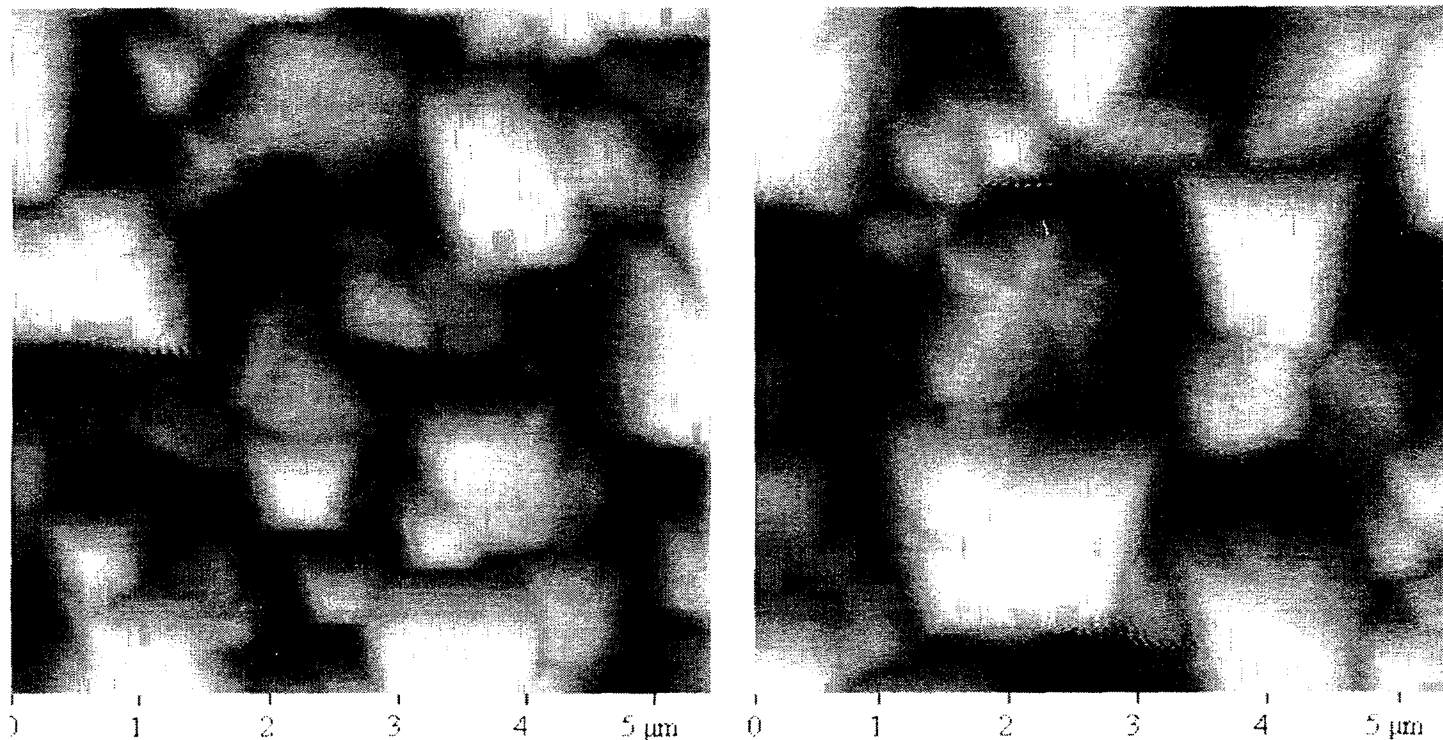

Fig. 8. AFM topographical images of $CuInSe_2$ film sample S1 before and after receiving the Se heat treatment.

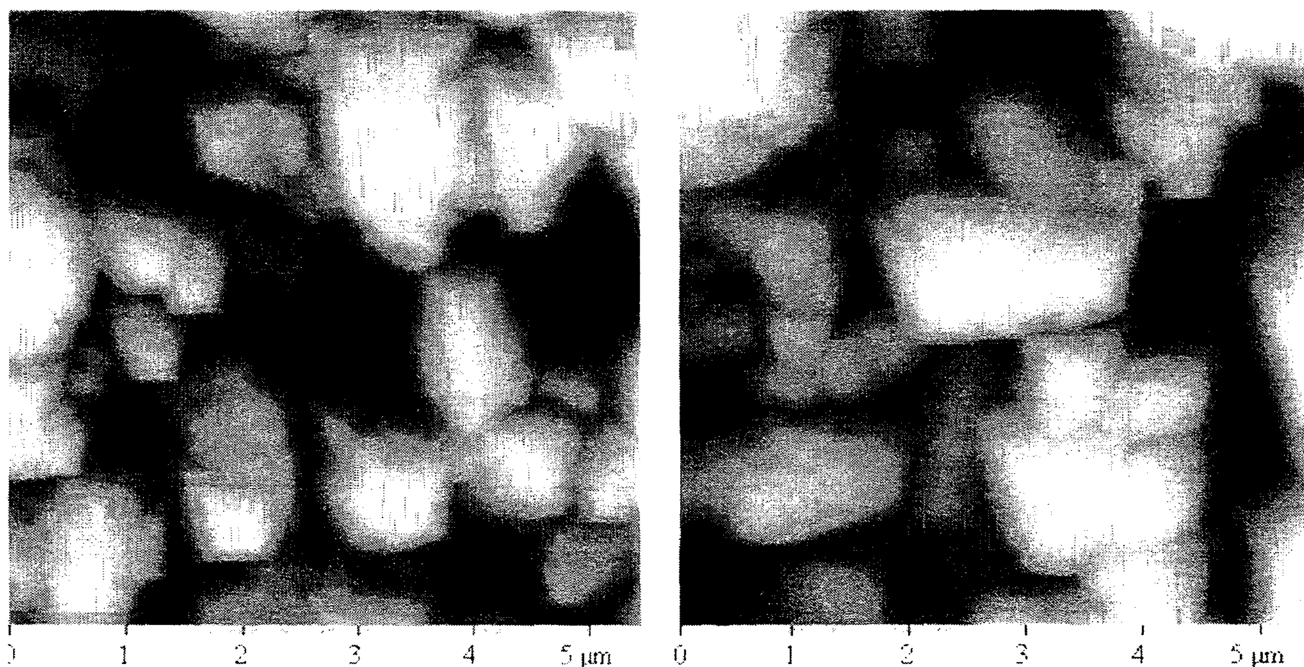

Fig. 9. AFM topographical images of $CuInSe_2$ film sample S2 before and after receiving the Se heat treatment.

the deep level state density, with a single state measured at 115 eV. This single state is much shallower than the two (or more) recorded for the pre-process case. The effect of the processing is to annihilate the deep states, and to provide distinct shallower states associated with Se chemical defects. Combining these results with the PL measurements, the dominant defect state is Se_{Cu} after Se treatment.

Structural and Nanoscale Investigations

The associated effects of the Se heat treatments on the film topography are indicated in the AFM micrographs in Figs. 8 and 9. The microscale features presented are typical for all the films studied. Fig. 8 provides information on a p-type film, nearly stoichiometric in composition, before and after processing (400°C, 4 hrs). Figure 9 presents similar measurements on a p-type, Cu-rich

film. In each case, substantial grain growth is observed following Se heat treatment. These changes are consistent with the modification in the defect levels and populations determined from the studies in the previous section. Defect contributions associated with the grain boundaries are certainly lowered as a result of the grain growth. In addition, the progressive shift in the PL signal as a function of temperature is consistent with this growth and associated annihilation/change of defects during such a process [6].

The electronic position of the defect levels associated with the Se have been confirmed using nanoscale investigations with the STM. The STM has been used for the removal and placement of atoms at specific sites at $CuInSe_2$ surfaces [7]. The effects of removal or Se atoms (to produce Se vacancies) has been measured with nanoscale PL technique. These results are presented in Fig. 10. The STM probe is used to confine the optical excitation laser light probe through its electric field. This confinement greatly enhances the spatial resolution of the light source, to regimes significantly better than those predicted from the wavelength of the light. This method provides spatial confinement of the light source impinging on the surface to the hundreds of Å level, and the resulting PL signal provides an evaluation of that small region [7]. These PL data show the evolution of the Se-vacancy transition upon atom removal. In this case, oxygen is placed at the site, with the resulting evolution of that transition. The position of this peak corresponds to the VSe levels observed in the PL data for the unprocessed films and crystals. However, the placement of oxygen at the Se site results in a defect transition to the O_{Se} that differs significantly form the Se_{Cu} or other post-processed levels identified in the macroscale PL data [3,4]. Therefore, these nanoscale PL data confirm that the Se treatments do not introduce oxygen or oxygen-related defects during the processing, and the changes in the electronic characteristics are associated completely with the placement of the Se.

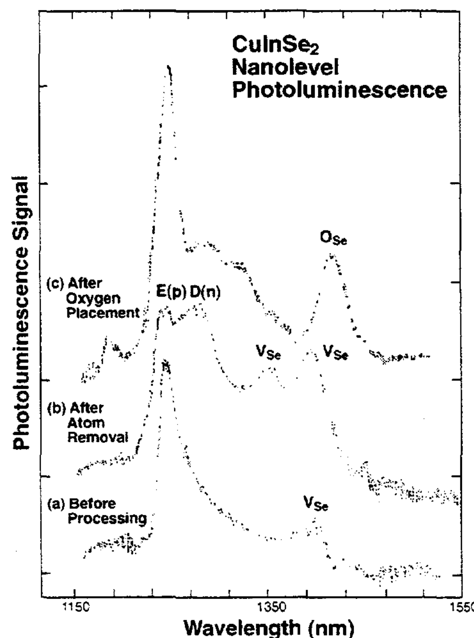

Fig. 10. Nanoscale PL for $CuInSe_2$: (a) pre-processed crystal; (b) after removing Se atoms (Se vacancies); (c) after oxygen placement, indicating origin of PL transition signals.

SUMMARY AND CONCLUSIONS

The electronic defect levels in $CuInSe_2$ have been investigated as functions of post-deposition processing (heat treatment in Se). Results for single crystals and polycrystalline thin films are compared. The following observations are made:

(1) Two distinct majority-carrier concentration regimes have been identified for both films and crystals, with higher concentrations ($>2 \times 10^{16}/cm^3$) dominated by In_{Cu} to V_{In} and In_{Se} to V_{Cu} transitions, and lower concentrations ($< 5 \times 10^{17}/cm^3$) dominated by Se_{Cu} to V_{Cu} transitions.

(2) Processing of crystals differs significantly from that of films. The crystals have an abrupt change from initial defect configurations to final states (V_{Cu} and Se_{Cu}), with some degree of the original defects always present, as long as the temperature exceeds 300°C. The films, however, show a progressive shift in the relative concentration and type of defect levels as the film changes from n- to p-type is observed over the range 300° to 400°C.

(3) Similar final PL signatures are obtained for the same processing treatments. These results are consistent for films prepared by various techniques, including three-source co-deposition, selenization of In/Cu precursors deposited by sputtering or evaporation or sputtered films. In all cases, Se_{Cu}, Se_{In}, In_{Cu}, and Se_i are the dominant defects after the Se treatment. The relative degree of dominance depends upon the length and the level of the thermal treatment, and *not* the initial composition or preparation method.

(4) DLTS measurements show that pre-processed films have multiple defect levels present, and that the Se/heat treatment provides annihilation of the deep levels. In most cases, only a single deep level dominates after processing.

(5) Nanoscale characterization using AFM and STM shows that significant grain growth accompanies the processing. This grain growth is consistent with the changes and lowering of the defect level in the films. In addition, nanoscale PL has confirmed that the O does not play the dominant role in the Se treatments, and supports the identification of the Se_{Cu} level in the macroscale PL data.

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POLYMER ENCAPSULANTS CHARACTERIZED BY FLUORESCENCE ANALYSIS BEFORE AND AFTER DEGRADATION

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ABSTRACT

Structural changes of the luminescent chromophores in various polymer encapsulants for photovoltaic modules due to processing, weathering and artificial degradation are characterized by the non-destructive, non-invasive fluorescence analysis. Undegraded, simulation-degraded, and weathering-degraded EVA films have been studied. The results show that curing the EVA films can generate new chromophores of α,ß-unsaturated carbonyls that can be excited by UV light up to ~400 nm. Their concentration in the EVA films made by a typical slow-curing process for EVA A9918 formulation is greater than those made by a fast-curing process for EVA 15295 formulation. Photothermal degradation of the EVA begins with an increase and lengthening of these chromophores. The UV-exposed EVA A9918 in solar cells turns brown and exhibits two types (one short and one long) of chromopores, and the thermally treated EVA shows yellow and only the short chromophores. The extent of discoloration from yellow to dark brown is a direct measure of the extent of degradation and an indication of an increase in the length of the polyconjugated carbon-carbon double bonds (polyenes). Similar results are observed for the weathering-degraded, yellow and brown PVB encapsulants in roof-top modules.

INTRODUCTION

Ethylene vinyl acetate (EVA) copolymer has been widely used as an encapsulant material for several types of photovoltaic (PV) modules since its development in early 1980s [1-4]. In comparison, poly(vinyl butyral), PVB, has been used to a lesser degree. In addition to providing structural support and electrical insulation for the solar cells, the encapsulant's long-term stability to remain optically transparent over a long period of time is highly desired for a consistent current output from PV modules. However, discoloration from light yellow to dark brown of both EVA and PVB in field-deployed modules has been observed at various sites and is partly responsible for the various degrees of loss in the efficiency and power output of the modules [5-7]. The discoloration is a consequence of structural changes on the chromophores, primarily due to the formation of polyenes on the EVA polymeric chains [8,9]. In practice, it is desirable to have an analytical method to detect or monitor in-situ the extent of degradation of the polymer encapsulants. Use of fluorescence analysis (FA) in our earlier work to characterize undegraded and degraded EVA film samples was found satisfactory [8,10]. This paper describes our work extending the use of FA as a non-destructive and non-invasive analytical method to characterize the free-standing EVA films and the EVA encapsulated in solar cells before and after simulated, thermal and photothermal degradations.

EXPERIMENTAL

Uncured and cured EVA sheet samples of various formulations (including A9918 and 15295) and small size, EVA-encapsulated solar cells were provided by several PV manufacturers. The monocrystalline Si (c-Si) and polycrystalline Si (pc-Si) solar cells have a glass superstrate, and the amorphous Si (a-Si) cells have a Tefzel cover layer on the EVA. The EVA A9918 contains a curing agent, Lupersol 101, for a typical (slow) curing process, and the EVA 15295 contains Lupersol TBEC for a fast curing process during the lamination-encapsulation step [3,4]. Weathering-degraded EVA and PVB films samples were taken from PV modules deployed in the field for several years.

Simulated thermal degradation was conducted in ovens in the dark from 85°C to 130°C and simulated photothermal degradation in a Sunlighter exposure chamber using three 100-W GE RS4 UV (mercury) lamps at 85°C±2°C or in a DSET Suntest CPS tabletop exposure system using a 1.8-KW-rated Xe arc lamp at 60°C±3°C for a certain period of days.

Chemical analysis of the undegraded and degraded EVA films involved extraction with methanol to remove the UV absorber (Cyasorb UV 531) and other ingredients and with tetrahydrofuran to determine the gel content (degree of cross-linking) of the EVA samples [8].

UV-visible absorption measurements of the methanol extracts were performed on an HP-8452A spectrophotometer to quantify the UV absorber. Fluorescence analysis employed a new SPEX model FL112XI Fluorolog-II fluorescence spectrophotometer equipped with a 450-W Xe lamp, four variable slits set at 0.50-mm width for both entrance and exit on the monochromators, and a Hamamatsu R928 photomultiplier

(PMT) emission detector and a Hamamatsu R508 PMT reference detector using Rhodamine B as the quantum counter. For free-standing EVA and PVB films, a solid sample holder was used to clamp flat the samples in such a way that the film plane was at a preset angle of 121° to the incident excitation light beam (clockwise). For encapsulated solar cells, the measurements were conducted directly through the front side glass or Tefzel superstrate with the plane of the solar cell positioned at an angle of 122.5°. All spectral data acquisitions were conducted with the "front-face" geometry and were uncorrected for the PMT response. For synchronous scans, a 50-nm offset was set between the excitation and emission monchromators.

RESULTS AND DISCUSSION

Figure 1 compares the fluorescence spectra of a cured EVA A9918 and a cured EVA 15295 to that of an uncured EVA A9918. The sample films were extracted with methanol to remove the stabilizers. For the uncured EVA A9918 film, the peak at ~260 nm range (curve 1) is primarily due to the emission of short α,ß-unsaturated carbonyls, $(C=C)_m$-C=O, where m=1 to 2 [10]. The uncured EVA 15295 has a similar emission spectrum. After curing by a fast process, the cured EVA 15295 shows an increase in the peak intensity and a shift of the peak position to 270 nm due to an increased concentration and conjugation of the carbonyls (curve 2). For the EVA A9918 cured by a typical (slow) process, a large emission peak at ~325 nm (curve 3) was observed. By combining the results from a series of UV-visible absorption measurements, the curing-generated chromophores are concluded to consist of a mixture of $(C=C)_m$-C=O and $(C=C)_n$, where $m \leq 5$ and $n \leq 6$ [10]. These results simply demonstrate FA's super analytical sensitivity and its applicability as a non-destructive analytical tool to monitor or control the quality of the polymer encapsulants.

When the cured EVA A9918, either as free-standing films or in encapsulated solar cells, is thermally or photothermally treated, the concentration of the chromophores and their conjugation length (i.e., m and n) increase as evidenced in Fig. 2. The film treated in an oven in the presence of acetic acid vapor to simulate the thermal degradation becomes yellow [11] and shows a large increase in the peak intensity at ~370 nm (Fig. 2a, curve 2). A similar peak intensity increase at 370 nm is also obtained for the EVA film laminated in a solar cell and exposed to a 1.8-KW Xe light source (Fig. 2b, curve 2). Accordingly, thermal and photothermal degradation of the EVA begins with an increase and lengthening of these chromophores. The dip at ~350 nm in Fig. 2b, curve 1, is due to quenching of Cyasorb UV 531 on the emission spectrum. Because the curing-generated chromophores in the cured EVA A9918 can be excited by UV light up to ~400 nm (Fig. 1, curve 3) and the UV absorption of the UV absorber, Cyasorb UV 531 is effective only up to ~360 nm, these chromophores can not be completely "shielded" from inducing photodegradation reactions [8,10]. This may account for the observations that PV modules encapsulated with EVA A9918 are prone to an earlier and faster photodegradation and discoloration than those encapsulated with EVA 15295.

Two types of chromophores can be clearly distinguished between the thermally and photothermally treated EVA A9918. In a simulated, accelerated degradation test by RS4 UV light over a period of 198 days at 85°C, the photothermally degraded EVA A9918 laminated in the c-Si and pc-Si solar cells shows a brown color and two emission peaks (one weak and one strong and broad), while the thermally degraded EVA A9918 shows a light yellow color and only the weak emission peak. The results, as shown in Fig. 3, indicate clearly that UV light is the main factor responsible for the EVA browning. The browned-EVA solar cells show a loss of 9%-13% in I_{sc} (short-circuited current) and 10%-19% in efficiency, while the light- yellowed-EVA solar cells show a loss of 0.5%-3.5% in I_{sc} and 2.5%-3% in efficiency [12]. The discoloration is due to the formation of long polyconjugated carbon-carbon double bonds (polyenes) on the EVA polymer chains as a consequence of deacetylation [8,10]. The extent of discoloration from yellow to dark brown is a direct measure of the extent of degradation and an indication of an increase in the length of the polyenes, producing a corresponding red shift of the emission peak position as illustrated in Fig. 4. The UV absorber in discolored EVA samples, which were taken from various weathering-degraded PV modules, was largely or completely depleted and the gel content substantially increased [8]. Greater power output losses from PV modules with darker EVA films are observed because of the greater degree of light absorption by the polyenes [9], which in turn also luminesces more strongly in the visible region [10].

Similar FA results are observed for the weathering-degraded PVB encapsulants in roof-top modules. Fig. 5 compares the emission spectra for a yellowed PVB and a browned PVB, showing the effect of discoloration extent on the emission peak intensity and position. The spectra are similar to those shown in Fig. 3 for the discolored EVA, indicating that similar polyenic chromophores were produced from the weathering. The initial PVB appears to be uncured (not cross-linked) during the module encapsulation step. However, an insoluble, yellow (or brown) thin layer was left from the front, sun-exposed surface side of the yellowed (or browned) PVB samples when the bulk was dissolved in methanol. These results, the same as observed on EVA, indicate that discoloration and cross-linking started from the top surface layers that were exposed to the sun light. Therefore, PVB underwent degradation mechanisms similar to those for the EVA.

CONCLUSIONS

In summary, fluorescence analysis is shown capable of serving as an analytical tool for quality control of the polymer encapsulants upon lamination, curing, and encapsulation processing. It is also very useful for monitoring the degradation and discoloration of the encapsulants by analyzing non-invasively the emission and/or excitation spectrum of the luminescent chromophores that change structurally upon thermal and/or photothermal oxidation.

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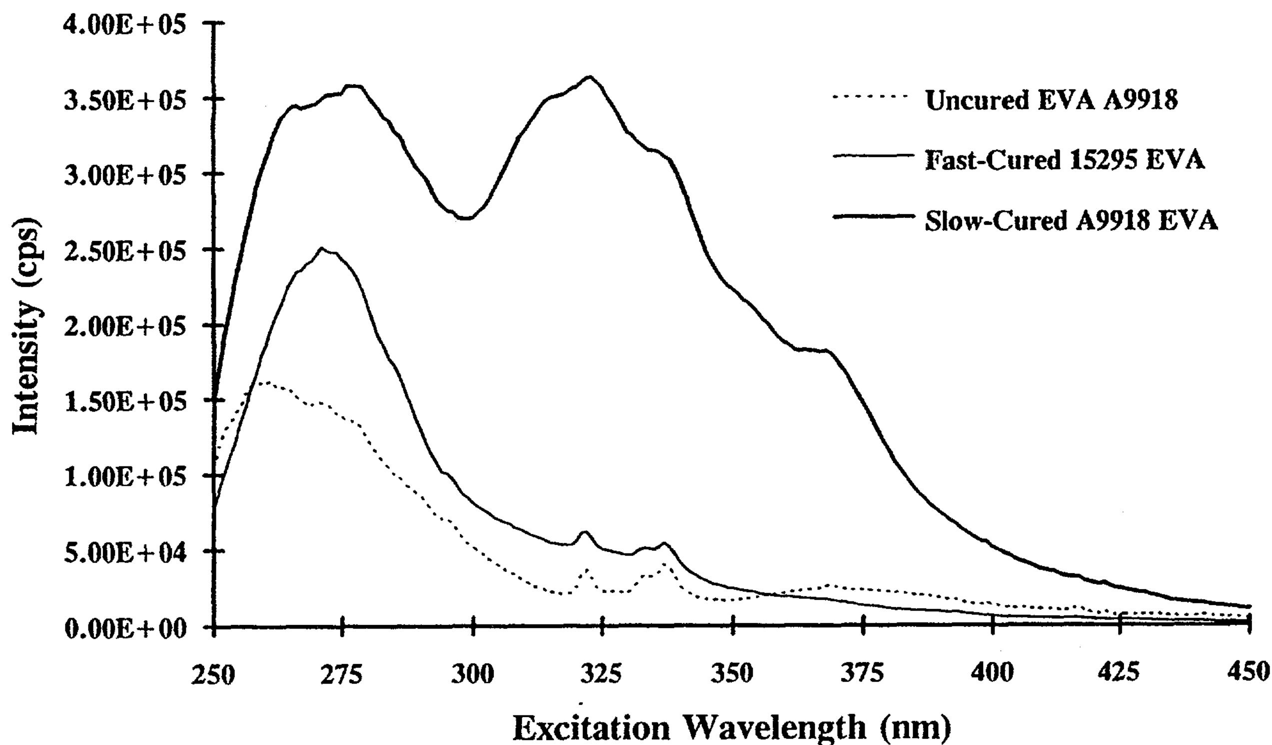

Fig. 1. Fluorescence spectra obtained by synchronous scans for the films of (1) an uncured EVA A9918, (2) a fast-cured EVA 15295, and (3) a slow-cured EVA A9918. The EVA films were extracted with methanol to remove the stabilizers before the analysis.

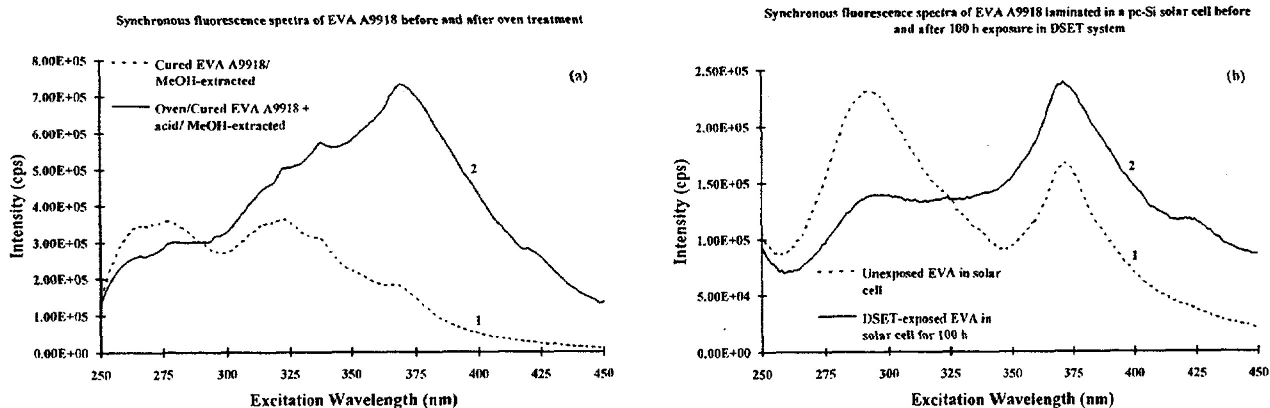

Fig. 2. Fluorescence spectra obtained by synchronous scans for (a) an EVA A9918 film before (curve 1) and after (curve 2) an oven treatment at 115°C in the presence of acetic acid vapor for 10 days, and (b) EVA A9918 laminated in a 5-cm x 10-cm (2-in x 4-in) polycrystalline Si solar cell before (curve 1) and after (curve 2) a 100-h exposure at 60°C ±3°C in a DSET Suntest CPS exposure system. The EVA films in (a) were extracted with methanol to remove the stabilizers before the analysis. The spectra in (b) were acquired directly through the glass superstrate.

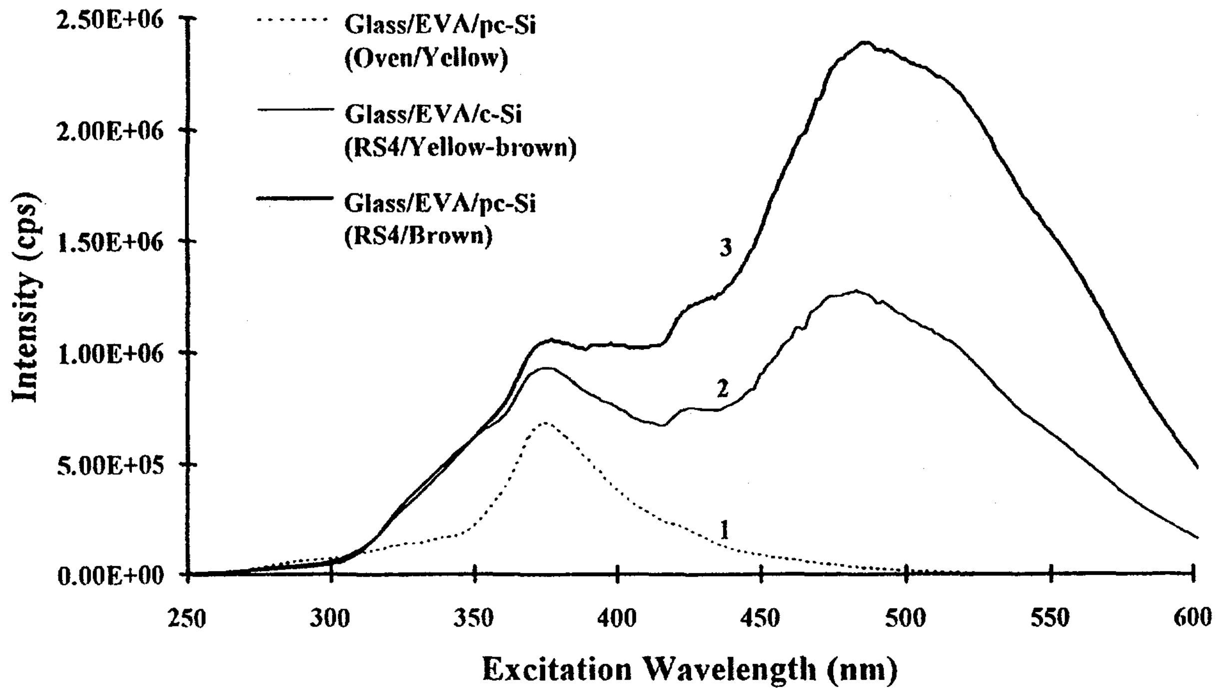

Fig. 3. Fluorescence spectra obtained by synchronous scans for EVA A9918 films laminated in solar cells heated in an oven in the dark and exposed to UV light (RS4 lamps) at 85°C ±2°C for 198 days. Curve 1: Oven-heated, light yellow EVA; curve 2: RS4-exposed, yellow-brown EVA; and curve 3: RS4-exposed, brown EVA. The spectra were acquired directly through the glass superstrate.

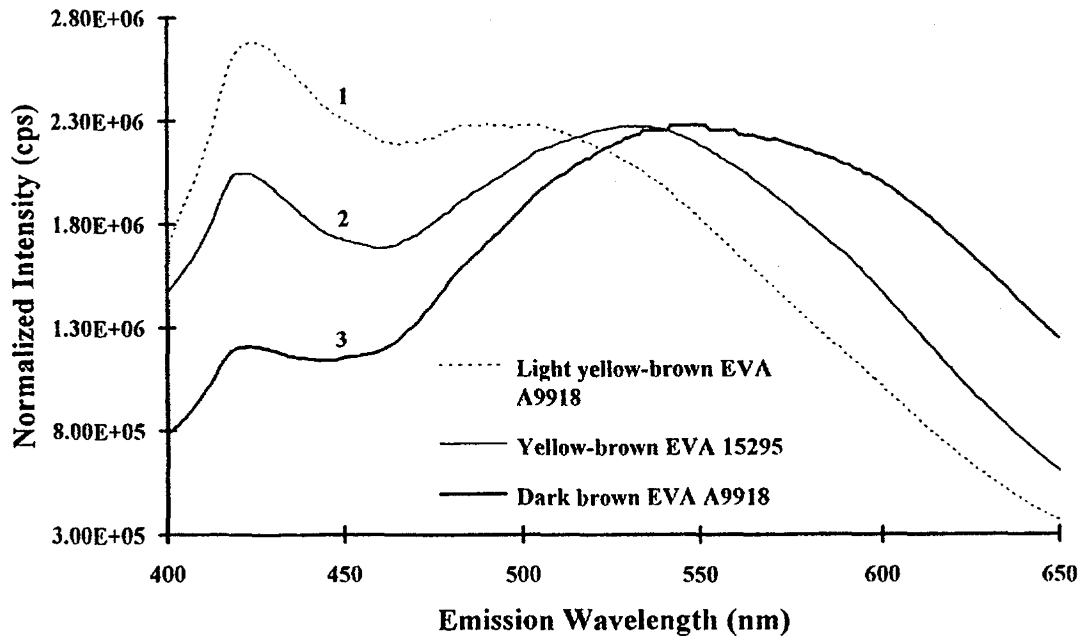

Fig. 4. Emission spectra for the weathering-degraded films of (1) a light yellow-brown EVA A9918, (2) a yellow-brown EVA 15295, and (3) a dark brown EVA A9918. The peak intensity in the 460-560-nm range was normalized for each spectrum to show the red shift of the emission peak as the discoloration increased. The excitation wavelength was 370 nm.

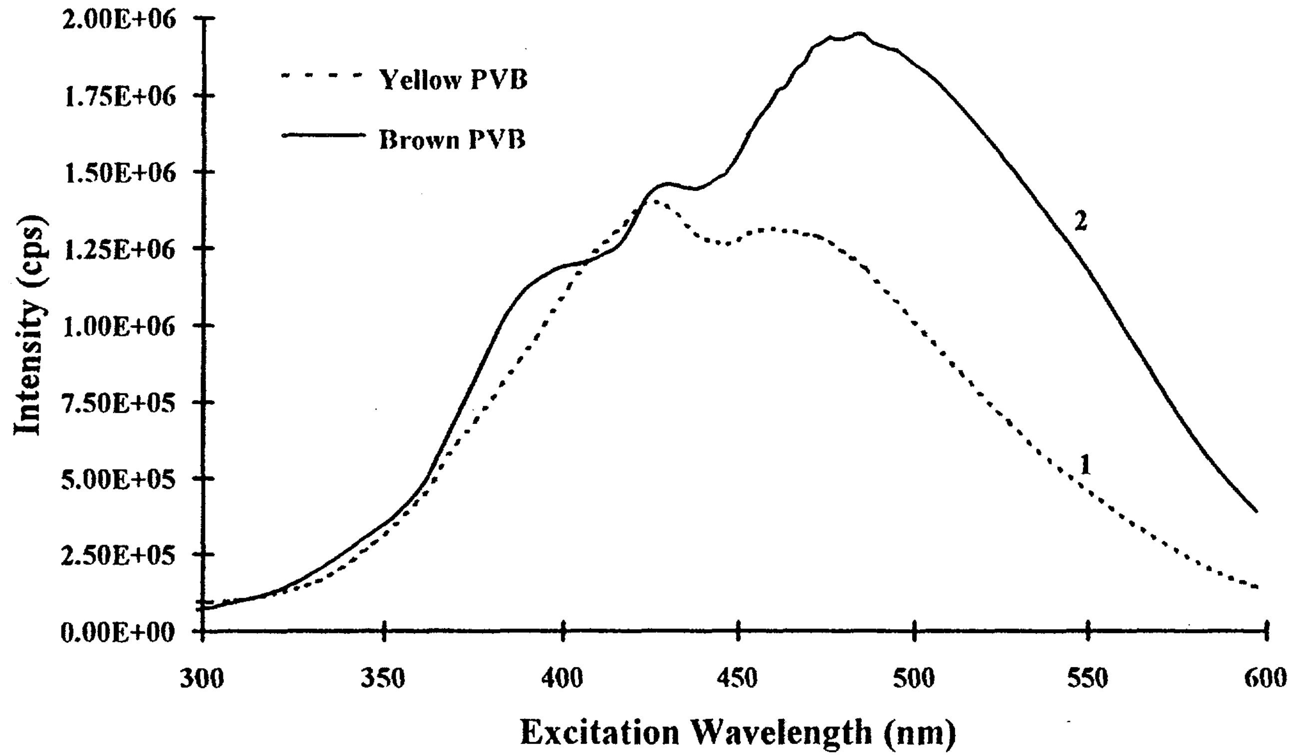

Fig. 5. Fluorescence spectra obtained by synchronous scans for (1) a yellow poly(vinal butyral), PVB, film and (2) a brown PVB film sampled from weathering-degraded roof-top PV modules.

RESULTS OF 1992 ASTM CELL AND MODULE MEASUREMENT INTERCOMPARISON

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ABSTRACT

Results of a cell and module measurement intercomparison, begun in June 1992, with eight U.S. laboratories participating, are presented. The intercomparison is sponsored by ASTM technical subcommittee E44.09, "Photovoltaic Electric Power Systems," for the purpose of obtaining inter-laboratory and intra-laboratory precision values for a number of important ASTM photovoltaic performance measurement standards. These standards include primary and secondary reference cell calibrations, cell performance measurements, spectral response measurements, and module performance measurements. Participating laboratories included PV manufacturers, the DOE national PV laboratories, and PV measurement equipment manufacturers.

INTRODUCTION

ASTM (American Society for Testing and Materials) is a well-known nonprofit organization devoted to the development of voluntary full-consensus standards for materials, products, systems, and services. Although ASTM standards are primarily used in the United States, they are also widely used and referenced throughout the world. ASTM standards are developed by technical committees whose members represent producers, users, consumers, and general interests. All participation by members is voluntary; therefore, standards developed by ASTM committees reflect the desires of organizations that feel that the content of standards is important for their business.

One special category of ASTM standards is test methods that produce numerical results. ASTM requires that such standards have a precision and bias statement that presents the results of an round-robin intercomparison (known as an interlaboratory study (ILS) in ASTM standard language) of the test method [1]. The primary purpose of the E44.09 ILS is to obtain the necessary data for precision and bias statements in several PV performance measurement standards. A secondary, but important, purpose is to use the intercomparison results to improve present measurement methods used throughout the photovoltaic (PV) industry.

ORGANIZATION OF ILS

Organization of the intercomparison was designed to provide the needed precision and bias information for the specific measurement standards covered by the ILS, titles and designations of which are listed in Table 1 [2]. The sample set, therefore, consisted of two groups—single solar cells and modules. Table 2 lists the complete sample set that was circulated among the participants; Table 3 gives the complete list of the participating laboratories. NREL functioned as the organizing agent for the ILS.

A wide variety of quantum efficiency curves were represented in the single cell samples, including single- and polycrystalline silicon, GaAs, and InP. Quantum efficiency (E 1021) measurements were performed on the single cell samples, and the results will be compared by calculating the spectral mismatch for a hypothetical *reference cell–simulator combination*. A *single-crystalline silicon* reference cell included with the sample set enabled all participants to perform the efficiency measurements (E 948 and E 1036) against a common reference. Because the single cell samples were all encapsulated with attached wires, differences due to contacting were eliminated. Thus, the results are indicative of the participants measurement systems and procedures, and not masked by using different reference cells and different contacting methods.

The module samples used commercial silicon panels. The module manufacturers also supplied production-line cells identical to the devices inside the module samples that were then included in the single cell sample set. Thus, quantum efficiency data for representative cells from the modules were available to the participants. Using these cells, spectral mismatch corrections could then be performed for the module efficiency measurements.

For the secondary reference cell calibrations (E 1362), the short-circuit current data from the cell I-V measurements were used to obtain the secondary calibration for each of the single-cell samples. Although the two primary calibration procedures were included in the ILS, it was not anticipated that more than one or two laboratories would be able to provide calibration data for the single-cell samples.

RESULTS

At the time this publication was prepared, the ILS was only 80% complete due to unavoidable delays. Therefore, the complete data set cannot be reported here. The reader will notice that there are different numbers of laboratories reported for the different portions of the ILS. This is because (1) some of the participants reported data from more than one measurement system; and (2) not all of the data has been delivered to the organizing agent as yet.

The results as reported by the participants were analyzed by calculating the mean for each sample, and then all data points were normalized by the mean value for the corresponding value.

Spectral Response/Quantum Efficiency

Quantifying differences between laboratories' results in past intercomparisons of cell spectral response has been difficult for two reasons. First, because the results consist of an array of values over a range of wavelengths, the lack of a single numeric quantity precludes using statistics to obtain the variability of the results. Second, many factors, such as cell active area and monochromatic illumination spot size, cause the absolute level of the responsivity to be highly variable from laboratory to laboratory. These problems have been overcome by the use of a reference spectral mismatch

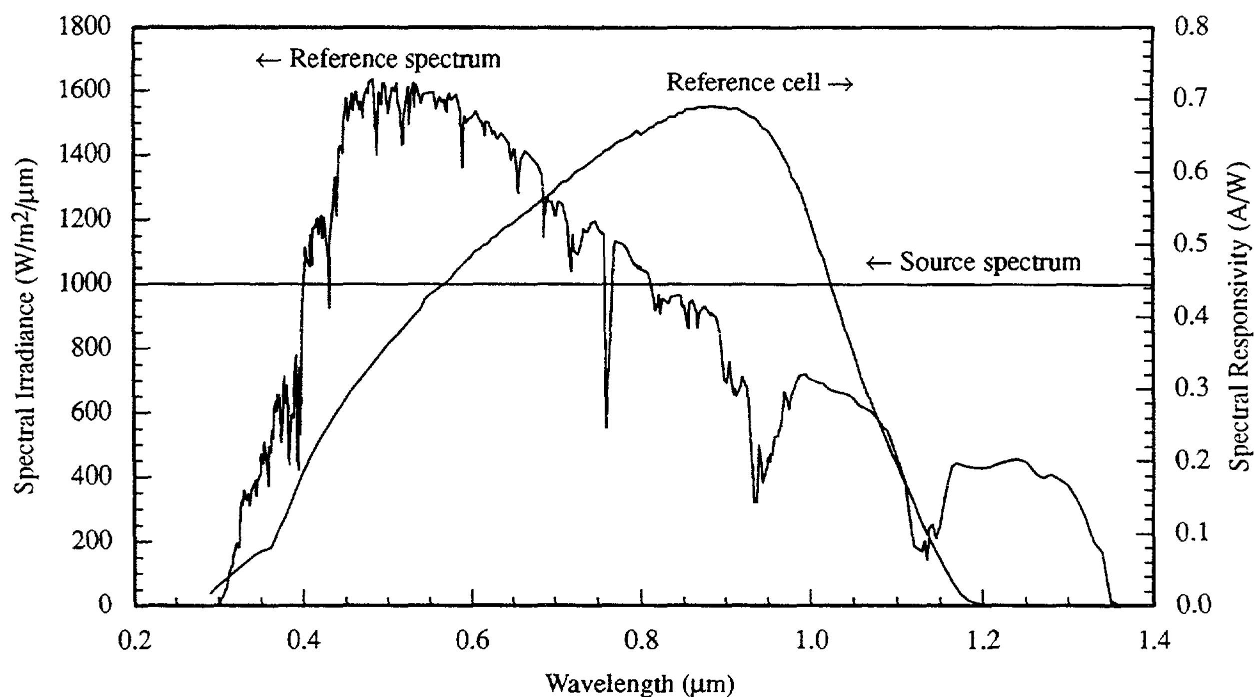

Figure 1. Reference spectral curves used for reference mismatch calculations.

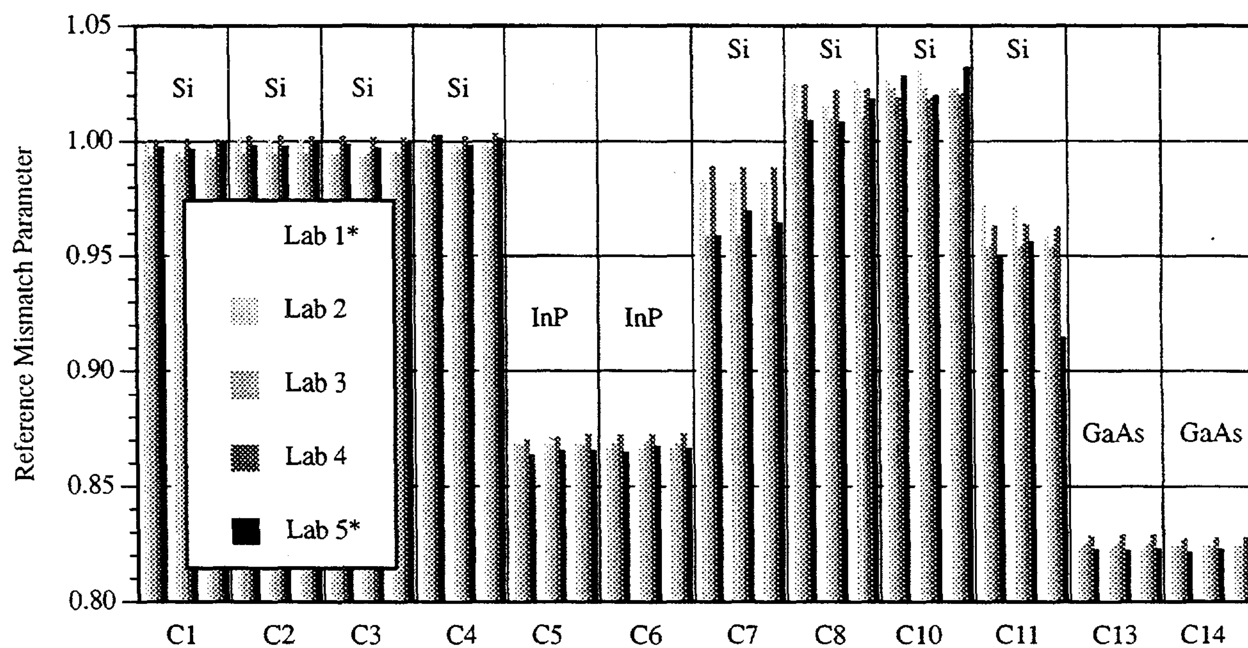

Figure 2. Reference mismatch calculation results of ILS. Laboratories marked with an asterisk did not measure spectral reponse beyond 1.1 µm.

calculation where the responsivity data are combined with a reference spectral irradiance, a reference source spectral irradiance, and a reference cell spectral response [3]. Using spectral mismatch for comparison of spectral response measurements is a new technique that produces a single numeric result for each spectral response measurement. This technique also overcomes the absolute value problem through normalization inherent in the spectral mismatch calculation. Figure 1 shows the three reference spectral curves that were used for the reference mismatch calculations. A flat-source spectral irradiance was chosen in order to prevent biasing the results toward any particular cell type. The reference cell is a high-efficiency silicon device.

Figure 2 shows the results of the reference mismatch calculation for five laboratories. The most obvious trend in Figure 2 is the much higher deviations polycrystalline silicon samples, on the order of 0.03. This difference is probably due to calibration errors in the measured infrared response at wavelengths greater than 1.0 µm. Because the single-crystal silicon samples matched the reference device in this region, these errors did not affect the results to the same degree as the polycrystalline silicon samples. The III-V samples were not affected because they do not respond in the 1.0 - 1.2 µm region. Also, several laboratories measured the quantum efficiency to only 1.1 µm, even though the responsivity of silicon does not go to zero until 1.2 µm. The 1.1 µm limit is due to the use of silicon photodiodes to measure the monochromatic light that have calibration curves that end at this wavelength. It should be noted that the ASTM standard for spectral reponse measurements, E 1021, specifies that the measurement range should include all wavelengths to which a device responds [4]. Therefore, these data were not made in strict accordance to the standard. In an attempt to reduce this discrepancy, a zero point was added at 1.2 µm. This procedure narrowed the difference considerably.

Single-Cell Performance

Figure 3 shows the normalized maximum power for the single-cell samples as measured by the participating laboratories. The maximum power, rather than the cell efficiency, was used to gauge the variability of the results in order to eliminate differences due to area. Also, several participants did not measure the areas of the samples. Aside from a few obvious outlier data points, the results show a lab-to-lab variation of about ±0.05, with one data set in particular, number 4, consistantly higher. These variations appear to be independent of the sample band gap, in contrast to the band gap-dependent errors shown by the spectral response results.

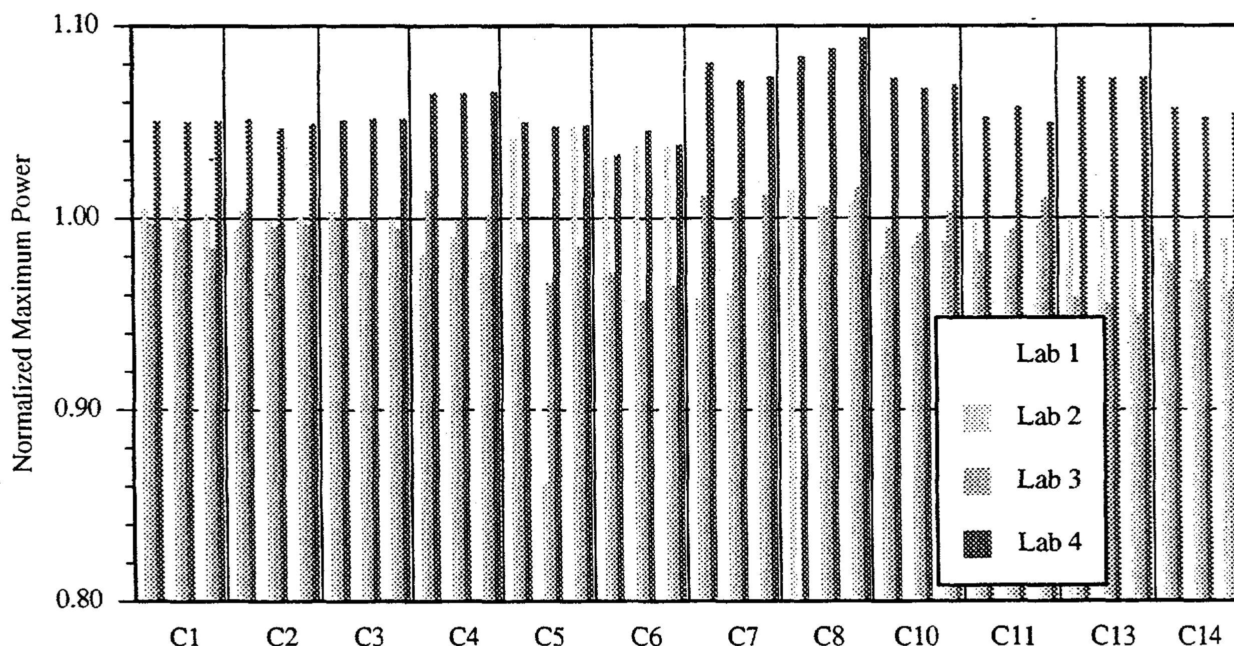

Figure 3. Normalized maximum power results of single-cell performance measurements..

Secondary Reference Cell Calibration

Results from the secondary reference cell calibrations are shown in Figure 4 for the 12 single-cell samples. The participants used the short-circuit currents measured during the cell performance measurements to obtain the calibration constants, in units of A/W/m2. Several outliers can be seen, and one laboratory, number 1, is consistantly low. Aside from these data points, the results are good, with lab-to-lab variations about ±0.01. The much lower variations for the short-circuit currents indicate that most of the errors in the cell performance measurements are in the maximum power point determination (variations of open-circuit voltage were very small—about ±1.5 mV).

Module Performance

Only three laboratories were able to provide module performance data in time for this publication. These data are presented in Figure 5. Laboratory number 3 is high by about 0.06 or more, while laboratories 1 and 2 are in agreement to within 0.01. Judging by the single-cell performance results, the difference here is probably again due to measurement of the module maximum power point.

Table 1. ILS test methods [4]. Test methods E 1039 and E 1125 were not performed by any of the participants.

E 948	Test Method for Electrical Performance of a Photovoltaic Cell using Reference Cells under Simulated Sunlight
E 1021	Test Method for Measuring the Spectral Response of Photovoltaic Cells
E 1036	Test Method for Electrical Performance of Non-Concentrator Terrestrial Photovoltaic Modules and Arrays using Reference Cells
E 1039	Test Method for Calibration of Silicon Non-Concentrator Photovoltaic Primary Reference Cells under Global Irradiation
E 1125	Test Method for Calibration of Primary Non-Concentrator Terrestrial Photovoltaic Reference Cells using a Tabular Spectrum
E 1362	Test Method for Calibration of Non-Concentrator Terrestrial Photovoltaic Secondary Reference Cells

CONCLUSIONS

An important conclusion that may be reached from this study is the importance of measuring the entire spectral response range of cells when the results will be used for spectral mismatch calculations. Also, the ±0.005 minimum normalized variation observed confirms empirical observations of several laboratories that correcting for spectral mismatch when the spectral mismatch M is within 1.00±0.01 does not reduce errors. This is because the magnitude of the correction is about the same size as the random variations in the spectral mismatch itself.

The results of the single-cell performance are somewhat disappointing, but they illustrate the need for carefull attention to detail in order to minimize errors in determinating the maximum power. Results of the module measurements show the need for intercomparisons with other laboratories as a check for errors that may not be apparent.

Table 2. ILS sample set.

C1-C4	Siemens single-crystal Si
C5-C6	NREL ITO/InP
C7	Westinghouse dendritic web Si
C8, C10	Mobil EFG Si
C11	Solarex polycrystal Si
C13-C14	ASEC GaAs/Ge
M1-M3	Solarex MSX-60 60 W polycrystal Si modules
M4-M6	Siemens M55 50 W single-crystal Si modules

Table 3 ILS participants.

- Solarex Corporation
- Sandia National Laboratories
- United Solar Systems Corporation
- Mobil Solar Energy Corporation
- Spire Corporation
- National Renewable Energy Laboratory
- Siemens Solar Industries
- Solec International

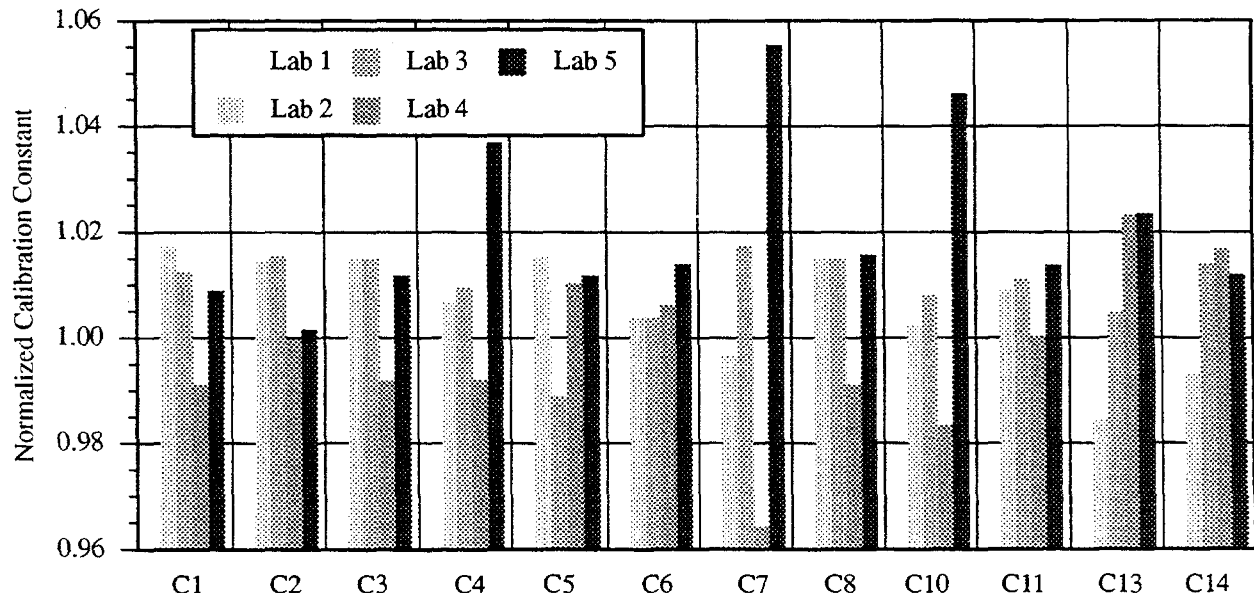

Figure 4. Normalized calibration constant results of secondary reference cell measurements.

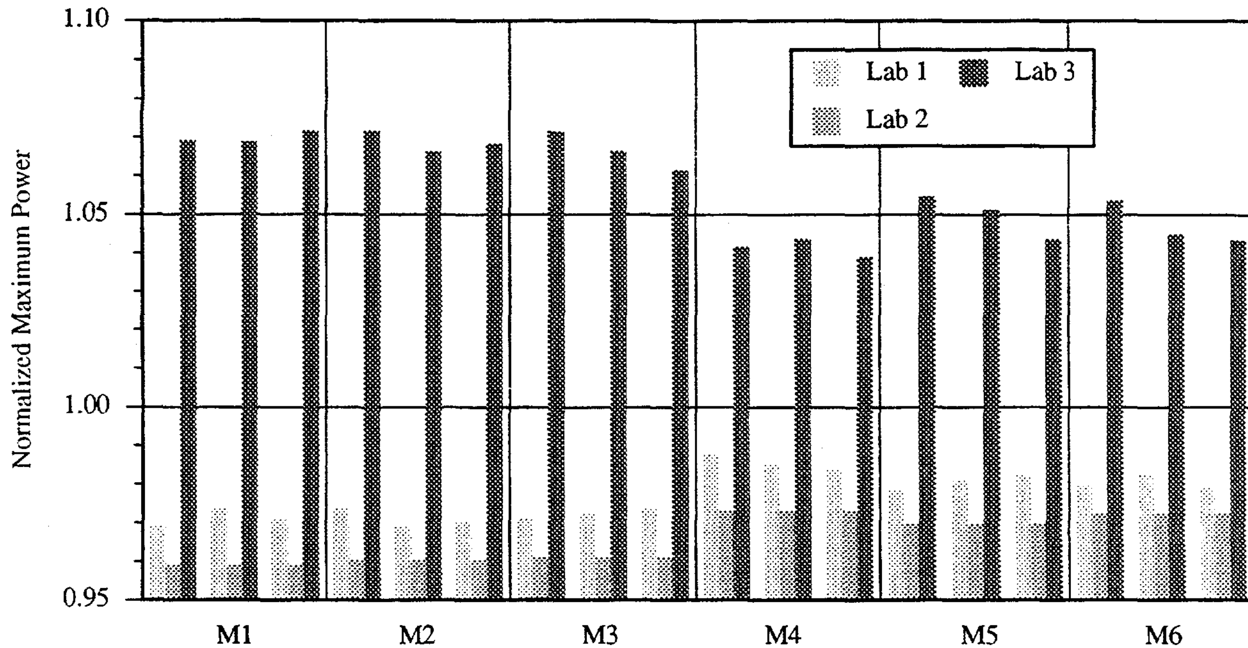

Figure 5. Normalized maximum power-point results of *module performance measurements.*

ACKNOWLEDGEMENTS

Many individuals contributed to the data presented here, including J. Wohlgemuth and D. Whitehouse of Solarex; D. King of Sandia National Labs; T. Glatfelter of United Solar Systems; R. Bell of Mobil Solar; S. Hogan of Spire Corp.; K. Emery, E. Beck, and A. Tennant of NREL; J. Anderson of Siemens Solar; and D. Anderson of Solec. Without the long hours and dedication spent by these and other people, this study would not have been possible. Spire Corp., in particular, did all of the encapsulation of the cell samples

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CdS/CdTe THIN FILM SOLAR CELLS ON LOW COST SUBSTRATES

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ABSTRACT

CdS/CdTe polycrystalline thin-film solar cells have been fabricated on tin oxide coated soda-lime glass substrates. CdS thin-films were grown from aqueous solutions and the CdTe by close-spaced sublimation. The influence of CdS thickness and the CSS deposition conditions were studied. A 10.6% efficient device was fabricated. The differences in the thermal properties of soda-lime and borosilicate glasses are compared and the process modifications for soda-lime glass substrates are discussed.

INTRODUCTION

CdS/CdTe polycrystalline thin-film solar cells have been produced by a variety of deposition methods. Close-spaced sublimation (CSS), also known as close spaced vapor transport, has been used very successfully by the University of South Florida group to fabricate a 15.8% efficiency device (1,2). The structure of the cell is as follows: borosilicate (Corning 7059) glass/ tin oxide/ thin CdS/CdTe/graphite doped with Hg or Cu. Transparent conducting tin oxide (SnO_2) is deposited by chemical vapor deposition, and CdS by chemical solution growth. One of the essential elements of this successful technology appears to be the borosilicate glass substrate (Corning 7059) itself. The possible reasons can be inferred from the thermal properties of borosilicate. The softening point of 7059 glass is in the range of 708°-815°C, and this permits the deposition of stress free, large grain CdTe films at 600°C. The coefficient of linear thermal expansion is $3.2\text{-}5.2\times10^{-6}/°C$ (3), and this matches that of CdTe, $5\times10^{-6}/°C$ (4). In terms of thermal and mechanical compatibility, borosilicate is an ideal substrate for CdTe.

However, for the low-cost production of solar modules, alkali soda-lime silicate glass (also called float glass) is used. Its softening point is in the range of 536°-696°C, and the expansion coefficient is $10.5\times10^{-6}/°C$ (3). Borosilicate glass is considerably more expensive than soda lime glass ($85 and $0.5, respectively, sq. ft), and this prohibits the use of borosilicate substrates for large scale production of thin-film modules. However, a comparison of the thermal and mechanical properties of soda-lime and borosilicate glasses shows that the former is somewhat inferior. The optimum conditions for the soda-lime glass must be chosen carefully to minimize the effects of thermally induced defects in the semiconductors. The high efficiency CdS/CdTe cells fabricated on borosilicate involve the deposition of CdTe at a substrate temperature of 600°-620°C, which appears to be too high for the soda-lime glass for reasons mentioned above. Also, one is concerned about the possibility of alkali diffusion at high temperatures. Keeping these considerations in mind, we have conducted a study of the CdS/CdTe junctions on soda-lime glass substrates. The results are reported in this paper.

EXPERIMENTAL

Our previous work on borosilicate substrates yielded a 11.3% efficient device (5), and the process remains essentially the same for the present work. The SnO_2 coated substrates used in this study were obtained from B. Mayer of Watkins-Johnson and they had a nominal sheet resistance of 10-12 Ω/sq. Thin CdS films were deposited from an aqueous solution of cadmium acetate, ammonium acetate, ammonium hydroxide and thiourea at 85°-90°C. A proper choice of the bath composition and other conditions, as described in ref. 1, allowed us to deposit uniform CdS films on 100 cm^2 substrates. Film thickness was in the range 60-150 nm. The quality of the CdS films is of utmost importance. The growth defects observed in CdS are: adhering particulates on the film surface, pinholes, and any colloidal particles trapped in the bulk of the film. The adverse influence of such defects is greatly enhanced at the CdTe deposition temperatures. Prior to the deposition of CdTe, the source-substrate combination was heated at 400°C in a hydrogen atmosphere for 15 min. A 3-8 µm thick CdTe layer was grown by CSS using the conditions described by Chu et al. (1). The samples were heated in an inert atmosphere containing oxygen at 400°C following a dip in $CdCl_2$ solution in methanol. The CdTe surface was etched in a bromine solution in methanol, and the graphite contact was applied and cured at 270°C. We have conducted a systematic study of the CSS deposition conditions and the subsequent device processing parameters to compare the effect of borosilicate and soda-lime glass substrates on CdS/CdTe solar cells. The variables in this study include CdS thickness (60-150 nm), CdTe thickness (3-8 µm), substrate temperature (520°-600°C), and the concentration and duration of the $CdCl_2$ dip. Substrate/source temperature difference and separation of 80°C and 0.2 cm respectively, and the reactor pressure of 0.666-12 kPa (5-90 Torr), were used. The source temperature and the reaction vessel pressure determine the sublimation rate of CdTe; the substrate-source temperature difference determines the deposition rate of CdTe; and the substrate temperature determines the microstructure of the CdTe films. At a fixed substrate temperature, the rate of deposition can be controlled over a wide range by adjusting the source temperature and/or reaction vessel pressure. The sublimation of CdTe was performed in an ambient of helium and oxygen to avail the benefits of oxygen as a dopant in p-CdTe.

RESULTS AND DISCUSSION

First, we discuss the effect of the CdS thickness on the device characteristics. We have used the dark current-voltage characteristics to identify the minimum CdS thickness that is necessary to produce devices without excessive shunting at the SnO_2/CdS/CdTe interfaces. An initial thickness of 150 nm yielded devices with good diode characteristics. When the CdS thickness was below 100 nm, the devices exhibited poor open circuit voltages. Analysis of the dark and illuminated current-voltage characteristics showed that the diode factor was as high as 3.0. The dark I-V curves exhibit a high current region for low forward bias voltages. These observations point toward a defective interfacial layer at the CdS/CdTe interface. A certain degree of intermixing occurs between CdS and CdTe during the CdTe deposition, and it appears as if the nature of this mixed layer is dictated by the substrate temperature and the CdTe deposition rate. The conditions for forming the optimum interface region must also take into account the role of $CdCl_2$ in recrystallizing the interface region. The validity and the exact implications of this hypothesis can be ascertained with more complete experimental data.

Under a given set of CSS conditions, CdTe films grown on CdS/SnO_2/soda lime glass react more vigorously with the $CdCl_2$ than those grown on CdS/SnO_2/borosilicate glass. Evidence for this is the appearance of local areas of discoloration when viewed through the glass. In the worst case, lifting of the CdTe layer due to a loss of adhesion was noted. The higher reactivity of CdTe films on soda-lime substrates is presumably related to the higher thermal stress in the films and the diffusion of impurities from the soda-lime glass substrate.

The photoluminescence (PL) lifetime of the CdS/CdTe junctions has been studied. Figures 1 and 2 show the PL decay curves for devices fabricated on borosilicate and soda lime glass substrates, respectively. The decay curve for the borosilicate case shows a rapid initial decay and virtually no tailing for

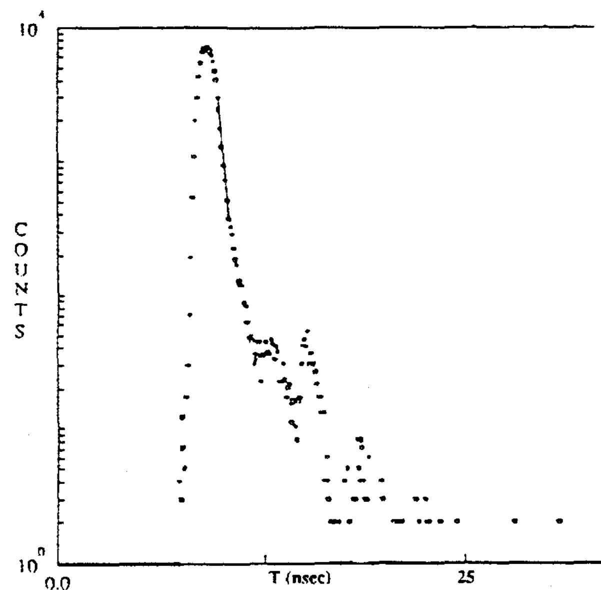

Fig. 1. PL decay of a CdS/CdTe cell on borosilicate. Substrate temperature, 600°C. Excitation through glass.

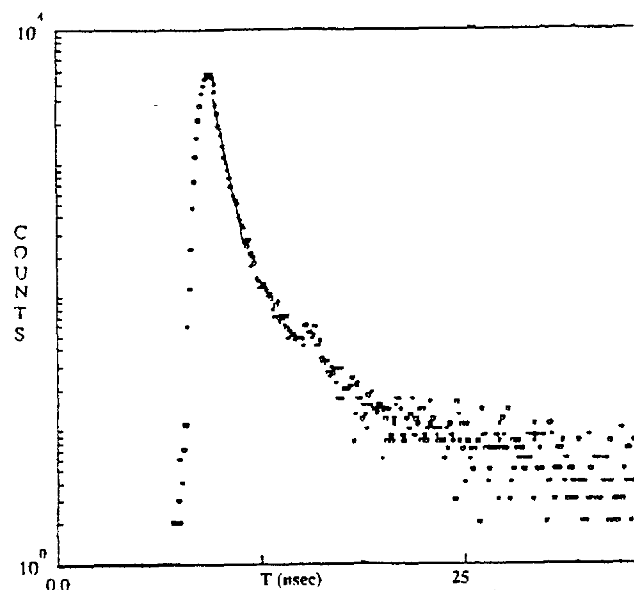

Fig. 2. PL decay of a CdS/CdTe cell on soda lime glass. Substrate temperature, 580°C, excitation through glass.

longer times. The soda lime sample exhibits the initial decay and a long tail. The latter is indicative of deep trapping states in the CdTe energy gap. The precise origin of these states or their identity has not been established. It is reasonable to speculate that the defects may be thermal in origin. This aspect needs further study.

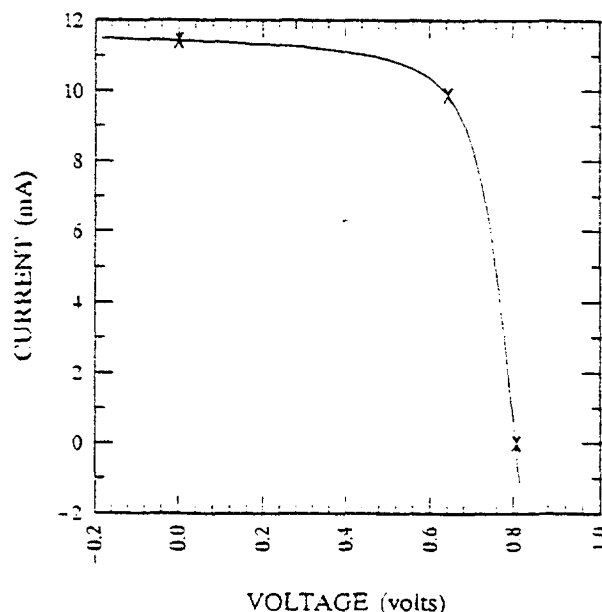

Fig. 3. Light I-V characteristics of a CdS/CdTe cell. Global 1.5. 100 mW/cm^2. Area = 0.6 cm^2. V_{oc} = 0.807 V, J_{sc} = 19.03 mA cm^{-2}, fill factor = 0.69, efficiency = 10.6%

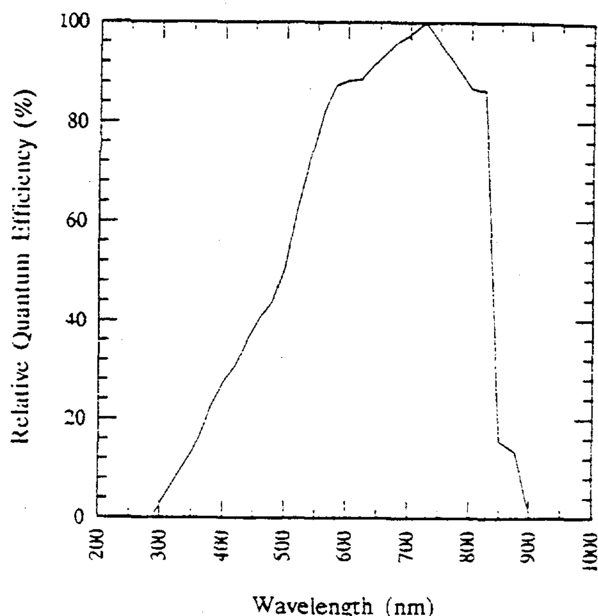

Fig. 4. Quantum efficiency of the device shown in Fig. 3.

The photovoltaic characteristics of the best CdS/CdTe cell fabricated on soda lime glass is shown in Figure 3. The quantum efficiency is shown in Figure 4. The major loss is in the current density. The short wavelength collection is limited by absorption in the thick CdS layer. The roll off in the long wavelengths is due to a poor diffusion length in the absorber: the $CdCl_2$ incorporated was insufficient to fully optimize the CdTe properties. Improvements can be made by reducing the CdTe thickness to 3-4 μm and by choosing the appropriate heat treatment conditions.

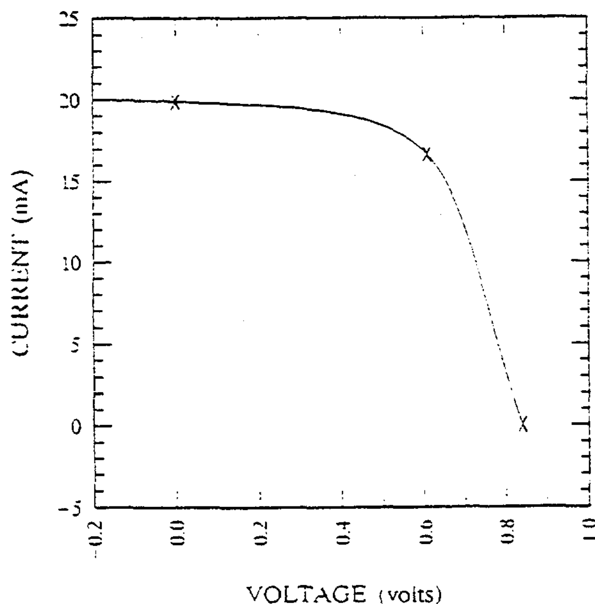

Fig. 5. Light I-V characteristics of a CdS/CdTe cell. Global 1.5. 100 mW/cm^2. Area = 1.0 cm^2. V_{oc} = 0.841 V. J_{sc} = 19.92 mA cm^{-2}. fill factor = 0.60. efficiency = 10.1%

The current-voltage characteristics of another device, shown in Figure 5, *indicates that superior devices can be fabricated on* soda lime glass substrate. The V_{OC} of the cell is 0.841 V, and this is comparable to the best values reported (2). Work is under way to fully optimize the film thicknesses and the process parameters.

CONCLUSIONS

CdS/CdTe thin film solar cells were fabricated on soda-lime glass substrates. The differences between borosilicate and soda-lime glass substrates have been identified, and an attempt has been made to find out if these considerations have an effect on the device characteristics. The conclusions are preliminary and further study is required to establish whether or not the soda-lime substrate can function as well as the borosilicate. The devices obtained so far indicate that the efficiencies can be improved to 13%-14% range in the near term.

ACKNOWLEDGMENTS

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OPTICAL PROCESSING: A NOVEL TECHNOLOGY FOR FABRICATING SOLAR CELL CONTACTS

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ABSTRACT

A novel semiconductor device processing technology is described that uses optical energy of a preselected spectrum to produce local melting at an illuminated semiconductor-metal (S-M) interface. This local melting results in an alloyed ohmic contact of very low contact resistivity. This process (called Optical Processing) takes place in a "cold wall" furnace, and is very insensitive to impurity contamination. We describe the application of Optical Processing to the formation of low-resistivity contacts on the front and back sides of a silicon solar cell in a one-step process. This process can result in considerable cost savings compared to conventional approaches for fabricating contacts on solar cells.

INTRODUCTION

Fabrication of low-resistance metal contacts on solar cells requires sintering and alloying of the S-M interfaces to produce the desired ohmic characteristics. In the fabrication of a typical n+/p solar cell, the back contact must by alloyed to have a low-resistivity contact on the higher-resistivity base region, while the front contact must be only mildly sintered to prevent metal from punching through the highly doped emitter and the depletion regions. The need for different processing conditions for the front and back contacts necessitates several process steps, the number depending on the method of metal deposition (e.g., plating, screen printing, or evaporation). In commercial silicon cells the contacts are fabricated by screen printing using Ag-based paste for the front (junction) side and Al-based paste for the back side. This procedure consist of first alloying the back contact by firing at about 800°C and then forming the front contact at a lower temperature. This process sequence typically requires six to eight steps that, in conjunction with the high cost of Ag, makes it difficult for this process to meet the criteria of a low-cost cell fabrication technology [1].

Laboratory studies have shown that the use of thin films of Al, Cu, and Ni (with a Pd barrier in some cases) deposited by standard techniques such as plating, vacuum or sputter depositions, can produce good contacts [2]. This approach requires a less-expensive second metallization, such as a solder dip, be performed to obtain a satisfactory low value of sheet resistivity (ρ_S) of the metal. However, this type of process is not commercially used because it would require many steps by conventional processing techniques [3]. As an example, Table 1 shows the typical steps involved in a conventional process using evaporated aluminum to make contacts on both sides.

This paper describes a new technology, called Optical Processing, that can simplify contact fabrication. It allows the formation of extremely low resistance contacts on both sides of a silicon solar cell to be carried out in one step. Advantages of this technology are described later in the paper.

OPTICAL PROCESSING

Optical Processing uses spectrally selected light to create a local melt at an illuminated S-M interface. The thickness of the melt can be controlled by controlling the energy delivered to the device. This local melt forms an alloyed region that regrows epitaxially on the silicon substrate to form an ohmic contact of extremely low contact resistivity. The energy delivered to the cell can also produce bulk heating to induce other predetermined thermal effects. The interface reaction is strongly diminished if the S-M interface is not directly illuminated. The following example describes the use of Optical Processing for the simultaneous formation of front and back contacts on a solar cell.

Figure 1 illustrates the structure of an n+/p solar cell which has a thin layer of Al deposited on the entire backside and narrow Al pads on the front side. In order to produce high quality contacts to the cell, the back contact must be alloyed without alloying the front. To accomplish this, the cell is placed in an Optical Processing Furnace (OPF) with the junction side upward, as shown schematically in Figure 2. The OPF consists of a quartz muffle that is illuminated from above by quartz-halogen lamps. The optics of the light sources are designed so that the illumination in the process zone is highly uniform. Process gases such as Ar, N_2, and O_2 are regulated to flow through the furnace. The walls of the muffle are maintained "cold" by flowing N_2 along the outside walls of the muffle. The spectrum, intensity, and duration of the incident flux are chosen for the specific application. Figure 3 shows typical process cycles using Al contacts for silicon solar cells with and without antireflection coating. As seen from this figure, the process is controlled in terms of the optical power delivered to the device.

Optical Processing and Rapid Thermal Annealing (RTA) differ in the basic mechanisms involved. In Optical Processing, the reaction occurs predominantly at the illuminated interface; the same reaction is greatly slowed if the interface is masked. In contrast, a typical RTA is a thermal process that cannot discriminate between the front and the backside of the cell since such a process is completely thermally controlled [4].

RESULTS

The Optical Processing cycles described in Figure 3 produce a melt at the back interface, resulting in the formation of an Al-rich Si-Al alloy. The front Al-Si interface remains abrupt without any significant alloying. By controlling the light intensity, the spectral content of the incident light, and the process time, one can control the thickness of the alloyed back layer and the sinter conditions for the front contact simultaneously. Figure 4 schematically illustrates the effects of Optical Processing on the front and back interfaces of a solar cell. While the front contact does not show the presence of an alloyed region, the back contact forms a thin Si-Al alloyed region adjacent to the Si surface. Figure 5 is a high resolution cross-sectional TEM image of the Si/Si-Al alloy interface showing an epitaxial growth of the alloy.

In order to compare the degree of reaction at the front and the back side of the cell we have processed a sample under accentuated conditions. Figures 6 and 7 show the Al and Si SIMS profiles of these "strongly" processed contacts before and after removal of the residual Al. Figures 6a and 6b show that the back contact has melted to produce an alloyed interface region of about 0.4 μm. However, Figures 7a and 7b show that the front contact has an alloyed region of << 0.1 μm. It is important to point out that under normal process conditions the alloyed interface thicknesses are considerably smaller than those in Figures 6 and 7.

The quality of the contacts formed by Optical Processing is extremely high. From the initial measurements of contacts fabricated on 0.5-10 Ω-cm substrates, we have estimated the contact resistivity to be less that 10^{-4} Ω-cm^2, up to current densities of 2 A/cm^2. As a result, solar cell contacts made by Optical Processing have proved excellent. Figure 8 shows the I-V characteristic of a large-area 32 cm^2 cell with contacts produced by this technique. The efficiency of the cell is slightly above that for the same cell with contacts made with conventional process steps. Even already fabricated contacts on fully finished commercial cells have been improved using Optical Processing.

Although we have only discussed forming Al contacts on both sides of a cell, the same principle is applicable to many other metals and combinations of metals. We have used other metals, such as Cu, Ni, and Pd, in various combinations with excellent results.

ADVANTAGES OF OPTICAL PROCESSING

• Since heating/melting initiates at the interface (and can be confined to a thin region at the interface), the effect of the impurities in the ambient gas(es) on the characteristics of the contact is minimal compared to either furnace processing or Rapid Thermal Annealing (RTA). In Optical Processing the surfaces of the Al contacts typically remain shiny and do not require further preparation for additional metallization, such as solder dip.

• Optical Processing is a "cold wall" process, which minimizes the impurity out diffusion as well as permeation from furnace walls.

• The process results in large-area uniformity of the alloyed/sintered layers. This feature is evidenced by the fact that the Si-Al contacts produced are free from the "spikes" and pitting produced by other processes.

• The process requires much less power than furnace or RTA anneals (particularly when the cell has an anti-reflection coating).

• The process is rapid, has high throughput, and can make devices with unique characteristics.

• The process requires fewer steps than conventional approaches and results in significant cost savings.

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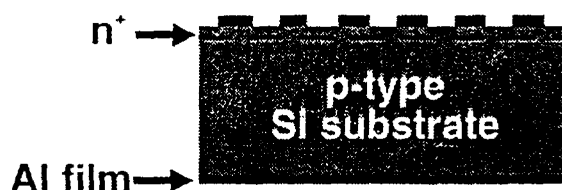


Figure 1. Schematic of the solar cell configuration used for simultaneous contact formation by Optical Processing

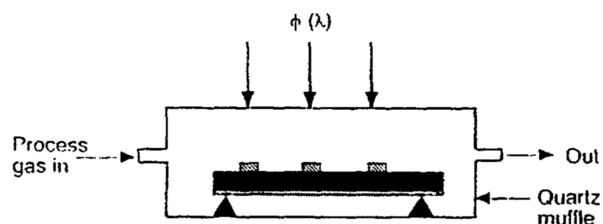


Figure 2. Illustration of the use of Optical Processing for simultaneous formation of the front and back contacts

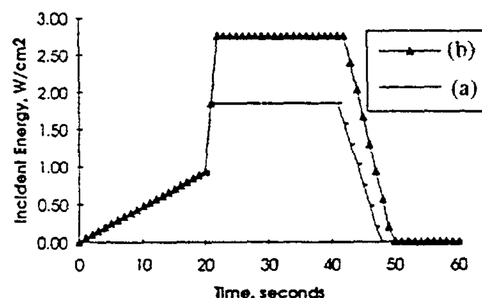


Figure 3. Typical process cycles for forming Si-Al contacts: (a) with AR coating; (b) without AR coating

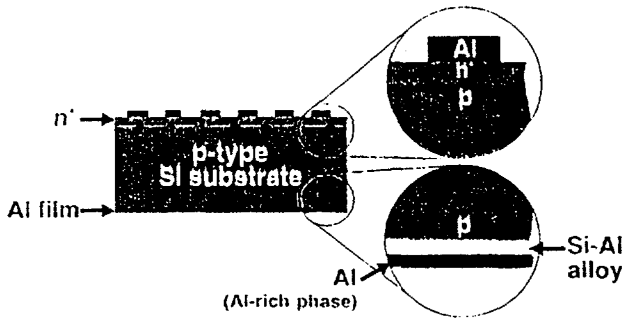


Figure 4. Illustration of the interface structure produced by Optical Processing.

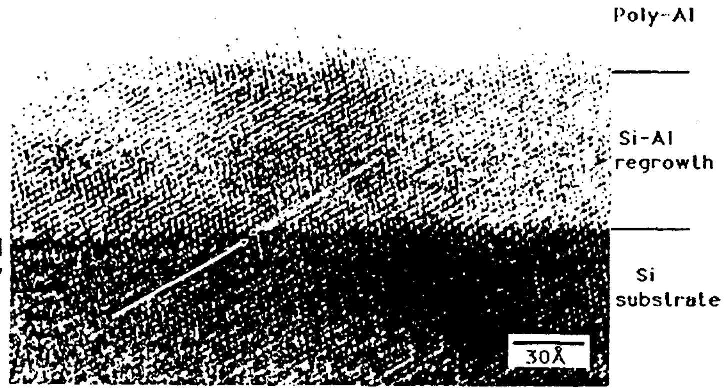
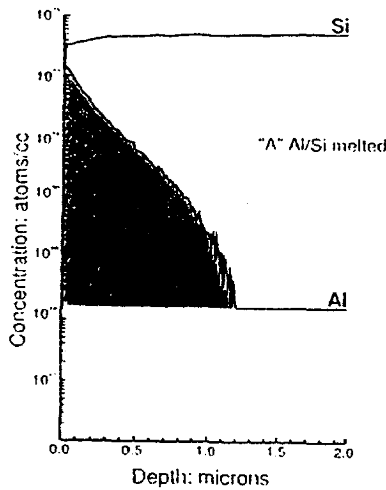


Figure 5. High resolution XTEM image of the Si/Si-Al alloy, showing epitaxial growth of the alloy on the substrate.



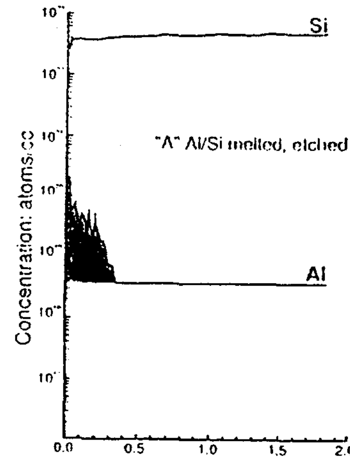
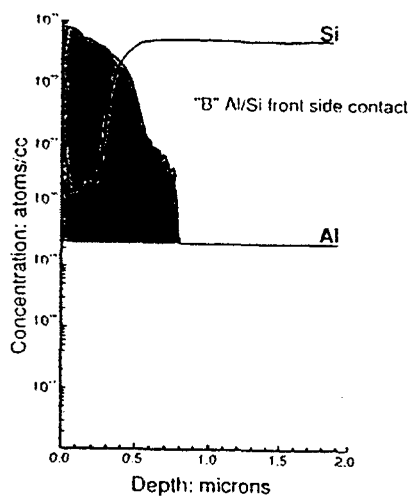


Figure 6. SIMS profiles of Al and Si on the backside contact of a "strongly" processed sample: (a) as-formed; (b) after residual Al was etched



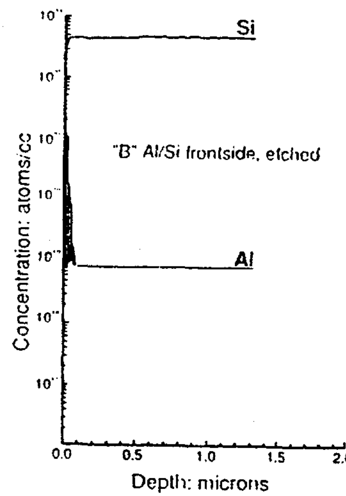


Figure 7. SIMS profiles of Al and Si on the front contact of a "strongly" processed sample: (a) as-formed; (b) after residual Al was etched

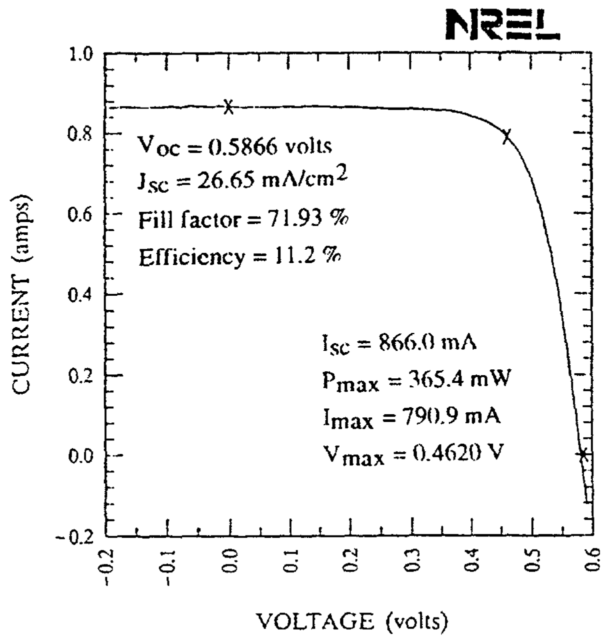


Figure 8. I-V characteristic of a 32.5 cm cell with contacts formed by Optical Processing.

Table 1: Comparison of process steps for fabricating contacts to solar cells using conventional methods and Optical Processing (this example uses Al on both sides).

	FURNACE ANNEAL OR RTA	OPTICAL PROCESSING
1	Deposit Al on back side	Deposit Al on front and back
2	First alloy	Sinter/alloy
3	Strip excess Al in HCl then Rinse in DI water; dry	
4	Dil. HF dip (or fume)	
5	Deposit Al on front	
6	Sinter front Al	
7	Deposit additional Al on back	

OPTICAL CONFINEMENT IN THIN SILICON FILMS: A COMPREHENSIVE RAY OPTICAL THEORY

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ABSTRACT

This paper describes a ray-optics theory to analyze optical confinement in silicon solar cells using random or periodically rough surfaces. This theory considers multireflections within the cell. It also takes into account polarization and interference effects to include antireflection coatings and local non-normal incidence of light. The results are given in terms of parameters such as reflectance, transmittance, and absorbance for Global AM1.5 illumination. A variety of thin-film structures, suitable for light trapping, are compared in terms of the maximum achievable current densities. The paper emphasizes optical concepts that are necessary to design thin-film solar cells using non-planar interfaces.

INTRODUCTION

Silicon solar cells using thin-film configurations are expected to yield higher performance than their thick-substrate counterparts by reducing the bulk recombination. One of the essential elements in this anticipated advantage is that optical confinement (or light trapping) must be implemented to increase the effectiveness of the silicon film as an optical absorber. Unfortunately, the optics of rough/textured surfaces, necessary to analyze light trapping, are difficult to handle in a convenient form. A number of papers have appeared early-on that address light trapping in thin silicon films using heuristic arguments (1-3). More recent work has applied ray optics in a limited form to derive some valuable results and develop a deeper understanding of the light trapping (4-6). However, these analyses also used approximations, such as constant values for reflection and transmission coefficients (i.e, independent of local angle of incidence and wavelength). Thus, the effects of antireflection (AR) coatings, and polarization associated with non-normal incidence of light, have been ignored. Currently, there continues to be a lack of understanding about a variety of issues related to light trapping that hamper proper cell design. These issues include

1. Distribution of the absorbed photon flux through the thickness of a thin cell, especially when the texture size is a significant fraction of the cell thickness;
2. Design features that can minimize the junction area, and yet, produce effective light trapping;
3. A physical understanding of the concepts of light confinement that can allow thin cell design to be carried out in a phenomenological manner.

We have extended the ray-optics theory (applicable to films with textures and thicknesses greater than several microns) to include interference and polarization effects. We have explicitly included features that can allow optimization of AR coatings, size and shape of texture, and the back-surface reflectors. This paper is aimed at using the results of this analysis to develop a physical insight for various concepts of optical confinement, and to allow researchers who are less involved in optics to acquire a sound working knowledge of the light-trapping mechanisms and their effects. The present analysis also provides results that can be directly used to compare the effectiveness of various light-trapping schemes in terms of the maximum achievable current density (MACD) they can produce. The analysis is extended to include encapsulated cells that allow a comparison of cell performance in the air and in the module. These results can be easily incorporated into the cell model PC1D.

FORMAT OF CALCULATIONS

Figure 1 illustrates the approach of our modeling. An optical beam illuminates a silicon solar cell with a rough surface that may be random or periodic. The light is normally incident on the "average surface" plane. Our analysis includes up to two layers of AR coating on the cell; these are referred to as mediums 1 and 2 in the figure. We assume that incident light is unpolarized and, hence, can be equally split into parallel and perpendicular components. The structure of the silicon surface is described by planes; for example, rounded peaks of a textured surface are fitted by means of planar interpolation. The total reflectance, absorbance, and transmittance of the incident beam is determined by splitting the incoming plane-wave into beamlets. Each beamlet is treated as an optical ray that propagates from the air into the cell and is multireflected until nearly all (99.9%) of the energy is depleted by the absorption in the cell or is radiated back into the air. The reflection and transmission characteristics (including magnitude and direction) are determined at each interface (7). The following equations are used when the beamlet enters an interface:

$$\cos(\theta_0) = \hat{r}_i \bullet \hat{n} \tag{1}$$

$$j = 1,2,3 \tag{2}$$

$$\cos(\theta_j) = \sqrt{1 - (\frac{n_{j-1}}{n_j})^2 \cdot (1 - \cos(\theta_{j-1})^2)} \tag{3}$$

The reflection coefficients for parallel and perpendicular polarization are

$$r_{\perp} = \frac{r_{1\perp} + A_{\perp} \cdot e^{-i\frac{4\pi}{\lambda} n_1 t_1 \cos(\theta_1)}}{1 + r_{1\perp} \cdot A_{\perp} \cdot e^{-i\frac{4\pi}{\lambda} n_1 t_1 \cos(\theta_1)}} \tag{4}$$

$$r_{\parallel} = \frac{r_{1\parallel} + A_{\parallel} \cdot e^{-i\frac{4\pi}{\lambda} n_1 t_1 \cos(\theta_1)}}{1 + r_{1\parallel} \cdot A_{\parallel} \cdot e^{-i\frac{4\pi}{\lambda} n_1 t_1 \cos(\theta_1)}} \tag{5}$$

where

$$A_{\perp} = \frac{r_{2\perp} + r_{3\perp} \cdot e^{-i\frac{4\pi}{\lambda} n_2 t_2 \cos(\theta_2)}}{1 + r_{2\perp} \cdot r_{3\perp} \cdot e^{-i\frac{4\pi}{\lambda} n_2 t_2 \cos(\theta_2)}} \tag{6}$$

$$A_{\parallel} = \frac{r_{2\parallel} + r_{3\parallel} \cdot e^{-i\frac{4\pi}{\lambda} n_2 t_2 \cos(\theta_2)}}{1 + r_{2\parallel} \cdot r_{3\parallel} \cdot e^{-i\frac{4\pi}{\lambda} n_2 t_2 \cos(\theta_2)}} \tag{7}$$

$$r_{j\perp} = \frac{n_{j-1} \cdot \cos(\theta_{j-1}) - n_j \cdot \cos(\theta_j)}{n_{j-1} \cdot \cos(\theta_{j-1}) + n_j \cdot \cos(\theta_j)} \tag{8}$$

$$r_{j\parallel} = \frac{n_{j-1} \cdot \cos(\theta_j) - n_j \cdot \cos(\theta_{j-1})}{n_{j-1} \cdot \cos(\theta_j) + n_j \cdot \cos(\theta_{j-1})} \tag{9}$$

$r_{\perp}$ and $r_{\parallel}$ are the field reflection coefficients at the interface, and n is the real part of the refractive index.

Each beamlet propagates in the silicon cell with an intensity absorption coefficient.

$$I_{final} = I_{initial} \cdot e^{-\alpha z} \tag{10}$$

$$\alpha = \frac{4 \cdot \pi \cdot k}{\lambda} \tag{11}$$

$$n(\lambda) = n - i \cdot k \tag{12}$$

Here $n(\lambda)$ is the complex refractive index, and k is the extinction coefficient. We determine the path of each beam, the angle at which the beam is reflected/transmitted at each interface during multireflections, and the total absorption along an elemental path within the cell. From these data, we calculate the total reflection at the air-cell interface, the distribution of the photon absorption, and the total absorption within the cell. The values of n and k are taken from ref. 8. In the cases of evaluating polarization effects, each polarization component and polarization conversion is considered at each reflection. We have found, however, that use of reflectance values averaged for TE and TM polarizations yield accurate results, and reduces the calculation time.

For a 180° symmetric surface structure and using average polarization,

$$R = \frac{|r_{\perp}|^2 + |r_{\parallel}|^2}{2} \tag{13}$$

We have used this methodology to analyze a variety of light trapping structures involving combinations of periodic and random surface structures with or without encapsulation, optimized AR coatings, and other suitable back-side optical reflectors. The calculations are performed using 2-D and 3-D analyses. 2-D calculations are performed simply to save computational time in such cases where 2-D and 3-D can give nearly same results (e.g., when the surface texture has 180° rotational symmetry).

RESULTS

We will first describe results of 2-dimensional analysis for some important structures. Next, some results of 3-dimensional analysis will be presented. The objective of these separate calculations is to show that, in most situations, the 2-dimensional analysis, which takes considerably less computing time, can suffice.

Results of 2-Dimensional Analysis

In the following, we summarize some of the results that demonstrate the capabilities of our analyses.

1. Figure 2 illustrates basic calculations of the reflectance, absorbance, and transmittance of a cell of thicknesses 250 µm. This cell had a textured front with texture size of 2 µm, an AR coating consisting of 710 Å of Si_3N_4 (n=1.95) on 100 Å of SiO_2, and a polished back side. The SiO_2 layer was included in the AR coating for surface passivation. When the absorbance is weighted with a Global AM1.5 spectrum, the total number of photons absorbed within the cell is determined to be 2.52 x 10^{17}/cm^2. For comparison, similar calculations performed for a 50 µm thick cell, with the same front and back surface characteristics, yield the absorbed photon flux of 2.35 x 10^{17}/cm^2. These values of the absorbed flux correspond to maximum achievable current densities (J_{sc}) of 40.47 mA/cm^2 and 37.59 mA/cm^2, respectively. The value of J_{sc} for a thick textured cell (of unknown texture size), as determined in refs. 5 and 6, are 40.11 and 39.5 mA/cm^2, respectively- both lower than our value of 40.47 mA/cm^2. We believe that the higher value obtained in our analyses is the result of the optimized AR coating. However, for the thinner cell our value of J_{sc} agrees well with that calculated in ref. 5.

2. It is instructive (as well as important for calculation of cell characteristics) to determine the distribution of photons within the thickness of the cell. Figures 3a and 3b show these distributions of absorbance (per unit area, per µm of thickness) for the cell of Figure 2, and the thinner cell (50 µm) discussed above. The distributions are shown for different wavelengths and are normalized with respect to the incident flux. {It is important to point out that the zero absorbance at the surfaces is the result of averaging the flux density at the textured or randomized rough surface. Since at the peak of the texture the area of the Si is zero, the flux absorbed shows a zero value; however, the flux density is non-zero as described in Figure 4} These figures show two features: (i) as expected, the photon flux for short wavelengths is confined near the front surface, and penetrates deeper with increase in the wavelength; (ii) for the thinner 50 µm film, the long wavelength illumination produces a nearly uniformly distributed flux within the cell.

3. The influence of texturing is to increase the absorbed photon flux density near the textured surface. Figure 4a shows the AM1.5 absorbed photon flux for a planar AR-coated (thickness 250 µm) and a textured AR-coated cell (the cell of Figure 2). The texturing increases the photon flux density near the surface. Figure 4b compares the flux density near the textured surface for the thick cell of Figure 2 with that of a thinner 50 µm cell; it is seen that the thinner cell has a higher density than the thicker cell. These are important results (not identified previously) that can make front surface recombination significantly more important than the back for very thin cells. Furthermore, it is seen that the major part of the absorption occurs within 20 µm below the front surface. Clearly, if the light absorption was the only criterion, a 20 µm film would be quite efficient. In order to perform the cell design, the optical analysis must be used in a cell model like PC1D to determine minority-carrier distribution and include recombination effects.

4. Application to solar cell module: The application of these analyses for encapsulated cells is demonstrated in Figure 5. The 100 µm thick cell has a nitride/oxide coating (thicknesses 710 Å and 100 Å, respectively) on a random front surface with a textured back surface reflector. In Figure 5, the encapsulant is 3,000 µm of glass on the 2,000 µm encapsulant. The absortion coefficient of the encapsulant was taken from reference 9. It is seen that encapsulation in this case produces about 6% loss in the current. Of this, ~ 4% of the loss is at the air-glass interface. The AR coating assumed in this example allows a better optical coupling from air than from the encapsulant. If a higher refractive index film, such as Ta_2O_5, or TiO_2, is used, the improved coupling can offset the losses due to encapsulation.

5. Effect of polarization: Because of the fact that the incident light that illuminates the cell normally is at oblique incidence at the local textured surfaces, one can expect TE and TM polarizations to have different reflection characteristics. For example, at the Brewster angle the reflection coefficient for TM polarization is zero, while that of TE polarization can be very high. We have performed calculations taking polarization into account. Figure 6a shows the reflectance of a textured, AR coated, 20 µm thick cell with a back reflector, for TE and TM polarizations. Some differences are evident. Figure 6b compares similar plots with polarization effects versus use of the of averaged reflectance value approximation as given by equation (13).

Results of 3-Dimensional Analysis

In the following, we describe 3-D analysis of three light-trapping structures and compare our results with previously published calculations.

Example 1: Textured pyramids: Figure 7a shows the reflectance, transmittance, and absorbance characteristics of a chemically textured 50 µm thick (100)-oriented silicon cell. These results show that the MACD can be 38.06 mA/cm^2. This current density is slightly higher than the 37.78 mA/cm^2 we obtained from 2-D (see Figure 7b). A comparison of the Figures 7a and 7b shows that the charcteristics are nearly identical for shorter wavelengths up to about 1 µm. For longer wavelengths, the 3-D calculations show lower transmittance and higher absorbance. This increased absorbance is due to the fact that the symmetry assumed in the 2-D modelling is valid only for the first pass of the light. This symmetry is lost when multireflections take place. Typically, 3-D calculations will show more effective light trapping than those using 2-D.

Example 2: Inverted pyramids: The results of inverted pyramids are shown in Figure 7c. The sample is 50 µm thick, with 5 µm deep inverted pyramids, and AR coating consisting of Si_3N_4 / SiO_2. This structure produces slightly lower reflectivity than the pyramid structure, which is partly offset by higher transmittance. The MACD is 39.2 mA/cm^2.

Example 3: Slat structure: Figure 8 shows the characteristics of a 50 µm slat cell with peak heights of 5 µm. The calculated value for the integrated absorbed photon flux was determined to be 2.52 x 10^{17}/ cm^2, yielding maximum achievable J_{sc} of 40.32 mA/cm^2. This value is in agreement with the values of refs. 5 and 6, which have assumed constant reflection of 80% at the back and 5% at the front.

The above 3-D calculations were performed by using averaged polarization reflection coefficient at each reflection.

DISCUSSION/CONCLUSIONS

From the above summary of results, we see that our analysis can optimize real AR coatings to closely match maximum currents determined by other analyses. Our analysis, by incorporating interference and polarization effects, can yield values of other parameters, such as the height and size of roughness, and the combinations of texture shapes that can optimize the thin cell performance.

The calculations we have performed show that:

- A significant increase in the effectiveness of the light trapping can occur by suitable selection of the texture. Ideally, the front surface texture is preferred since it is accompanied by a lower total reflectance. Figure 9 shows thickness dependence of the MACD for several light trapping structures. It is seen that the increase in the MACD due to texturing of a 25 µm thick film is about 3 mA/cm^2. This increase is about the same as increasing the thickness to 50 µm. It is also typically seen that the increase due to texturing is 3-4 mA/cm^2 (as compared to a rough surface and optimized AR coating).

- Surface recombination effects become very important because of the increased photon flux density due to texturing. In addition, as the thickness decreases, the photon flux due to long wavelengths tries to become more uniform within the cell thickness. Clearly, the need for passivated surfaces increases with a reduction in the cell thickness. The optical calculations do not show the effect of surface recombination. However, it is clear that as the absorbed photon flux near the surface increases, the surface recombination will have a more pronounced effect on the carrier loss.

- All our calculations have included the effect of polarization. However, it is clear from Figure 6b that one can use average values of reflection and transmission coefficients at each reflection. This assumption was implicitly made in a previous publication (7); this paper provides the proof.

- Our modelling shows that 2-D analyses can yield very valuable results for comparison of various structures. Such analyses can be performed rather fast. 3-D caculations take long times on personal computers and typically will result in higher current densities.

ACKNOWLEDGEMENT

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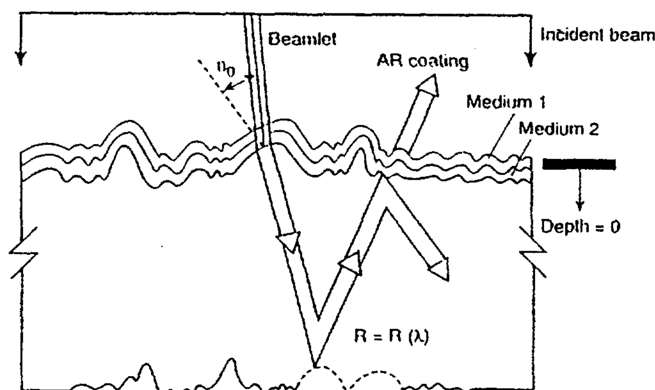


Fig. 1. Schematic model used for light trapping calculations

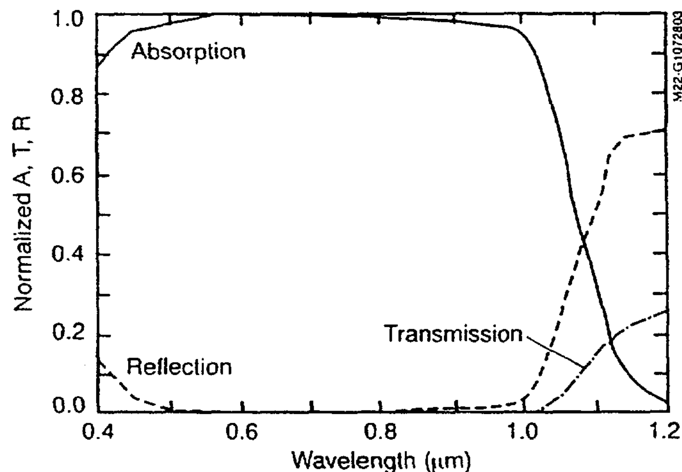


Fig. 2. Absorption, transmission, and reflection versus wavelength for a 250 μm thick, textured AR front and polished back cell

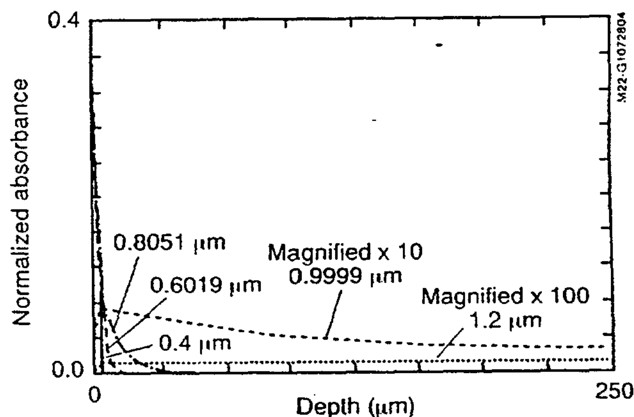


Fig. 3(a). Absorption plot as a function of depth for various wavelengths for the cell in Fig. 2 (250 μm thick)

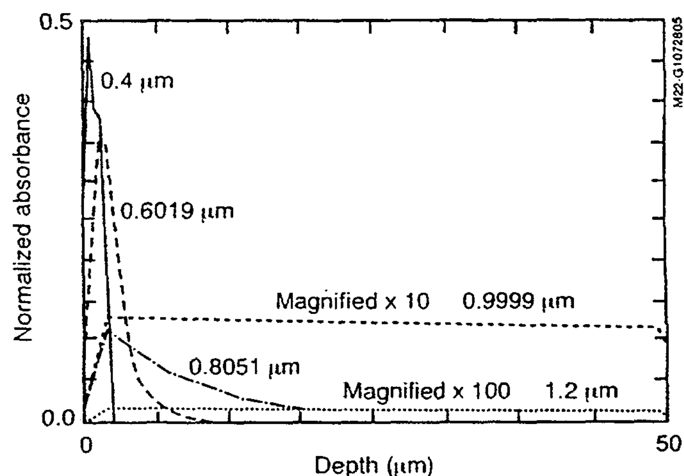


Fig. 3(b). Absorption plot as a function of depth for various wavelengths for the cell in Fig. 2, except 50 μm thick

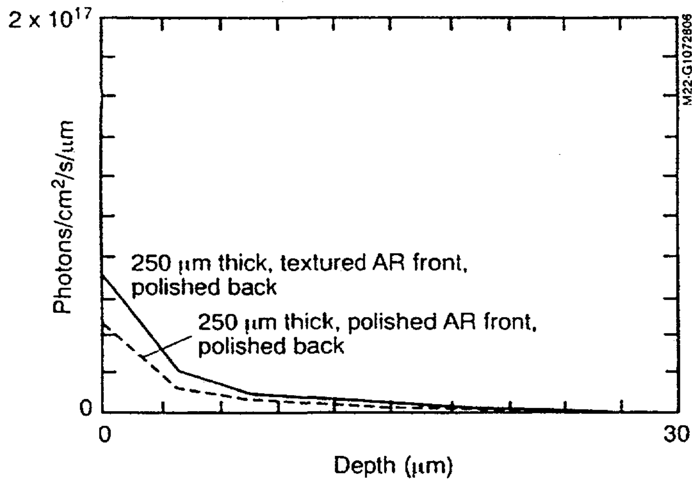


Fig. 4(a). AM1.5 absorbed photon flux density as a function of depth

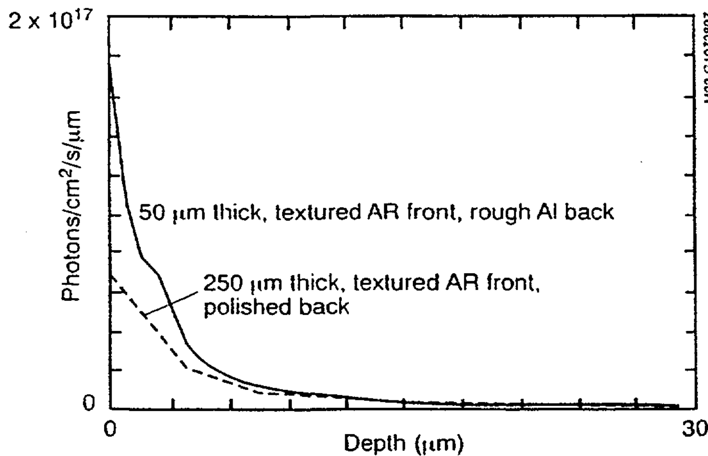


Fig. 4(b). AM1.5 absorbed photon flux density as a function of depth

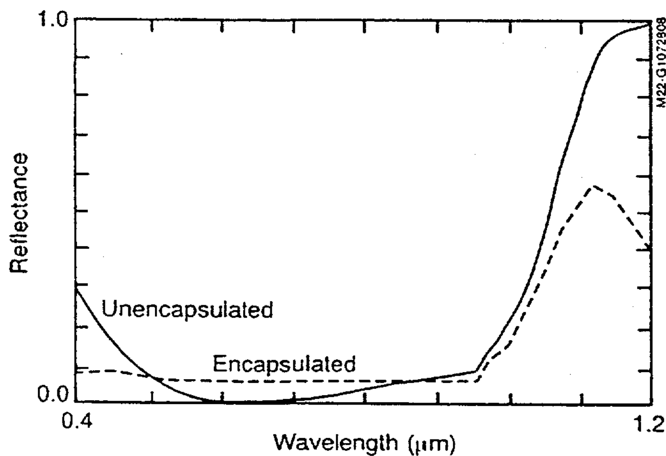


Fig. 5. A comparison of reflectance between encapsulated and unencapsulated cells

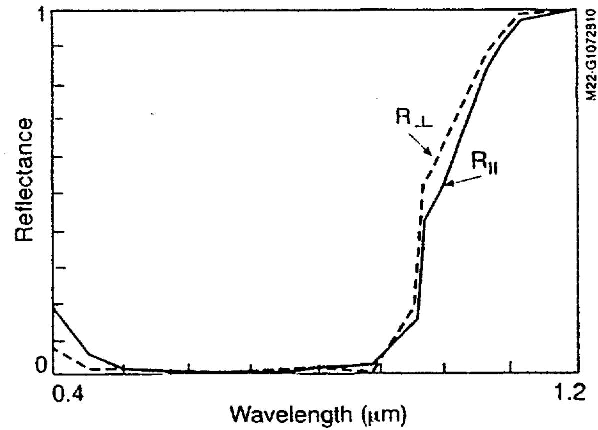


Fig. 6(a). A comparison of the total reflectance of a textured cell for parallel and perpendicular polarizations

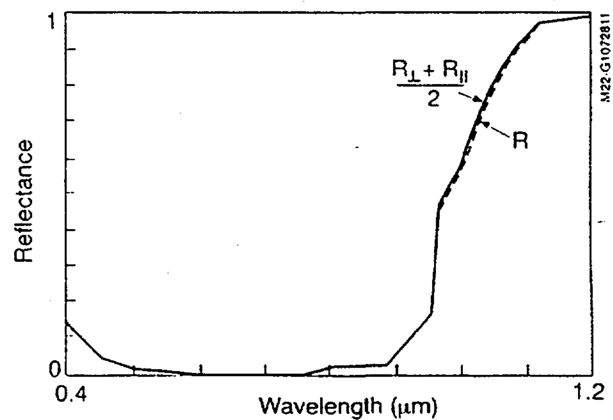


Fig. 6(b) A comparison of the reflectance of a textured cell based on two methods of including polarization effects
____ considering each polarization component separately
_ _ _ effects averaged at each reflection

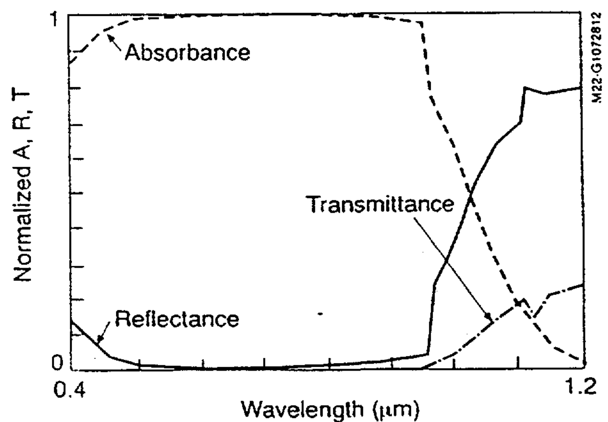


Fig. 7(a). Results of 3-D calculations for a textured 50 μm thick cell with pyramid shaped texture

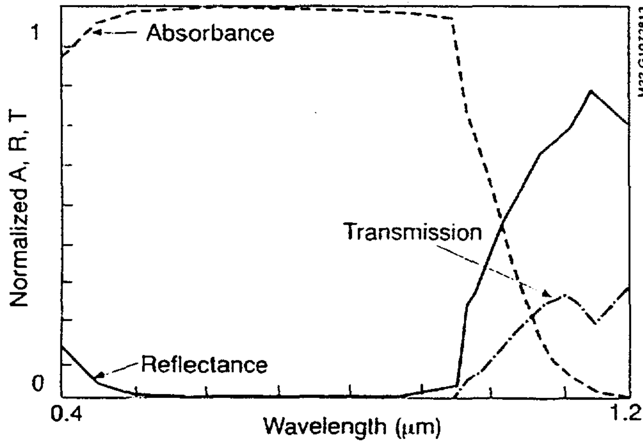


Fig 7(b). Results of 2-D calculations for the cell of Figure 7(a)

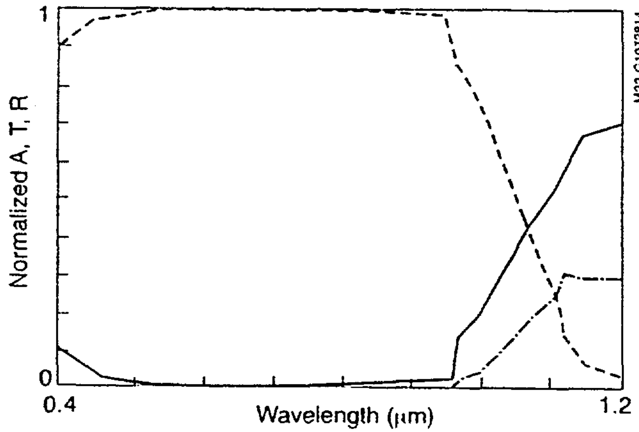


Fig. 7(c). Results of 3-D calculations for a textured 50 μm thick cell with inverted pyramid texture shape

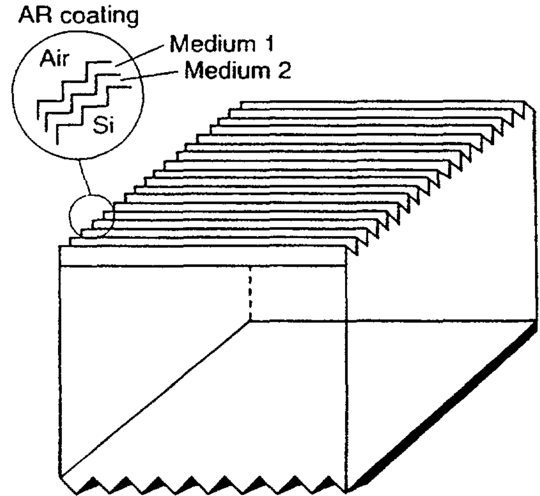
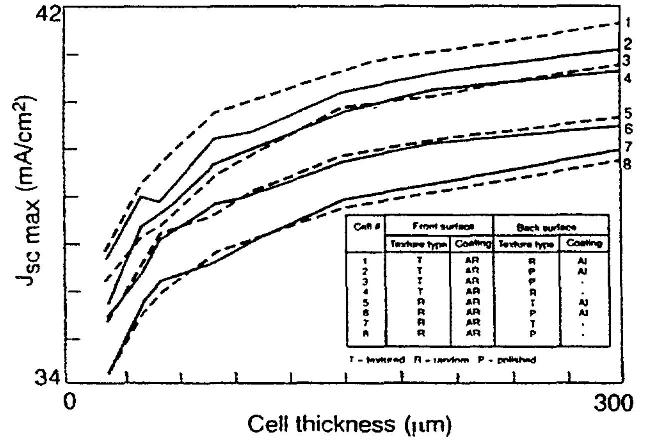


Fig. 8 Schematic of 50 μm thick cell with crossed slat structure discussed for 3-D modeling



Cell #	Front surface		Back surface	
	Texture type	Coating	Texture type	Coating
1	T	AR	R	Al
2	T	AR	P	Al
3	T	AR	P	-
4	T	AR	R	-
5	R	AR	T	Al
6	R	AR	P	Al
7	R	AR	T	-
8	R	AR	P	-

Fig 9. Maximum J_{SC} versus cell thickness for various front/back texture combinations

A SCANNING DEFECT-MAPPING SYSTEM FOR LARGE-AREA SILICON SUBSTRATES

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ABSTRACT

An optical scanning system has been developed that can produce maps of the spatial distributions of defects in polycrystalline silicon substrates. This instrument can operate in either the dislocation mapping mode or the grain boundary (GB) mode. In the "dislocation mode," the optical scattering from the etch pits is used to statistically count dislocations in large-area substrates. In the "grain boundary mode," the system recognizes local scattering from the GBs to generate grain boundary maps. The information generated by this instrument is valuable for material QA, identifying mechanisms of defect generation, the nature of thermal stresses during the crystal growth, and the solar cell process design.

INTRODUCTION

Crystal defects, such as dislocations and grain boundaries, strongly influence the performance of silicon solar cells. In commercial solar cells (fabricated on large-grain polycrystalline substrates), the dominant defect appears to be the intragrain dislocations. Recent analyses have shown that an average value of the dislocation density, measured over the large-area substrate, does not correlate well with the cell performance. This is because the localized regions of high dislocation density can produce a significantly higher effect on the cell performance compared to a case where these dislocations were uniformly distributed over the cell area. Consequently, a determination of the dislocation distribution over the large-area substrates has become quite important for a variety of purposes, including determining material quality variations within an ingot and among different ingots for QA purposes; improving the thermal conditions during crystal growth for lowering dislocation densities; achieving a proper cell design that can incorporate material inhomogeneities; and establishing the most effective cell fabrication processes.

The conventional method for determining the dislocation distribution in a wafer is to defect etch the sample and count the etch pits under an optical microscope. This procedure can be extremely tedious and time-consuming for large-area wafers (even with the help of image analysis attachments for the optical microscope). Other methods such as X-ray topography are not suitable for polycrystalline substrates.

We have developed a rapid, optical scanning technique that uses scattering from a defect-etched wafer to statistically count dislocations at the surface. It has been shown previously that the total integrated light, scattered from an illuminated region of a suitably defect-etched surface, is proportional to the number of dislocation etch pits in that area (1,2). This principle was previously applied to map dislocation density in large-area, single crystal semiconductor wafers. However, the usefulness of this technique for polycrystalline substrates was severely limited. It was found that grain boundary (GB) "grooving," which occurs during defect delineation by chemical etching, produced very strong signals that erroneously indicate a high dislocation density. This problem prevented application of the proposed technique to polycrystalline samples - a domain where it is expected to be the most valuable. We have recently solved this problem and successfully applied this technique to produce maps of the dislocation distributions in commercial silicon substrates, typically 10 cm x 10 cm in size. Furthermore, this technique is extended to image the grain distribution of the wafer.

This paper describes our new technique, which is capable of producing either dislocation maps or grain-boundary maps of polycrystalline silicon substrates. The paper also discusses how this information can be used for improving the material growth and predicting the solar cell performance.

PRINCIPLE OF THE TECHNIQUE

In the new approach, we use different scattering characteristics of dislocations and grain boundaries to distinguish them. It is seen that GB scattering occurs with a very large scattering angle, and the reflected light is primarily scattered as a line pattern perpendicular to the direction of the GB. However, the scattering from the dislocations occurs within a narrower cone as discussed previously (1). These scattering features allow us to retrieve the dislocation and GB information from the scattered and near-specular components of the reflected beams, respectively. In the setup described in this paper, the input and output apertures are adjusted such that the first lobes of the light scattered by the GB's, accompanying the specular reflection, are allowed to emerge from the integrating sphere along with the specular beam. However, the light scattered by the dislocations is captured by the integrating sphere. The GB and dislocation signals are individually detected by two different detectors. It is clear that in order for the

statistical method to work, the etch pits produced by the defect etching must have the same optical cross section. This can be accomplished by using a recently developed etch called the "Sopori etch", which consists of 36:15:2:: $HF:CH_3COOH:HNO_3$ (3). This etch delineates dislocations on all crystal orientations to produce etch pits of the same optical scattering cross-section, and produces V-shaped grooves at the grain boundaries.

SYSTEM CONFIGURATION OF SDMS

The Scanning Defect Mapping System (SDMS) is a high-speed laser scanning system that produces maps of the spatial distributions of crystal defects such as grain boundaries and dislocations in semiconductor wafers. Figure 1 is a schematic showing the major components of the SDMS. A light beam from a HeNe laser (λ=6328 Å) illuminates the defect-etched sample at normal incidence. The light scattered by the sample is collected by two detectors referred to as the Grain Boundary Detector (GBD) and the Dislocation Detector (DD), shown in Figure 1. These detectors are positioned so as to differentiate between etch pits and grain boundaries as follows.

When the laser beam is incident on a group of etch pits, the light is primarily scattered into a well-defined cone with an angular spread of about 20°. This light is collected by the integrating sphere and is measured by the photodetector DD. The signal from the detector, which measures the integrated light intensity, is proportional to the local dislocation density of the sample.

When the laser beam hits a grain boundary, the light is scattered as a 1- dimensional streak, elongated perpendicular to the length of the GB. The near-specular component of the scattered light passes through the integrating sphere and is reflected by the beam splitter towards the GBD. The central stop of the annular aperture blocks the axial component of the beam, allowing the off-axis component to focus on the GBD.

When the laser beam is incident on a defect-free area of the sample, the light is specularly reflected back out of the integrating sphere, giving no signal on the DD. This beam is then blocked by the annular aperture, thus producing no signal on the GBD either.

The sample is scanned under the light beam using an X-Y stage. The SDMS can be used in two modes: "dislocation" mode, and "grain-boundary" mode. It is possible to acquire the data simultaneously in both the modes. Electronic circuits are provided to minimize the cross-talk between GB and the dislocation signals. The signals from the two detectors are digitized and fed into a computer along with the X-Y position signals from the scanning stage. The data are stored in high speed buffer memory. Commercial software is used to make a map of the defect distribution or grain boundaries in the sample. Having the information stored in the computer allows the user to perform detailed analyses of the distributions. Alternatively, the analog signals from the detectors are processed to directly display the defect and GB distributions on a storage oscilloscope.

RESULTS

Figure 2a is a dislocation density map of a 2.5-cm x 2.5-cm commercial solar cell substrate generated by the SDMS. The dislocation densities corresponding to various gray scales are identified; a calibration sample is used to establish this relationship [Typically, the SDMS produces color maps of the defect distributions. We have used gray scale maps to facilitate printing of this paper]. Figure 2b shows a grain-boundary map of the same sample. Figure 3 is a photograph of the sample whose dislocation and GB maps are shown in Figure 2 ; the sample was mildly textured to enhance the grain appearance. In comparing these figures, one can clearly note the absence of grain boundaries in Figure 2a and the absence of dislocations in Figure 2b.

Due to short times required for mapping dislocations (typically 2 hours for a 10-cm x 10-cm wafer), SDMS can be used routinely to evaluate material quality of commercial photovoltaic silicon substrates. Figure 4a is dislocation map of a polycrystalline silicon wafer for commercial solar cells. A photograph of the defect-etched sample is given in Figure 4b for comparison. It is seen that a large fraction of the total substrate area has very low dislocation density. However, a strong variation in the dislocation distribution seen in this figure is expected to degrade the cell performance due to the fact that heavily dislocated regions can acts as "sinks" and shunts for the rest of the device.

In evaluating the material quality by this technique we consider two parameters: the average dislocation density, and the degree of spatial variation in the dislocation density. At this time it is not known how each of these parameters influence the cell performance. These issues are being addressed in our current research work.

The dislocation distributions determined by SDMS can also be used on a qualitative basis to determine the locations of high thermal stresses (above the yield stress level) during crystal growth. Figure 4 is a dislocation map of a sample that has high dislocation density near the center of the casting, indicating a high level of stress towards the center of the casting. It is important to note that this information can only be obtained by extensive defect analyses, such as by SDMS. Further details of the relationship between defect distributions by SDMS and the crystal growth conditions are given in a forthcoming paper (4).

CONCLUSION

We have described an optical scanning technique for the defect mapping of single- and poly-crystalline silicon substrates. This technique uses optical recognition of dislocations and grain boundaries and performs statistical counting of dislocation etch pits. These features make this technique rapid and accurate compared to any other techniques currently available. Furthermore, the cost of the instrument is very low compared to other instruments based on imaging and electronic recognition. Although we have demonstrated the use of this technique for silicon wafers, it is also applicable to other semiconductors.

ACKNOWLEDGMENT

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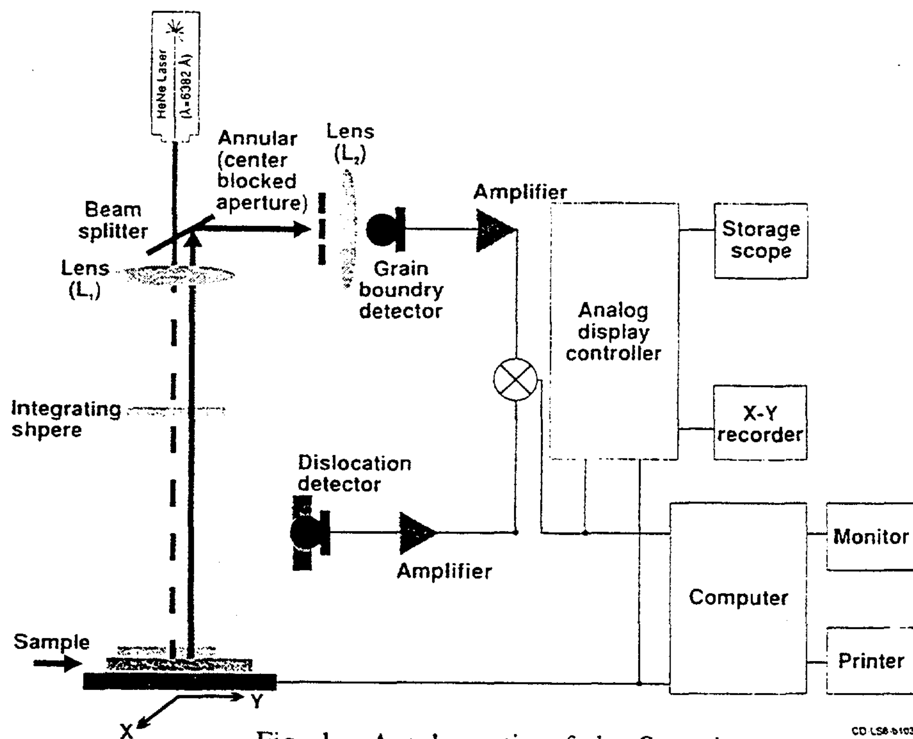


Fig. 1. A schematic of the Scanning Defect Mapping System

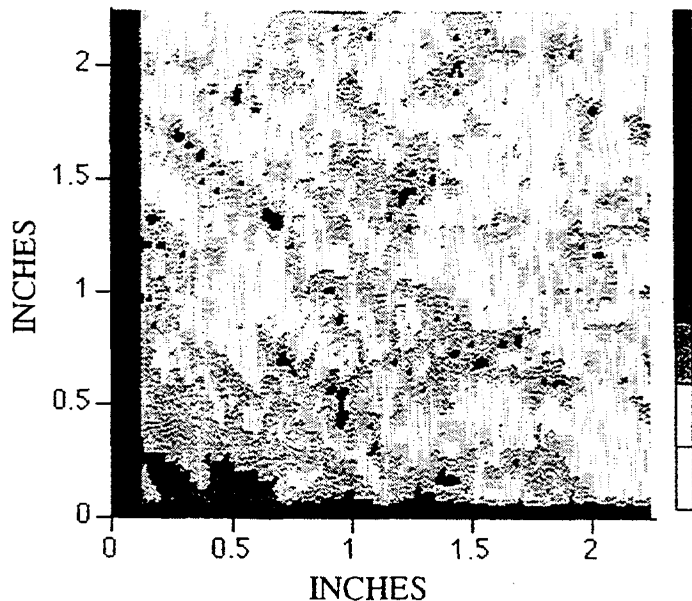


Fig. 2a. Dislocation map of a 5-cm x 5-cm polycrystalline silicon substrate (shown in Fig. 3) produced by SDMS

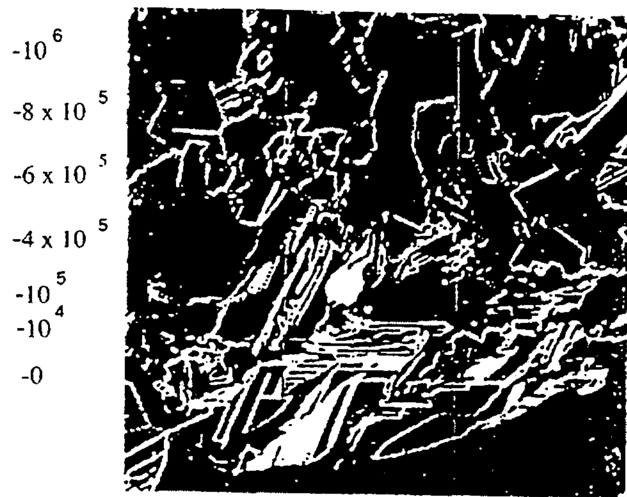
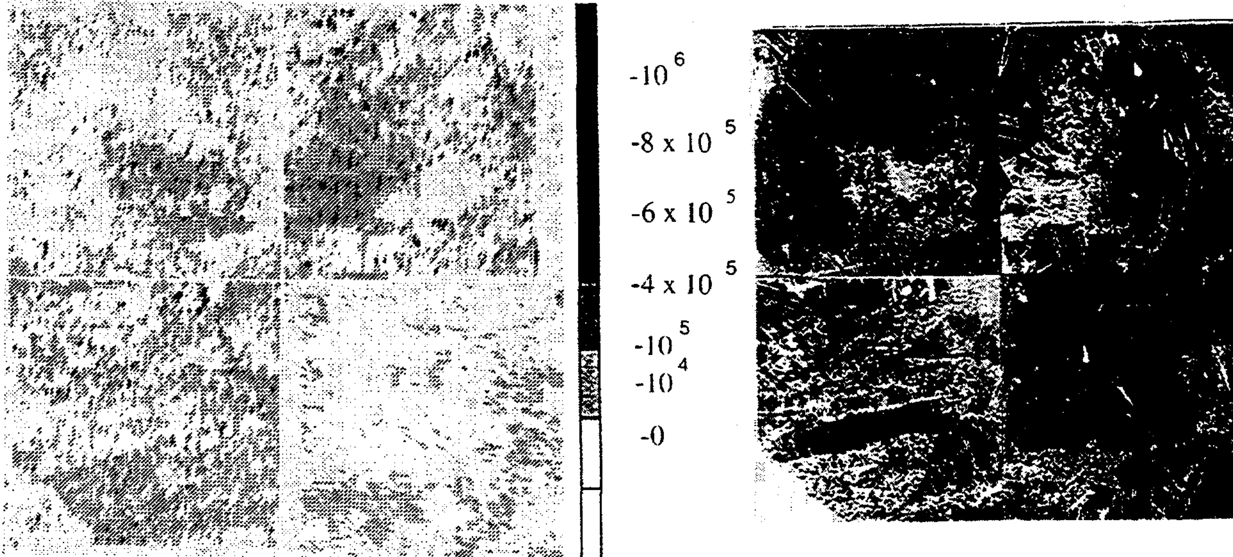


Fig. 2b. Grain-boundary map of the 5-cm x 5-cm sample shown in Fig. 3

Fig. 3. Photograph of the defect-etched sample used in Fig. 2

Fig. 4a. Dislocation map of a 10-cm x 10-cm commercial silicon wafer showing non-uniform dislocation distribution

Fig. 4b. Photograph of the defect-etched sample corresponding to the dislocation map of Fig. 4a.



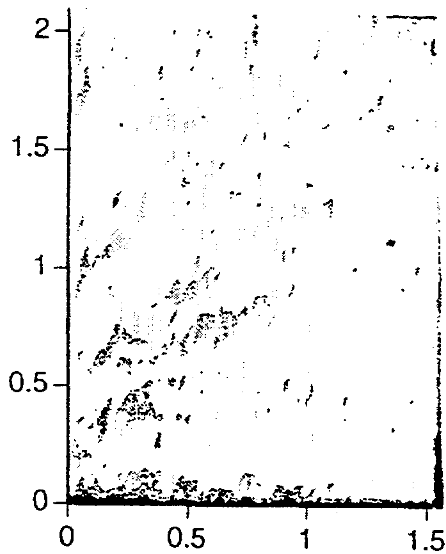


Fig. 5. Dislocation density map of a 5-cm x 5-cm corner section of a cast wafer indicative of a high thermal stress near the center of the casting, manifested as high dislocation density in the center.

PV:BONUS -- DEVELOPING A U.S. MARKET OF PV IN BUILDINGS

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ABSTRACT

The use of photovoltaic (PV) systems in and on buildings is seen as a key intermediate market for the PV industry. The buildings market is challenging, but it provides a large potential for increased U.S. production of "high-value" PV technology that will benefit electric utilities and building owners. To assist the PV industry in developing products for this market, the U.S. Department of Energy began a new initiative called "Building Opportunities in the U.S. for Photovoltaics" (PV:BONUS). The responses cover nearly all of the PV-buildings product options envisioned, with multiple responses on topics such as architectural glazings and roofing systems. The paper describes the types of products that will be pursued by the teams selected. Additional supporting activities are described that will further encourage the development of a sustainable infrastructure.

INTRODUCTION

Photovoltaics (PV) are large-area semiconductors that generate direct-current electricity directly from the sun with no moving parts needed. PV is cost-effective today for many applications such as remote homes, water pumping, telecommunications, and rural electrification. If PV is incorporated as a part of the building envelope, most likely its orientation will be fixed. The orientation of PV will determine the electrical energy generated on a daily and annual basis. The annual production of electricity is a maximum for a fixed PV array facing south and sloping at an angle equal to the latitude. The maximum production of electricity can be optimized for winter or summer by changing the slope angle closer to vertical or horizontal, respectively. During summer a vertical PV wall facing east or west can maximize the monthly energy production in the morning or afternoon compared to a PV wall facing south.

PV on buildings is not a new concept. Three market factors contribute to the renewed interest in PV-integrated buildings. First, electric utilities are changing; second, environmental awareness is increasing, and third, international PV competition is strong. Many electric utilities are recognizing the additional value of distributed electrical generation provided by PV [1]. Electrical generation close to the customer avoids costs associated with transmission and distribution. A building is the closest an electric utility can place a PV system to the customer. Also, the area of buildings' roofs and walls is more than sufficient to incorporate a significant amount of PV. There are increasing levels of awareness and regulations concerning the environment and sustainable construction. In addition to reducing air emissions, other considerations include the energy required to produce a product, and environmental impact during production and disposal of products. PV is a net energy producer -- few products can claim this distinction. The energy payback of PV is estimated at three to eight years depending on the technology and production volume. Finally, international competition for PV markets is fierce.

OPPORTUNITIES

Approximately two-thirds of the electricity generated in the U.S. is consumed in residential, commercial, and institutional buildings. Major electrical end uses in these buildings include lighting, air handling, air conditioning, pumping, and refrigeration, as well as a long list of small-to-medium appliance loads. The use of photovoltaic (PV) systems in and on buildings is a key market for the PV industry. Figure 1 is a drawing of potential applications. PV systems can provide a variety of functions in a building environment. These functions can be classified as architectural, demand-side management (DSM), control, and hybrid. In architectural functions, the PV array does double duty as a roof, a wall, or a window. For DSM, the PV array is designed to provide power to partially offset a building's contribution to the utility peak loads. In control functions, the PV system provides the primary energy for powering air movement (fans), fluid movement (pumps), or "active" windows and walls. The match of the solar resource to the load requirements is a key in control-function applications. For hybrid functions, the PV system supplies all or a portion of the energy in conjunction with "conventional" equipment, such as heat pumps, air conditioners, or lights. Cost effectiveness in hybrid applications can come from multiple uses of the electronics and coincidence between PV output and time-of-day rates. The buildings market is challenging, but it provides a high potential for increased U.S. production of PV. Appropriate product and system designs can open up major markets in the residential, commercial, and institutional buildings sectors.

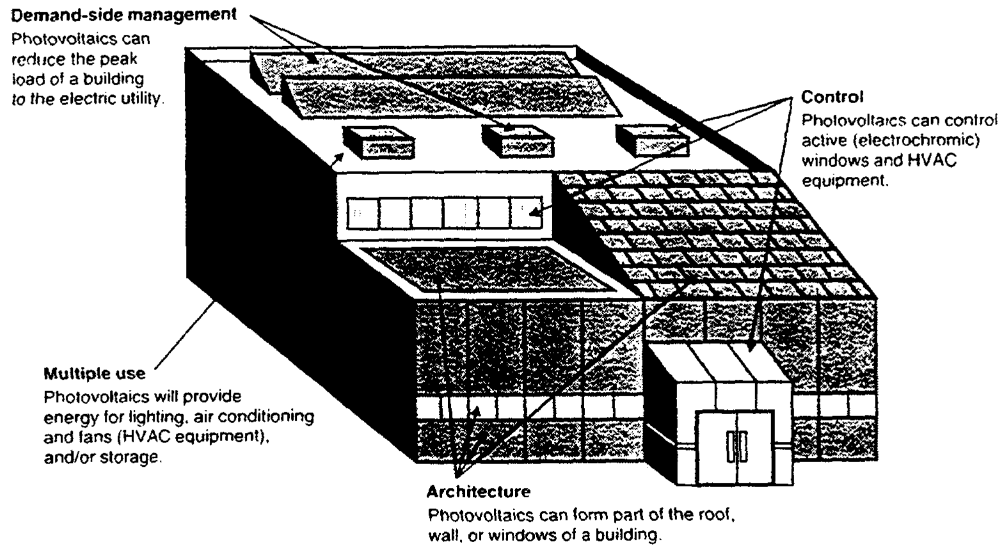

Fig. 1. Potential Applications of Photovoltaics in Buildings.

Unless a PV-integrated building has a need for autonomy, the building will be connected to the local electrical grid. While the dc output of PV could service a dc load directly, more likely the PV output will be inverted to ac electricity and connected to an existing ac distribution circuit. As more buildings incorporate advanced load management centers, the PV generated electricity will be just another input.

PROGRAM OVERVIEW

Developing the required PV-integrated building infrastructure requires the participation of many U.S. industry sectors, each of which has the opportunity to benefit from the development. The U.S. industry sectors include the PV industry, building equipment suppliers, utility industry, developers/builders, construction industry, and the building owners.

In 1992, NREL contracted Solar Design Associates and the Florida Solar Energy Center to document what had been done or is planned for PV-integrated buildings. Steven Strong, Solar Design Associates, reviewed the present status of PV-integrated buildings in Europe, Japan, and the United States [2]. Switzerland and Germany have strong programs. William Young and Kirk Collier, Florida Solar Energy Center, discussed roof-mounted PV systems designed for or installed on buildings [3]. Roof-integrated designs from 1973 to 1992 were discussed.

A report by Gregory Kiss of Kiss, Cathcart, and Anders Architects explores the issues and opportunities of PV-integrated buildings from the perspective of the design community [4]. Looking toward the future, NREL has contracted the American Institute of Architecture, Association of Collegiate Schools of Architecture (AIA/ACSA) to develop and disseminate teaching cirriculum on photovoltaics-in-buildings for North American schools of architecture. A pilot curriculum will be developed and then taught during the 1993 fall semester by John Reynolds, University of Oregon; Jeffrey Cook, Arizona State University; Dimitri Procos, Technical University of Nova Scotia; and Richard Diamond, Harvard University. The final curriculum will include a primer on PV, guidelines on teaching PV in lecture and design studio settings, and case studies of successful PV applications in buildings.

PV:BONUS SOLICITATION

To assist industry in developing near- and long-term markets within the buildings sector, the DOE began a new initiative called "Building Opportunities in the U.S. for Photovoltaics" (PV:BONUS). PV:BONUS is envisioned as a 5-year, $25-million (DOE), government/industry cost-shared initiative to develop cost-effective PV products and product-supply/product-user relationships that provide a sustainable market for PV-integrated building products.

A Notice of Program Interest (NOPI) was issued on August 14, 1992. Table 1 outlines the preliminary responses that covered nearly all of the PV-buildings product options envisioned, with multiple responses on topics, such as architectural glazings and roofing systems. The DOE announced that it started negotiations with five companies: Advanced Photovoltaic Systems, Energy Conversion Devices, Fully Independent Residential Solar Technology (FIRST), Solar Design Associates, and Delmarva Power & Light. The following describes the types of products being considered for funding.

TABLE I. Preliminary Responses to PV:BONUS Solicitation.

Building Products
PV-Curtain Walls
PV-Blinds
PV-Greenhouses
PV-Dynamic Facades
PV-Roofing Systems
PV-Variable Transmission Windows
PV-Smart Windows
PV-Roofs for Manufactured Homes
Hybrid Products
PV-AC-Lighting
PV-DC-Lighting
PV-Air Handling
PV-Condensor Fans
PV-Heat Pumps
PV-Air Cleaner
PV-Vent Fans
Applications
Gas Stations
Fast Food Restaraunts
Payphones
EV Charging Stations
Residential/Commercial Development
Parking Lots & Walkways

Dispatchable PV: Delmarva Power & Light

Generally, PV output follows the electric utility peak demands. However, sunshine can not be guaranteed and many utilities have a peak that extends past sunset. The combination of PV and batteries would improve the availability and reduce demand charges.

Roofing shingles: Energy Conversion Devices

The use of PV modules as the roofing material has always interested building owners and architects. The dual use of PV -- to generate electricity and serve as the roof -- offsets the cost of the PV by the amount not invested in traditional roofing materials.

ac modules: Solar Design Associates

PV modules produce dc electricity. Typically, modules are wired in parallel and series for the appropriate voltage input to an inverter for transformation to ac electricity. Given the advances in power electronics, a PV module can be envisioned with its own inverter mounted on the back of the module. An ac module would free architects and designers from the dc wiring constraints and minimum PV system size for using an inverter.

Building facades: Advanced Photovoltaic Systems

PV can be used in curtain-wall construction for building facades. Instead of a traditional glass panel, a PV module can be used. These PV modules can also be made semitransparent during the module construction. A complete building facade can then be designed using a combination of opaque, semitransparent, or clear modules.

Manufactured homes: FIRST, Inc.

Many residential homes are manufactured in a factory and then trucked to the building site. The installation of a PV system on a house in the factory could result in a consistent and less-costly PV system. Also, the house can be wired PV-ready.

SUMMARY

Today, PV is cost-effective for many applications. The concept of PV systems mounted on buildings or as a part of the building envelope has been demonstrated. However, for sustainable use of PV in the building sector, more work is needed. Architects, builders, utilities, and owners need to be participants. DOE/NREL has begun a program incorporating the key stakeholders working together to make energy-producing buildings a reality.

ACKNOWLEDGMENTS

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POTENTIAL APPLICATIONS OF POROUS SILICON IN PHOTOVOLTAICS

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ABSTRACT

Porous Si formed on crystalline Si wafers using electrochemical etching exhibits photoluminescent and electroluminescent properties. We report on the results of our investigation of using porous Si as surface texturing to enhance the performance of crystalline silicon photovoltaic solar cells. Unlike conventional KOH-based texture etching, which can only be used on [100]-oriented single-crystalline Si substrates, porous Si can be etched onto Si surfaces of any crystallographic orientation and onto polycrystalline or microcrystalline Si surfaces. A porous-Si-covered single-crystal Si wafer showed an integrated reflectance of only 1.4% at a wavelength of 500 nm. The reflectance of a porous-Si-covered polycrystalline Si was found to be comparable to other much more complicated texturing methods.

INTRODUCTION

Properties of Porous Silicon

The discoveries of the visible light emission behavior and the apparent bandgap widening of porous Si were reported less than 3 years ago [1,2]. Since then, the possibilities of gaining insight into the physics of quantum confinement in Si and of forming Si optoelectronic devices have attracted considerable research interest. (See, for example, Materials Research Society Symposium Proceedings Vol. 256 [1992], 283 [1993], and 298 [1993].) Porous Si is usually formed on a crystalline Si substrate at room temperatures by a simple anodic dissolution process in a HF-based electrolyte. A porosity range of 30% to 90% has been observed for light-emitting porous Si. The nanostructure of porous Si, although twisted as appeared in scanning electron microscopy images, is well aligned with the underlying crystalline Si lattice [3-5]. The peak wavelength of the room-temperature photoluminescence (PL) depends on the size of the porous Si wires, which is usually a few nanometers across, and the PL quantum efficiency can be up to about 10%.

The quantum confinement model [1,2,6,7] is most widely used to explain the origin of the light-emission properties of porous and nanostructured Si. In this model, the absorption process responsible for the strong visible photoluminescence occurs primarily inside dimensionally confined Si wires. The widely observed correlation of the emission wavelength with the dimension of the quantum wire can be easily explained by this model. The broad PL emission peak of porous Si indicates a large size distribution of the quantum wires produced by the electrochemical etching process. Other models include light emission from surface-resident chemical species, such as siloxene [8], and light emission from entrapped amorphous Si phases [9].

The as-etched porous Si surface is hydrogen-terminated. Hydrogen passivation of nonradiative recombination centers at the surface is important for the light-emission properties of porous Si. The porous Si PL is quenched by annealing and recovered by rehydrogenation or oxidation of the surface. Improved PL intensity and stability have been reported with postetching oxidation methods [10-12]. Light-emitting porous Si films on thin-film polycrystalline and microcrystalline (μc) Si have also been demonstrated [13,14]. These demonstrations are important for developing large-area display applications of porous Si.

Electroluminescent (EL) emission from porous Si was first observed during electrochemical oxidation [15]. Since then, solid-state light-emitting diodes (LED) using porous Si have been successfully fabricated. Reported porous Si LED structures include a Au top contact on p- and n-type porous Si [16,17], n-type indium tin oxide (ITO) on p-type porous Si [18], p-type Si/porous Si/n-type μc-SiC p-n junction diodes [19], and homojunction p-n diodes [20].

The photoconductivity spectra of samples of vacuum-deposited semi-transparent Au films on porous Si were measured and found to exhibit a peak at about 500 nm (2.5 eV) [17,21]. A significant external quantum yield (20% at the peak) was observed at a temperature of 75 K using a Schottky diode with the structure of Au (15 nm)/porous Si (0.4 μm)/p-type Si/Al [21].

Potential Porous Si Applications in Photovoltaics

Generally speaking, materials that exhibit PL and EL properties should also be good candidates for solar cells and photodetectors. Potential advantages of using porous Si in solar cell structures include: (1) The highly textured morphology of porous Si may be used to enhance light trapping. (2) The bandgap of porous Si may be adjusted for optimum sunlight absorption; the maximum theoretical solar cell efficiency versus bandgap curve peaks at around 1.5 eV, which is within the range of observed porous Si bandgaps. The apparent wide bandgap of porous Si may allow it to be an ideal material for the top layer of a heterojunction cell, or for the absorber of the top cell of a tandem cell structure with Si. The wide bandgap of porous Si may also be useful for establishing a back or front surface field in a diffused-junction Si solar cell. (3) The photoluminescent property of porous Si may be used to convert ultraviolet and blue light into longer wavelength light that has a better quantum efficiency in a Si solar cell. (4) Porous Si formed on the back surface of a Czochralski-grown Si wafer can be effective as an external gettering center for impurity atoms that would otherwise

form stacking fault nucleation sites during high-temperature oxidation [22]. This property can be very useful for photovoltaics, because high efficiency crystalline Si solar cell fabrication often involves several high-temperature oxidation steps. (5) The ease and the large-area potential of electrochemical etching should make porous Si a very suitable technological candidate for large-area applications such as solar cells.

However, there are also many problems associated with using porous Si in solar cell structures. The high resistivity and the lack of understanding of the photocarrier generation and charge carrier transport mechanisms of porous Si make it difficult to design high-efficiency solar cell structures that use porous Si as the light-absorbing layer. In addition, conventional dopant diffusion and oxidation processes for Si solar cell fabrication require temperatures higher than 800°C, much higher than the temperature that would quench the light-emitting properties of porous Si [10].

Zheng et al. [23] fabricated Al/porous Si/Si photodetectors and found that they have high sensitivity with a spectral response curve similar to that of conventional single-crystal Si photodetectors. The porous Si layer has little absorption; most of the photoresponse comes from the Si substrate. However, Zheng et al. concluded that the porous surface was "perfect" in trapping light, and the surface was "well passivated with very low surface recombination." Smestad et al. [24] studied the photoresponse of a Pt probe/porous Si/Si structure and also showed that the spectral response was characteristic of the single-crystal Si substrate itself. Moreover, from their time-resolved photoconductivity measurements, the authors concluded that the porous Si/Si interface was poorly passivated (in contrast to Zheng et al.) and that the porous Si/Si interface had a higher initial surface recombination rate than either the SiO_2/Si or air/Si interface.

For this study, we concentrated on investigating the effects of forming a porous Si layer on the front surface of a crystalline Si solar cell. In addition to light trapping, such a porous Si layer may also serve as a heterojunction, a front surface field, and/or a photon converter for the underlying Si solar cell. The results on front surface texturing of point-contact solar cells [25] from SunPower Corporation, Sunnyvale, California with porous Si were recently reported by Tsuo et al. [26] and will be briefly summarized here. The point-contact solar cells are well suited for studies of front surface texturing by porous Si because of a backside-contact design that has both polarities of contacts made to the back of the cell. This allows us to readily perform the porous Si etching on the front surface after the junction formation, after the metal contacts have been evaporated and alloyed, and after the cell has been mounted on copper electrodes and an alumina supporting plate.

EXPERIMENTAL PROCEDURES

Our porous Si etching method and apparatus have been described in detail elsewhere [27,10]. A typical porous Si etching process involves anodization in a 50% ethanol/50% HF (48 wt. %) electrolyte with a 10 mA/cm^2 current density for 3 min. The resulting porous Si films were about 1.2-µm thick. Alternatively, an electrolyte of two parts of methanol mixed with one part of 48% HF was also used with a current density of 1 mA/cm^2. The ethanol/HF mixture produces porous Si with lower porosity, longer peak emission wavelength, and lower PL intensity than those of porous Si produced using the methanol/HF mixture [5].

Optical transmittance and reflectance were measured using a Beckman dual-beam spectrophotometer with an integrating sphere. PL and photoluminescence excitation (PLE) [6] data were taken using a SPEX model FL112XI Fluorolog-II fluorescence spectrophotometer equipped with a 450-W Xe lamp and a Hamamatsu R928 photomultiplier emission detector.

RESULTS AND DISCUSSION

Integrated Reflectance

To study the effectiveness of using porous Si as a front-surface light-trapping layer in a single-crystal Si solar cell, we compared the integrated reflectance of porous Si layers with thicknesses ranging from 0.2 to 10 µm and polished crystalline Si surfaces. The least reflective porous Si film is a 10-µm-thick film that went through an additional leaching process in a solution of 10 parts of 48%HF and one part of HNO_3 for 3 to 5 s after electrochemical etching. The leaching solution was pretreated by dissolving a small amount of Si to increase the amount of HNO_2 in the solution [28]. This leaching process further reduced the thickness of the Si filaments. This film has an integrated reflectance that is much lower than that of a KOH-solution-textured (100) Si surface. It is even better than textured Si with a layer of 110-nm-thick SiO_2 (refractive index, n = 1.46) antireflection (AR) coating, which is widely used by the Si solar cell industry for light trapping (see Fig. 1). This porous Si reflectance is comparable, as shown in Fig. 1, to the best AR-coated Si surface that we have ever achieved using a textured Si surface with a double-layer AR coating of 90-nm-thick MgF_2 (n = 1.38) and 53-nm-thick ZnS (n = 2.30). This is noteworthy, because texturing by KOH-based solutions can only be done on [100]-oriented single-crystalline Si substrates while porous Si can be etched onto Si surfaces of any crystallographic orientation and onto polycrystalline or microcrystalline Si surfaces. Porous Si etching is also much simpler and cheaper than multilayer AR coating depositions.

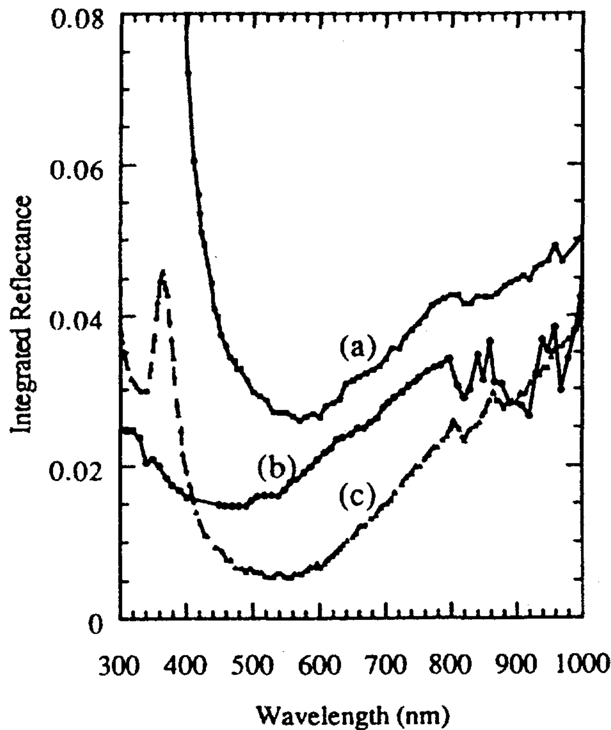

Fig.1. The integrated reflectance spectra of (a) KOH-textured Si with a SiO_2 AR coating, (b) a porous-Si-textured Si, and (c) KOH-textured Si with an additional double-layer AR coating.

Transmission Properties

The absorption and light-emission properties of porous Si can be adjusted over a wide range. Shown in Fig. 2 is our measurement of porous Si transmission. This measurement was made by abrading a 2-µm-thick porous Si film onto a Corning code 7059 glass plate. The sample had an orange-colored photoluminescence emission even in powder form. Because a typical Si solar cell has its strongest photoresponse in the wavelength region of 400 to 1000 nm, the optical absorption of a thin porous Si layer in the front surface of the cell should have minimal effects on the spectral response.

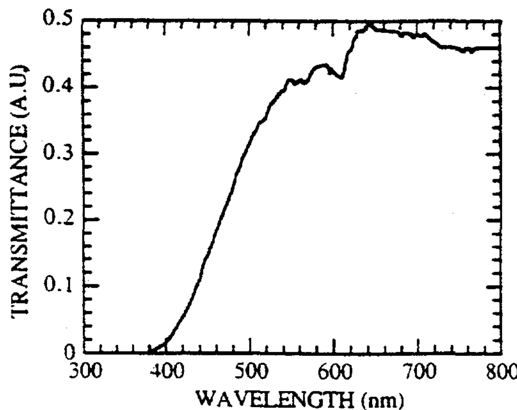

Fig. 2. Optical transmission of a porous Si film

Front-Surface Texturing for Solar Cells

The concept of using an *oxidized* porous Si layer for antireflection coating for single-crystalline and polycrystalline Si solar cells was discussed and demonstrated by Prasad et al. [29] long before the discovery of the light-emission behavior of *as-etched* porous Si. They used relatively low-conversion-efficiency P^+N diffused junction solar cells and performed porous Si etching on the diffused P^+ layer. The porous Si layer was then oxidized at 500° to 600°C. The average reflectance of the solar cells from 300 to 800 nm wavelength was found to decrease from 37% to around 8% with the addition of the oxidized porous Si antireflection coating. Metal contact to the solar cells was made through the oxidized porous Si without difficulty. The conversion efficiencies of the solar cells were improved by a combined effect of light trapping and front surface oxide passivation. More recently, photoelectrochemically etched porous Si was used to reduce surface recombination and incident light reflection of Si-based aqueous photoelectrochemical cells, and thus improved the efficiency and stability of the cell [30].

The work by Tsuo et al. [26], mentioned earlier, showed that porous Si etching on the front surface of a point-contact solar cell increased the amount of light absorbed by the cell. This produced slight improvements on the long wavelength side of the photoresponse curve. However, etching also removed the surface-passivating oxide and part or all of the 0.5-µm-thick n^+ region on the cell surface, which is used to establish a front-surface field. This resulted in slight degradation of cell performance. The sample surface had visible PL emission after porous Si etching, indicating that the blue light absorbed by the porous Si layer was re-emitted as longer wavelength light. The main reason for the cell degradations is believed to be because of increased surface recombination caused by the removal of the front surface oxide layer. Oxide passivation of the front and back surfaces is an important requirement for modern high-efficiency Si solar cell designs. Thus it is important to compare the surface passivation capability of porous Si with that of silicon dioxide and to develop low-temperature oxidation methods for the porous Si surface.

Si Surface Passivation

To compare the surface passivation capabilities of porous Si and SiO_2, we measured the effective minority-carrier lifetime, τ_{eff}, in wafers with different surface treatments. The value of τ_{eff} in a wafer is related to the surface recombination velocity, S, by the relationship $1/\tau_{eff} = 1/\tau_b + 2S/L$, where τ_b is the minority-carrier lifetime in the bulk, and L is the wafer thickness. τ_{eff} in a Si wafer can be determined by an inductively coupled, contactless photoconductivity decay (PCD) measurement. Two types of PCD measurements were used: (1) a pulsed 904-nm laser diode is used to illuminate the sample, and the change in sample conductivity is monitored by reflected 9.6-GHz microwaves (MW). The acid used for surface passivation by immersion, if needed, is H_2SO_4;

Table I. Effective lifetime of Si samples measured by photoconductivity decay.

Sample	MW τ_{eff} (μs)	RF τ_{eff} (μs)
Wafer oxidized on both sides Measured in air	230	130
Control wafer Measured with acid immersion	178	165
Porous Si etched in front Measured with acid immersion	53	90
Control wafer Measured in air	12	12

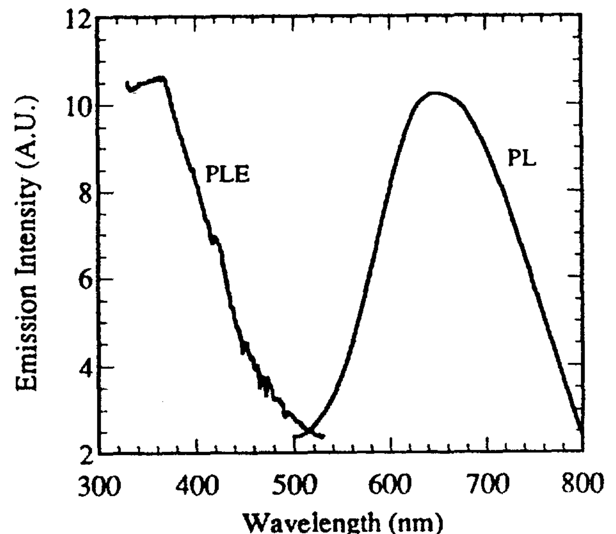

Fig. 3. Photoluminescence (excitation wavelength = 380 nm) and photoluminescence excitation (monitor wavelength = 640 nm) spectra of a porous-Si-etched polycrystalline Si sample.

(2) a 1538-A General Radio Stroboscope Lamp is used to illuminate the sample, and the change in sample conductivity is monitored by reflected 53.5-MHz radio-frequency (RF) waves. The acid used for surface passivation by immersion, if needed, is HF. N-type, 3 Ω-cm, 250-μm-thick, (100) float-zone Si wafers were used for the experiments. A 60-nm-thick SiO_2 grown at 1000°C was used for oxide passivation. In Table I, we show the results of these measurements.

The lower τ_{eff} measured on the porous Si-etched wafer compared with that of oxide-passivated and acid-passivated control wafers may indicate higher recombination velocities at the porous Si/Si interface and/or the porous Si/acid interface than at the Si/SiO_2 interface and hydrogen-passivated (by acid immersion) Si surfaces. More systematic measurements are being done in our laboratories to separate the contributions of front and back surface recombination and to quantitatively determine the surface recombination velocity at various surfaces and interfaces of porous Si-etched samples.

Polycrystalline Silicon

For the polycrystalline texturing study, we used Wacker SILSO p-type, 1 Ω-cm resistivity, cast Si wafers with millimeter-sized grains. We found that porous Si etching of this polycrystalline Si using the HF/methanol electrolyte produced a much more uniform etch and a much brighter PL than the HF/ethanol electrolyte. The HF/ethanol etch tended to concentrate in certain grain boundary or small grain areas producing very strong light-emitting spots at these areas. The HF/methanol etch produced visibly uniform and strongly light-emitting porous Si over the entire sample. No obvious grain boundary nor grain orientation dependence was observed. The PL and PLE spectra of a HF/methanol etched sample are shown in Fig. 3. In the PLE measurement, the wavelength of the excitation light is varied while the PL intensity is measured at a fixed wavelength of 640 nm. In the PL measurement, the emission spectrum was excited by a 380-nm light. The PL and PLE data shown here were not corrected for the photomultiplier response. The PLE data contain information on the absorption processes in porous silicon which lead to the visible luminescence [6]. A variation of about 20% in PL intensity across the etched area was observed during the measurements. Leaching in HF/HNO_3 solution further enhanced the PL emission but did not further reduce the reflectance of the porous Si.

The reflectance spectra of an unpolished polycrystalline Si wafer and a porous-Si-etched polycrystalline Si wafer are shown in Fig. 4. This porous Si sample was etched in a HF/methanol mixture for 100 min using a current density of 1 mA/cm^2. The average reflectance of the porous Si in the wavelength range from 350 to 850 nm is about 10%. Compared with other polycrystalline Si texturing methods, such as laser texturing, which has a reflection loss of about 5% over the wavelength range of 500 to 900 nm [31], and mechanical grooving, which has a 6.6% reflection loss from 500 to 1000 nm [32], porous Si etching should be able to produce equal or better results once the etching condition is fully optimized for minimum reflectance. The porous Si etching is an extremely simple process and is well suited for a large-area, low-cost solar cell process. It is also important to note that the reflectance of our porous Si-etched sample increases with wavelength above 350 nm whereas the reflectance of mechanically grooved polycrystalline Si decreases with wavelength in this region.

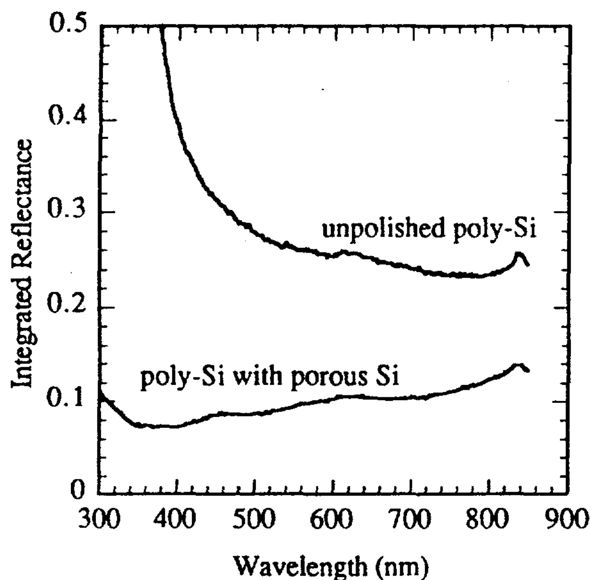

Fig. 4. The reflectance spectra of an unpolished polycrystalline Si wafer and a porous-Si-etched polycrystalline Si wafer.

SUMMARY

We have shown that porous Si provides excellent surface texturing and, thus, light trapping for solar cells. Porous-Si-etched polycrystalline Si has comparable light trapping properties as other much more complicated texturing methods. The cell performance and minority-carrier lifetime measurement results we have so far obtained seem to indicate porous Si-etched wafer surfaces have higher recombination velocities than oxide-passivated surfaces. Further experiments designed to assess the performance of porous Si in photovoltaic device structures are currently in progress.

ACKNOWLEDGMENT

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HIGH EFFICIENCY THIN-FILM $Cu(In,Ga)Se_2$-BASED PHOTOVOLTAIC DEVICES: PROGRESS TOWARDS A UNIVERSAL APPROACH TO ABSORBER FABRICATION

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ABSTRACT

The formation chemistry of $Cu(In,Ga)Se_2$ by several reaction paths has been considered, and growth models of these processes have been developed. The results suggest a simple, reproducible approach to the formation of the multinary compound. The foundation of a universal process for the fabrication of $Cu(In,Ga)Se_2$-based solar cells is presented. Several embodiments of the process make it self-limiting with moderate compositional tolerances and simple endpoint detection. It is applicable to different device structures, and scalable to a variety of hybrid deposition technologies. A growth model is presented that correctly describes this process and related ones. Novel $CuInSe_2$ single-layer and $Cu(In,Ga)Se_2/CuGaSe_2$ multilayer absorber structures have been fabricated by physical vapor deposition using this process. Laboratory-scale photovoltaic devices demonstrate a total-area efficiency of 13.3%.

INTRODUCTION

Photovoltaic (PV) technology based upon polycrystalline thin-film $CuInSe_2$ and related alloys continues to advance towards economic viability with laboratory-scale total-area device efficiencies approaching 14% [1]. Recent advances can be attributed to processing temperatures in excess of 500°C and to the inclusion of either gallium or sulfur to raise the band gap to values more suitably matched to the AM1.5 solar spectrum. To date, the absorbers for the high-efficiency devices are fabricated by either physical vapor deposition (PVD) of the constituent elements, or by the selenization of the metal precursors in H_2Se. PVD is being investigated as a viable technology for the fabrication of $CuInSe_2$-based absorbers by this laboratory [2] and others [3-5]. A successful validation of an "in-line" approach to large-area deposition of high quality $Cu(In,Ga)Se_2$ absorbers resulting in nearly 13% total-area device efficiencies is summarized elsewhere in these proceedings [2]. The selenization process, and variations thereof, have been developed for large-area PV module production by several industrial participants [6-9]. Successful introduction of a profitable product, however, has been hindered by a compound formation chemistry that leads to spatial non-uniformities and poor adhesion to the Mo back contact.

In this paper, the results of characterization efforts on single- and multi-phase $CuInSe_2$-based thin films are presented in the form of a growth model. The growth model accurately describes the formation of $Cu(In,Ga)Se_2$ thin films fabricated here [2] and elsewhere [1, 3-5] by conventional PVD processes. The formation chemistry has been qualitatively examined via several reaction paths. Our findings suggest a simple, reproducible approach to the formation of the multinary compound. The foundation of a simplified universal process for the fabrication of $Cu(In,Ga)Se_2$-based solar cells based on this growth model is presented. Several aspects of the process make it self-limiting with moderate compositional tolerances and simple endpoint detection. A manufacturing scenario is presented that suggest the process is scalable to a variety of hybrid deposition technologies. Novel device structures have been readily fabricated with this process. Specifically, $CuGaSe_2$ and Ga-containing alloys have been incorporated into the absorber in a manner that permits higher Ga contents than previously reported [10]. Results for $CuInSe_2$ and $Cu(In,Ga)Se_2/CuGaSe_2$ device structures are presented. An open-circuit voltage (V_{OC}) parameter near 700 mV [2], in conjunction with total-area efficiency exceeding 12%, and a near record total-area efficiency of 13.3% have been achieved.

EXPERIMENTAL DETAILS

$CuInSe_2$, $CuGaSe_2$ (hereafter referred to as $CuMSe_2$, M=In,Ga), and $Cu(In,Ga)Se_2$ thin films were grown by PVD of the constituent elements under a vacuum of $\approx 10^{-8}$ Pa (10^{-6} torr) onto heated 5-cm x 5-cm bare 7059 and Mo-coated soda-lime silica (SLS) glass. Warping of the SLS substrate at temperatures above 500°C was minimized by the appropriate combination of SLS glass type and thickness, and Mo film deposition parameters. In many cases, an intentional compositional gradient of $\approx$2-15 at.% Cu was introduced across the substrate.

Laboratory-scale PV devices were fabricated by chemical bath deposition (CBD) of $\approx$500 Å of CdS, followed by ion-beam sputtering of 900 Å of intrinsic ZnO and 5000 Å of Al-doped ZnO. The devices were finished by the electrodeposition of a Ni grid with $\approx$ 5% coverage. Current-voltage (I-V) and quantum efficiency measurements were carried out under simulated AM1.5 illumination, and junction behavior was investigated by electron-beam induced current line-scans of completed devices under low injection conditions.

GROWTH MODEL

Previous reports [11,12] identify and describe the multi-phase behavior of Cu-rich $CuMSe_2$. An inspection of the $CuInSe_2$ bulk phase diagram (Fig. 1) suggests the entire $(Cu_2Se)_\delta$-$(CuInSe_2)_{1-\delta}$ two-phase region [13,14] constitutes the most direct chemical path to stoichiometric, high-quality

$CuInSe_2$. The mixture can generally be described as a polycrystalline aggregate with enhanced grain size and orientation, the degree of which relates to the nature of the surface on which it is grown and the relative concentrations of the constituent compounds [15]. The films are highly degenerate with a bulk resistivity ranging between 10^{-3} - 1 Ω-cm, and are of poor PV quality.

In order to produce material suitable for making high performance PV devices from the mixture, the excess binary phase must either be removed or converted to the multinary $CuMSe_2$. Previous studies [16] examined the removal of the Cu_xSe phase and discovered that the resulting structure contained voids through to the Mo back contact, resulting in shorting of the device upon application of the CdS/ZnO window.

We present here a process whereby, first, a $(Cu_2Se)_\delta:(CuMSe_2)_{1-\delta}$ $(0.5<\delta\leq 1)$ mixture is deposited under such conditions so as to produce large-grain $CuMSe_2$ in a host of Cu_xSe. This structure is referred to as the large-grain precursor (LGP). This step is followed by the conversion of the Cu_xSe to $CuMSe_2$ by exposure to In and/or Ga (In,Ga) and Se activity at elevated temperatures. This process is considered novel because the second stage of the process does not require the introduction of Cu into the process chemistry and is the subject of a patent disclosure.

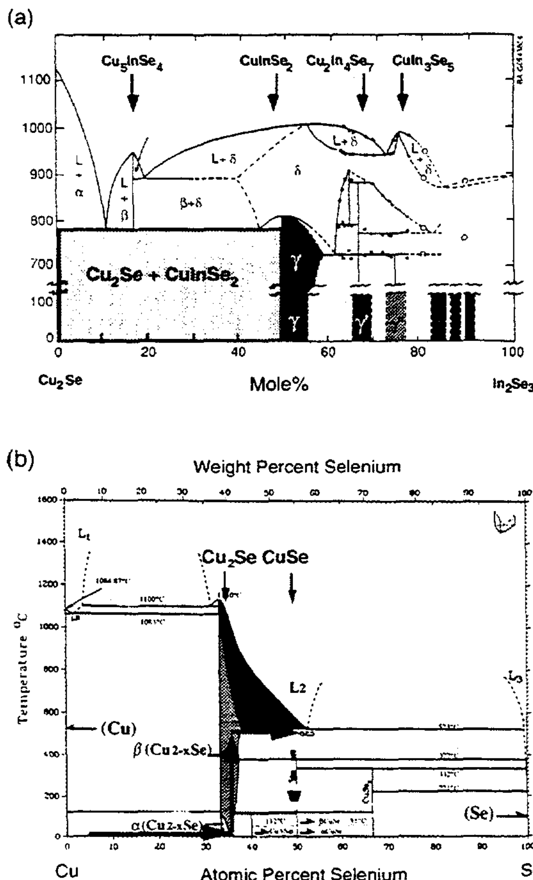


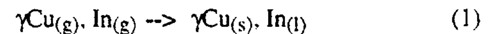
Fig. 1 (a) Cu_2Se-In_2Se_3 pseudobinary, and (b) Cu-Se binary phase diagrams. (After Ref. 13,17)

In order to properly optimize the conversion process, which is responsible for the creation of the absorber at and near the heterointerface, the reaction chemistry, kinetics, thermodynamics, and transport/diffusion mechanisms of the following should be considered: 1) The delivery of the In, Ga, and Se to the LGP; 2) the reaction chemistry at the surface between the (In,Ga) and Se and the host LGP structure; 3) the diffusion/transport of the reacted (In_ySe, $CuIn_xSe_y$) and unreacted (In, Ga, Se) species away from the surface; 4) the nucleation and growth of the solid species in solution; and 5) the resulting net concentration of unreacted elemental and binary species. Such an examination, however, is beyond the scope of this paper. Instead, a qualitative argument that suggests a simple, direct path to high quality $Cu(In,Ga)Se_2$ is provided.

To study the properties of the LGP and the Cu_xSe-to-$CuMSe_2$ conversion process, films were fabricated over a wide compositional range and with large compositional gradients across the substrate. The details of this work and supporting data for the growth model presented here is the subject of current [18,19] and previous [4,11,12,15,16,20] publications.

Growth Model

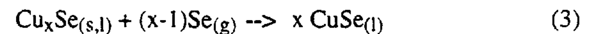
In Figs. 2 and 3, a model is presented for the growth of high-quality thin-film $CuInSe_2$-based PV material. The formation chemistry is described from the perspective of PVD. The model qualitatively describes the process for the formation of Cu-rich $CuGaSe_2$ and $Cu(In,Ga)Se_2$ as well. The intent of the first stage of the process (Fig. 2) is to produce a mixed-phase enhanced-grain precursor of $CuInSe_2$ and Cu_xSe. The following reaction chemistry applies (described for Cu:In flux ratio = $\gamma \geq 1$);



$$\gamma Cu_{(g)}, In_{(g)} \rightarrow \gamma Cu_{(s)}, In_{(l)} \quad (1)$$

$$xCu_{(s)} + {}^1/_y Se_{y(g)} \rightarrow Cu_xSe_{(s,l)}, \ (1\leq x\leq 2) \quad (2)$$

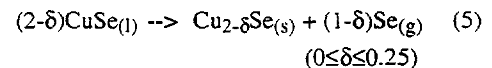
For $T_{sub} \geq 500°C$,



$$Cu_xSe_{(s,l)} + (x-1)Se_{(g)} \rightarrow x\, CuSe_{(l)} \quad (3)$$

$$\gamma CuSe_{(l)} + In_{(l)} + Se_{(g)} \rightarrow CuInSe_{2(s)} + (\gamma-1)CuSe_{(l)} \quad (4)$$

Upon cooling,



$$(2-\delta)CuSe_{(l)} \rightarrow Cu_{2-\delta}Se_{(s)} + (1-\delta)Se_{(g)} \quad (5) \quad (0\leq\delta\leq 0.25)$$

where x in (2) and (3) signifies the variable composition of the Cu-Se binary during growth, and δ in (5) represents a specific phase identified by x-ray diffraction (XRD)..

The above-described reaction path requires some additional discussion. Initially, Cu and In metals are the only constituents to accommodate on the ≈500°C substrate surface [eq. (1)]. It was previously believed [16] that each metal would subsequently selenize, in the presence of Se vapor, into Cu_xSe and In_ySe binaries, followed by the formation of $CuInSe_2$ from the binaries. Recent studies on the reaction rates of Cu and In in the presence of Se vapor [21] indicate that Cu selenizes faster than In. On inspection of the Cu-Se binary phase diagram (Fig. 1), the likely candidate for early formation is the $Cu_{2-\delta}Se$ solid phase. In the presence of an over-pressure of Se and at substrate temperatures in excess of 500°C, the formation of the liquid CuSe phase occurs according to eq. (3). It

therefore appears that the growth of the ternary $CuInSe_2$ proceeds in a liquid environment of the excess Cu_xSe binary phase. This accounts for the observed enhanced-grain nature of the aggregate mixture [15].

The compound formation may now readily proceed according to eq. (4), which is thermodynamically more favorable than the reactions between the Cu-Se and In-Se binaries according to calculations made by Albin et. al [22]. If the film is cooled, the liquid CuSe phase would liberate Se according to eq. (5), leaving the $Cu_{2-\delta}Se$ solid phase. This phase has been detected by XRD [16] and its presence is consistent with compositional analysis.

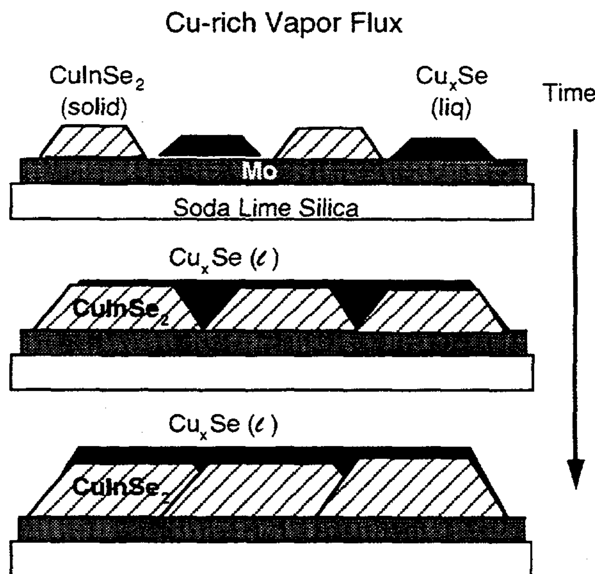


Fig. 2 Growth model for Cu-rich $CuInSe_2$ by physical vapor deposition.

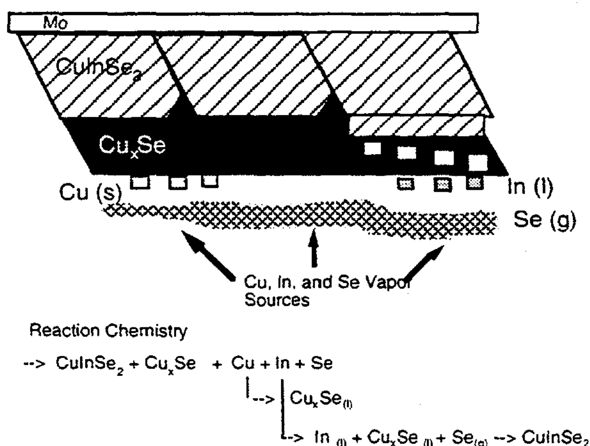


Fig. 3 Growth model for the conversion of Cu_xSe into $CuInSe_2$ by exposure to an In-rich vapor trail. The substrate is inverted to represent the orientation during growth.

The subsequent stages of film growth are a combination of reaction chemistry and film formation dynamics. This is illustrated in Fig. 2. The liquid (CuSe) - solid ($CuInSe_2$) phase separation occurs parallel to the substrate plane during the initial stages of growth. As the $CuInSe_2$ solid coalesces, the surface tension between the liquid and solid phases increases and reaches a critical value [23], at which time the phase separation transforms to an orientation normal to the substrate plane. The result is a layered structure with the Cu_xSe is at the surface. This facilitates the conversion of the Cu_xSe to $CuInSe_2$ during subsequent processing. This mixed-phase structure, as will be suggested below, can be created by other deposition techniques.

The second, and most critical, stage of the process involves the conversion of Cu_xSe to $CuInSe_2$ (Fig. 3). This requires an In-rich or In-exclusive (relative to Cu) medium. to consume the excess Cu_xSe by the equivalent reaction chemistry as described in eq. (4). If Cu is present in this stage, the mass balance is modified only by the addition of Cu_xSe to the pool. In this study, however, Cu is deemed unnecessary during the conversion process and is excluded from the vapor trail. The device results presented below suggest that material produced in this manner is of equal or superior quality to that produced by conventional methods that require Cu. The exclusion of Cu from the final stages of film formation has clear ramifications on the application of the process to manufacturing.

The presence of a liquid CuSe phase simplifies the diffusion/transport and reaction kinetic issues discussed earlier. As Fig. 3 depicts, the $CuInSe_2$ is formed and transported in solution to the liquid-solid interface, where epitaxial growth continues. The continuity of the $CuInSe_2$ crystallite normal to the substrate plane, as observed in morphological studies [15], is consistent with such a growth mechanism.

As the conversion process nears completion, the surface coverage of liquid Cu_xSe is incomplete and solid regions with a surface composition of $CuIn_3Se_5$ [4,19] will appear. Thus, there exists both a liquid Cu_xSe and a solid $CuIn_3Se_5$ surface on which the additional In and Se can react. In order to minimize the incorporation of excess In into the solid bulk regions (in contrast to the liquid Cu_xSe regions where the reaction chemistry described above will still hold), the Se/In vapor ratio is lowered to encourage the formation and subsequent volatilization of Se-poor In-Se compounds and discourage the formation of stable In_2Se_3 phases that may diffuse into the bulk and drive the composition Cu-poor. In this way, the process is self-limiting and stabilizes to a uniform $CuInSe_2/CuIn_3Se_5$ bulk/surface composition. The change in surface chemistry is also conducive to an end-point detection scheme that either observes a transition in surface composition or state (liquid -> solid).

With this approach to absorber fabrication in mind, it is germane to consider the application of the growth process to a manufacturing environment. In Fig. 4, several scenarios are presented whereby the first stage involves the fabrication of a mixed-phase precursor film followed by the introduction of In and/or Ga and Se for the second-stage conversion process. The vision here is that the intermediate LGP structure is achievable by the concurrent or sequential deposition of the elemental or

compound constituents without initial regard to quality or composition. When this deposition, or series of depositions, is accomplished in, or followed by, an anneal in a Se environment, the desired LGP structure is achieved. At this stage, either previous process control or in-line diagnostics can determine the Cu-excess and hence the level of In and/or Ga activity that is required to produce a high quality absorber. The termination of the process would occur upon the observation of a transition in surface chemistry from Cu_xSe to $CuIn_3Se_5$ or in surface state from a liquid to solid. The prospect of real-time process control for the fabrication of $CuInSe_2$-based modules would accelerate the introduction of a profitable product. Our laboratories at NREL are presently validating several of these approaches.

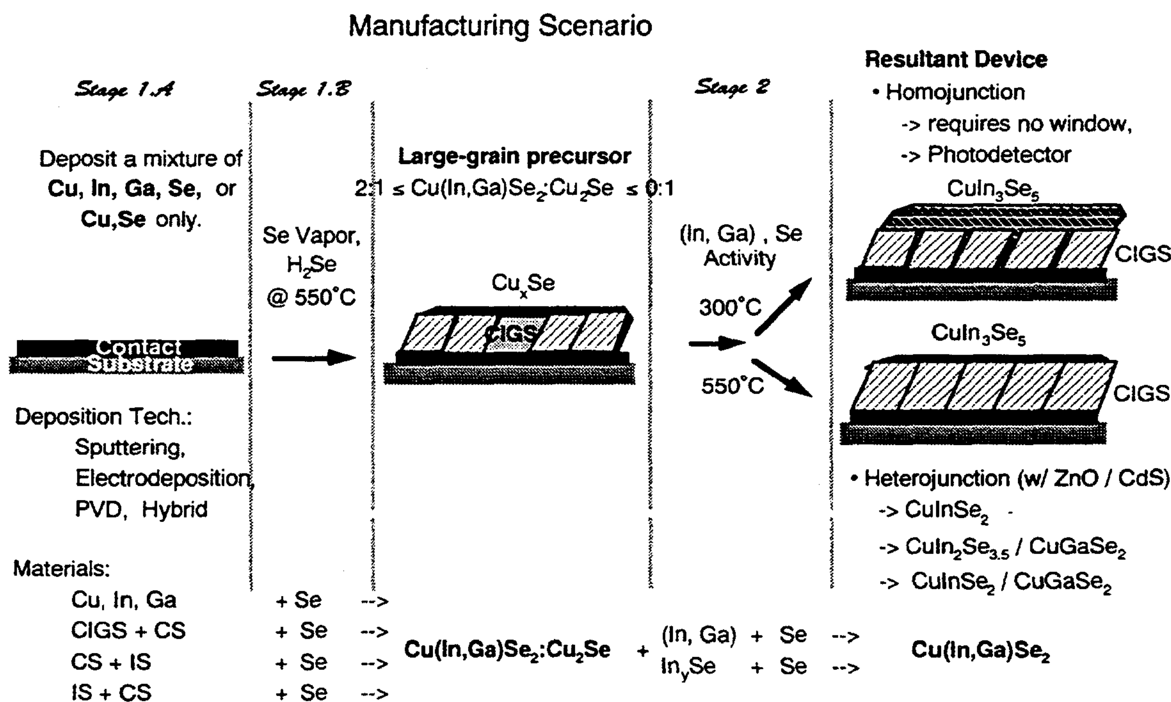


Fig. 4 A scenario for the manufacturing of $Cu(In,Ga)Se_2$ solar cells utilizing the above described two-stage process.

DEVICE STRUCTURES AND CHARACTERIZATION

In this investigation, improvements on state-of-the-art device efficiencies have been examined from two perspectives. For a given absorber band gap, V_{oc} may be increased by improving the absorber quality, by enhancing grain size to reduce losses at grain boundaries, or by reducing forward currents that result from injected minority carriers into the space charge or from recombination at the back contact. Another approach is to increase the band gap of the $CuInSe_2$ absorber by alloying with a higher-band-gap ternary such as $CuGaSe_2$ (E_g = 1.7 eV) and/or $CuInS_2$ (E_g = 1.5 eV). Ideally, the composition may be tuned to achieve a band gap close to the optimum value of ~1.4eV, where it is optimally matched to the terrestrial AM1.5 solar spectrum. In practice, however, Ga contents (relative to the total Ga+In) greater than about 27% within a homogeneous absorber degrade the device performance [10] by drastically reducing the carrier collection efficiency. The $ZnO/[Cd,Zn]S/CuIn_{0.73}Ga_{0.27}Se_2/Mo$ device structure described in [1] demonstrates both the improvement achieved relative to $CuInSe_2$ with a $h_{total\ area}$ of 13.7% and a V_{oc} of 546 mV, and also represents the upper limit in Ga content for homogeneous $CuIn_{1-x}Ga_xSe_2$ solar cells.

In this paper, a hybrid approach is discussed that incorporates higher Ga contents throughout much of the absorber, resulting in enhanced performance relative to a $CuInSe_2$ standard. Two alternative absorber structures are presently being investigated. They are described schematically below in Fig. 5. Similar structures fabricated by Contreras and co-workers using the "in-line" variable-flux process are presented elsewhere in these proceedings [2] and have successfully produced devices with nearly 13% total area efficiency. The intent in either case is to introduce a 1.7 eV $CuGaSe_2$ layer adjacent to the back contact of such a thickness to reduce back-surface recombination and/or confine forward injected carriers. The remainder of the absorber is either $CuInSe_2$ or $CuIn_{0.75}Ga_{0.25}Se_2$. The relative amounts of each are quoted as a percentage of the total volume, determined by the percentage of Ga_{total} and $(Ga+In)_{total}$ delivered to the substrate during each stage. The structures are fabricated by the process described herein and the transition between layers is designed to be abrupt. The temperature profile is as follows: T_{sub} is ramped from 500°C to 550°C during the first stage of the process, and held at 550°C during the second stage.

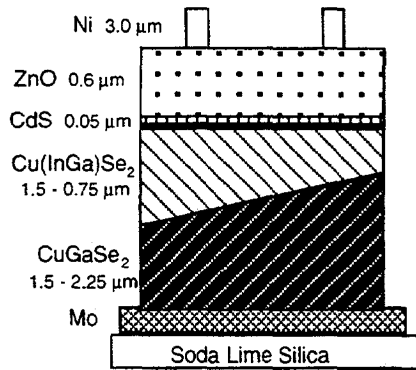


Fig. 5 $CuInSe_2/CuGaSe_2$ and $Cu(In,Ga)Se_2/CuGaSe_2$ device structures characterized below.

Table 1. Summary of device results. These devices are referred to in Figs. 6 & 7 as (a) - (e), respectively.

Absorber (Layer fraction)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF	η (total area)	A	J_0
CIS	450	36.6	72.2	11.9	1.5	8.9e-8
CIS/CGS (0.5 / 0.5)	490	37.6	69.3	12.8	1.7	6.5e-7
CIS/CGS (0.25 / 0.75)	526	30.8	65.6	10.6	2.0	1.1e-6
CIGS/CGS (0.35 / 0.65) w/ CIS cap	573	32.8	70.8	13.3	1.6	4.7e-8
CIGS/CGS (0.35 / 0.65)	627	28.6	65.7	11.8	2.4	1.1e-6

In Table 1, results are summarized for several absorber structures. In Figs. 6 & 7, the quantum efficiency and I-V characteristics of these structures are compared. Several conclusions may be drawn from these data. A systematic shift in V_{oc} to higher values is observed as the $CuGaSe_2$ layer gets closer to the heterointerface. This is true for both the $CuInSe_2$ and $Cu(In,Ga)Se_2$ surface layers. In the case of $CuInSe_2$ surface layers (Figs. 6 & 7, (a) - (c)), Ga is not detected at the surface of the sample by Auger electron spectroscopy (AES). The increase in V_{oc} is therefore not associated with a larger band gap of the absorber at the heterointerface, but is due to a decrease in injected forward current due to carrier confinement. Concurrent with an increase in V_{oc} is a decrease in J_{sc} consistent with the QE measurements of Fig. 6. The increase in near-infrared losses is indicative of a shrinking space-charge and/or of Ga diffusion towards the surface with associated generation losses.

A puzzling observation is the shift in the band edge for those devices without any detectable Ga at the surface (Fig. 6 (a) - (c)). For stoichiometric films grown in a Cu-rich environment without Ga, Cu_{In} and In_{Cu} compensating defect pairs are known to exist and give rise to Cu-Pt ordering [24]. If these defects are not ordered in the bulk, then they are of sufficient density to produce "banding" of defect levels and a decrease in the optical band gap. If a source of Ga is present in the bulk, producing Ga concentrations in the $CuInSe_2$ at a doping level ($< 10^{20}$ cm^{-3}) rather than at an alloying level ($> 10^{20}$ cm^{-3}), the Ga may act to retard the formation of the native defects, with a resulting increase in the optical absorption edge.

By incorporating Ga into the near-surface layer as well (Fig. 6 and 7, (d), (e)), device performance is generally enhanced. The difference between the two structures is that the total Ga content of sample (d) is less than that of (e), and sample (d) has an In enriched surface relative to the underlying material. An NREL-confirmed total-area device efficiency of 13.3% has been achieved. This translates to an ≈14% active area efficiency.

There is significant room for improvement in J_{sc} of the Ga-based devices. This will be realized when the interdiffusion of Ga and In is controlled so as to optimize the carrier generation in the near-surface region of the absorber. It is felt that total area device efficiencies in excess of 14% are readily attainable with these structures.

DISCUSSION

The process presented here for the fabrication of $Cu(In,Ga)Se_2$ PV material has the potential for application to industrial-scale systems. The material has produced state-of-the-art solar cells that exhibit good uniformity and reproducibility. The adhesion of the film to the Mo back contact is superior to that fabricated by selenization of the metal precursors. The process is simple and conducive to the production of multilayer absorber structures. In fact, lower processing temperatures during stage 2 of the process produce absorbers that do not require the use of a CdS and ZnO window, although their performance is inferior to those produced at higher temperatures.

Fabrication of $Cu(In,Ga)Se_2/CuGaSe_2$ layered structures by this process has shed light on the device performance dynamics. A higher-band-gap material inserted at the back of the absorber consistently increases V_{oc} relative to absorbers without the $CuGaSe_2$. The mechanism is believed to be a reduction in injected forward currents due to carrier confinement in the space-charge. Systematic studies are presently under way to further elucidate the role of Ga in the absorber and to validate the absorber fabrication process for industrial application.

ACKNOWLEDGEMENTS

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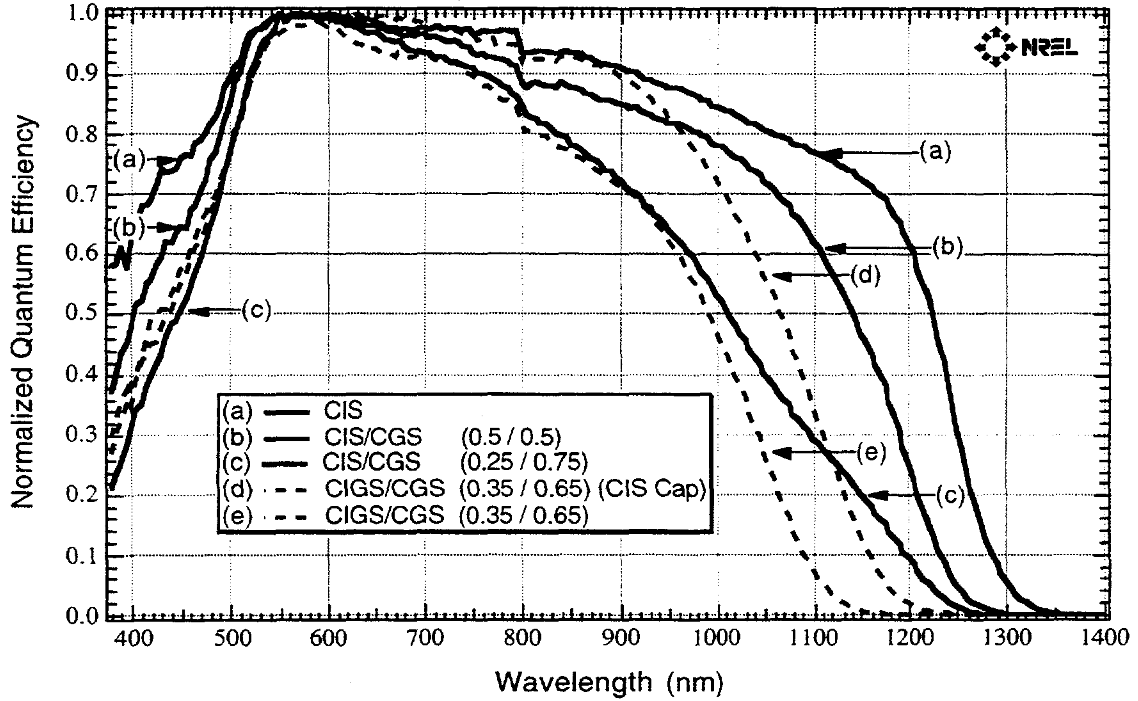

Fig. 6 Normalized quantum efficiency measurements for $CuInSe_2/CuGaSe_2$ (solid lines) and $Cu(In,Ga)Se_2/CuGaSe_2$ (dashed lines) absorber structures.

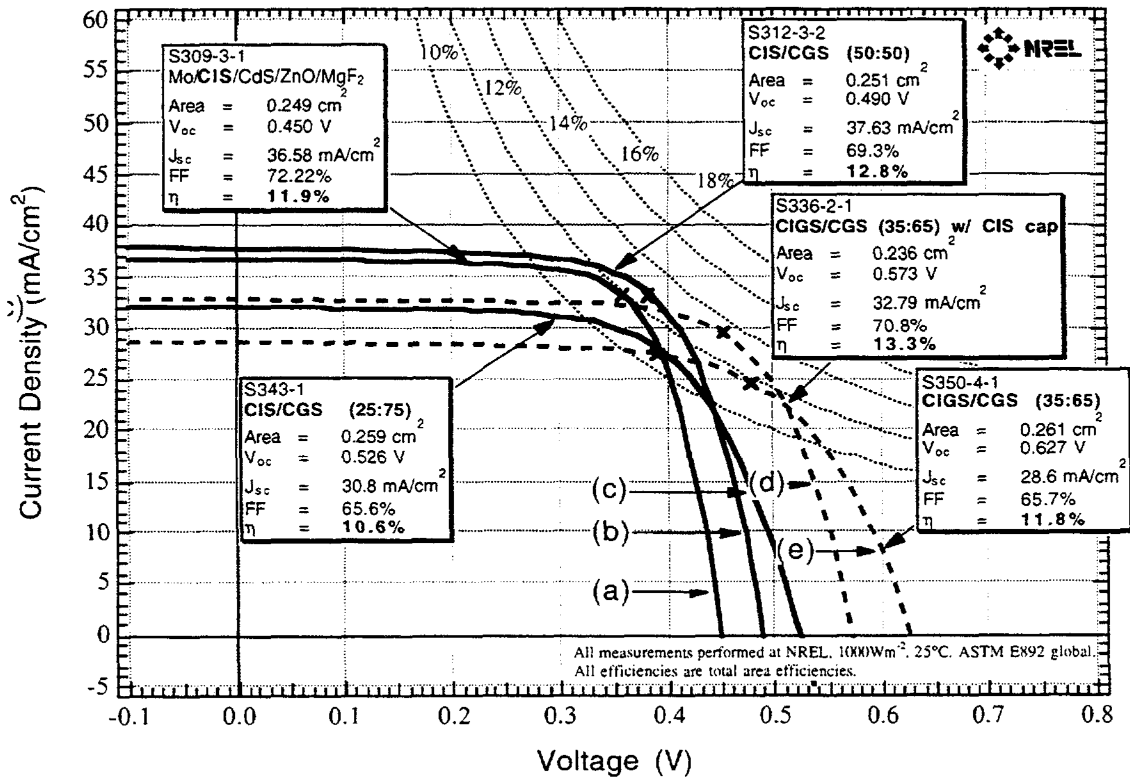

Fig. 7 I-V measurements for $CuInSe_2/CuGaSe_2$ (solid lines) and $Cu(In,Ga)Se_2/CuGaSe_2$ (dashed lines) absorber structures. The structures (a) - (e) are described in Figure 6.

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PROGRESS IN PHASES 2 AND 3 OF THE PHOTOVOLTAIC MANUFACTURING TECHNOLOGY PROJECT (PVMAT)

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ABSTRACT

The first year of the process-specific activities of the Photovoltaic Manufacturing Technology (PVMaT) project has been completed, and the first subcontracts for teamed efforts on R&D of a general nature have been awarded. A second solicitation for process-specific research and development (R&D) is in the evaluation stage for award of subcontracts. This paper describes the technical accomplishments of the first process-specific subcontracts (Phase 2A), the status of the teamed research (Phase 3A), and the status of the solicitation for the second process-specific solicitation (Phases 2B).

INTRODUCTION

As has been described previously [1], the Photovoltaic Manufacturing Technology project (PVMaT) is a government/industry R&D partnership composed of joint efforts between the federal government (through the U.S. Department of Energy) and members of the U.S. photovoltaic (PV) industry. The project's immediate goal is to assist U.S. industry in retaining and extending its world leadership role in the manufacture and commercial development of PV components and systems. PVMaT is designed to do this by helping the U.S. PV industry improve manufacturing processes, accelerate manufacturing cost reductions for PV modules, improve commercial product performance, and lay the groundwork for a substantial scale-up of U.S.-based PV manufacturing plant capacities.

PVMaT is being carried out in three separate phases, each designed to address separate research and developent (R&D) requirements for achieving PVMaT goals. Phase 1 was a problem-identification phase of about 3-months duration. In Phase 1, the status and needs of the U.S. PV manufacturing industry were identified, and the development of Phase 2 procurement responsive to the industry's needs was initiated. Phase 1 was completed in 1991.

Phase 2, the problem solution phase, which addresses process-specific problems of specific manufacturers, is now under way with an expected duration of 5 years. The first solicitation under this phase (PVMaT 2A) was open only to those organizations that received awards in the Phase 1 solicitation, and seven resulting subcontracts were implemented in early 1992. The subcontracts are cost-shared between the U.S. government and U.S. industrial participants. Technical accomplishments for the first year of PVMaT 2A are presented below. Proposals for a second, overlapping, and similar process-specific solicitation (PVMaT 2B) were due in September of 1992. This second Phase 2 solicitation is in the evaluation stage, with awards planned for later this year. PVMaT 2B was open to all U.S. PV industrial firms, thus giving organizations that were not ready for the first Phase 2 procurement cycle another chance to "ramp on" and participate in the solution phase of the program.

Phase 3 addresses R&D problems that are relatively common to a number of PV companies or the PV industry as a whole. These "generic" problem areas are being addressed through a teamed-research approach. A solicitation (Phase 3A) for these teamed research efforts was released in October 1991. Two subcontracts for Phase 3A have recently been awarded. These research organizations are focusing on module-related R&D problems found to be common to a significant set of PV manufacturers, and these subcontract activities are described below.

PVMaT PROGRESS

Phase 2A

The winners in PVMaT 2A are listed in the Table 1 below. Following Table 1 is a description of the seven subcontractor projects and their first year PVMaT accomplishments.

Siemens Solar Industries Photovoltaic Cz Silicon Manufacturing Technology Improvements -Siemens Solar Industries (SSI) is improving Cz Si-ingot quality; increasing the materials use efficiency for crystalline-silicon (c-Si) wafer sawing; investigating improvements in device processing; investigating the introduction of automation to a significant portion of their c-Si module manufacturing lines; and reducing the amount of hazardous waste gener-

Table 1: PVMaT Phase 2A Participants

Subcontractor	Subcontract Title	Principal Investigator
Siemens Solar Industries Camarillo, California	*Photovoltaic Cz Silicon Manufacturing Technology Improvements*	T. Jester
Solarex Corporation Newtown, Pennsylvania	*Large-Area, Triple-Junction, a-Si Alloy Production Scale-Up Project*	R. Oswald
Mobil Solar Energy Corporation Billerica, Massachusetts	*Thin Edge-Defined Film-Fed Growth (EFG) Octagons*	J. Kalejs
ENTECH, Inc. Dallas, Texas	*Photovoltaic Manufacturing Technology (PVMaT) Improvements for ENTECH's Concentrator Module*	M. O'Neill
AstroPower, Inc. Newark, Delaware	*Silicon-Film Photovoltaic Manufacturing Technology*	W. Bottenberg
Utility Power Group Chatsworth, California	*a:Si Photovoltaic Manufacturing Technology— Phase 2A*	G. Duran
Energy Conversion Devices Troy, Michigan	*Continuous Roll-to-Roll Amorphous Silicon Photovoltaic Manufacturing Technology*	M. Izu

ated. This effort is being addressed in three 1-year phases. Successful implementation of this program will result in decreasing SSI's c-Si module cost by more than half while doubling its U.S. manufacturing capability. SSI's accomplishments during the first phase of this subcontract include an increase in wire-saw production capacity by over 30% due to reduced kerf loss and thinner wafer processing; an increase in crystal-growth yields through polysilicon studies; elimination of Freon and replacement with a no-clean solder paste in SSI's module production by April 1993; and incorporation of graphite design changes into the SSI's crystal growers, resulting in a 30% cost savings ($300K/yr).

Solarex Corporation Large-Area, Triple-Junction, a-Si Alloy Production Scale-Up Project - Solarex Corporation is improving the deposition and quality of its transparent front contact; optimizing its laser patterning process; scaling up the semiconductor deposition process; improving the back contact deposition; and scaling up and improving the encapsulation and testing of its a-Si:H modules. Successful implementation of this 3-year program will result in Solarex producing ≥0.56-m² (6-ft²), 10% stabilized efficiency, 75-W a-Si:H modules with a total overall module yield of ≥75%. At a proposed production capacity of 10 MW/year, this would result in a potential cost reduction from the present price of $\$11.05/W_p$ to $\$1.14/W_p$. Solarex's accomplishments during the first phase of this subcontract include; the design of an ≥0.56-m² (6-ft²) plasma-enhanced chemical vapor deposition (PECVD) a-Si:H based deposition system; completion of light soaking tests; demonstration of a new laser-scribing system that does not cause module failures in the wet hi-pot tests; and the fabrication of a Frit Dispenser used in Solarex module fabrication.

Mobil Solar Energy Corporation Thin Edge-Defined Film-Fed Growth (EFG) Octagons -Mobil Solar Energy Corporation (MSEC) is reducing the cost of solar cell processing through a 50% reduction in its EFG Si-wafer thickness; increasing the throughput of the laser-cutting of the wafers; increasing the mechanical strength, and thus yield, of the wafers; and evaluating integrated computer-aided manufacturing control programs for the MSEC crystal growth manufacturing line to enhance productivity. Successful implementation of this 3-year program will allow Mobil Solar to produce octagonal Si tubes, producing 200-µm-thick Si wafers with a thickness variation of ±50 µm. The previous minimum wafer thickness for this process was 400 µm. MSEC will also develop laser wafer-cutting capabilities resulting in the processing of 12 wafers per minute. Its accomplishments during the first phase of this subcontract include testing and analysis that indicate potential materials cost reductions of 15% due to wafer thickness, 10% due to wafer flatness improvement, and 25% due to a growth rate; completing specifications for a factory prototype EFG octagon crystal growth furnace for 300-µm-thick Si wafers; designing and testing a laser cutting station that will increase pilot production line throughput by a factor of two; and demonstration of the cutting feasibility of silicon wafers near the low-damage threshold with a 585-nm high-power dye laser.

ENTECH, Incorporated Photovoltaic Manufacturing Technology Improvements for ENTECH's Concentrator Module - ENTECH is automating a significant portion of its manufacturing line, aiding key ENTECH vendors in improving the vendors'

technologies; scaling up the ENTECH manufacturing line to accommodate large volume production; and addressing ES&H issues throughout all of the associated manufacturing processes. The effort is being addressed in two 1-year phases. Successful implementation of this program will result in an initial linear concentrator module manufacturing plant with the capability of producing PV modules at a rate of 10 MW/yr. ENTECH's accomplishments during the first phase of this subcontract include; the development of laboratory prototype work stations for PV cell assemblies and receivers; the identification and delivery of process-compatible advanced-cell samples from four separate vendors; the development of an improved prismatic lens cover for cells that resulted in a 90% reduction in both material and labor costs for that step; the development of a continuous, prelaminated, rolled Fresnel lens that resulted in both a 20% materials cost reduction and the elimination of solvent use in the ENTECH process; and development of ribbon solder techniques that have resulted in an 80% reduction in materials costs with additional savings in labor.

AstroPower, Incorporated Silicon-Film® Photovoltaic Manufacturing Technology - AstroPower is enhancing its Silicon-Film® wafer production capabilities, optimizing its solar cell processing, and improving the polycrystalline silicon-film module assembly portion of its manufacturing line. Successful implementation of this 3-year program will result in an upgrade to AstroPower's facility that will allow it to reach a production rate of 19 MW/yr of 1.22-m^2 polycrystalline silicon modules with an output of 170 W_p each by the mid-1990s. AstroPower's accomplishments during the first phase of this subcontract include the demonstration an 8.8% efficient 10-cm x 10-cm Silicon-Film® solar cell; the fabrication of the first 15-cm x 45-cm Silicon-Film® cell (the largest solar cell ever produced); the demonstration of a 0.48-MW/yr Silicon-Film® machine operation rate, and 74% silicon feedstock use efficiency; the initial planning for 2.4-MW/year wafer fabrication machine; and planning for the introduction of new 225-cm^2 Silicon-Film® solar cell product in 1993.

Utility Power Group a:Si Photovoltaic Manufacturing Technology—Phase 2A - The Utility Power Group (UPG) is conducting research on encapsulation of their a-Si:H modules, with consideration given to approaches that do not require a second glass layer, and automation of module termination. Additionally, UPG's lower-tier subcontractor, Advanced Photovoltaic Systems (APS), is optimizing the automation of its Eureka® manufacturing line; improving the encapsulation of the Eureka® module, and introducing real-time processing and quality control to the Eureka® production line. Successful implementation of this 3-year effort will result in increasing the module manufacturing yield over the current level by 35% while decreasing the direct cost by about 25%. The accomplishments of the UPG-APS team during the first phase of this subcontract include the completion of POWERGLASS module qualification testing for candidate encapsulation materials; reduced POWERGLASS module termination and encapsulation manufacturing costs by 50%; the introduction of three new Eureka® module products (25-W and 50-W products for 12-V applications); completion of the automation of about 60% of the Eureka® production encapsulation line; and completion of a design for full-scale enhanced Eureka® modules.

Energy Conversion Devices, Incorporated Continuous Roll-to-Roll Amorphous Silicon Photovoltaic Manufacturing Technology - Energy Conversion Devices (ECD) is developing the production of 0.3-m x 1.22-m (1-ft x 4-ft) triple-junction a-Si-Ge alloy modules with 11% stable efficiency, reducing its manufacturing costs through utilization of its high deposition rate techniques to enhance the production throughput, and reducing material and labor costs. The effort is being addressed in three 1-year phases. Successful implementation of this program will allow ECD to work toward an ultimate goal of building a 100-MW/yr roll-to-roll, automated a-Si module manufacturing facility. At this anticipated production capacity, ECD could reduce the cost of PV-generated electricity to less than $1.00/$W_p$. ECD's accomplishments during the first phase of this subcontract include completion of improvements to the ECD a-Si-Ge alloy deposition system, establishing the first roll-to-roll a-Si-Ge production line facility; demonstration of 7.2% stabilized efficiency on ≥1.22-m (4-ft^2) triple-junction a-Si alloy modules; and significant efforts toward increasing the effective manufacturing throughput.

Phase 3A

The winners in PVMaT 3A are listed in the Table 2 below. Both contracts began in early January 1993. Following Table 2 is a description of the seven subcontractor projects.

Spire Corporation Automated Solar Cell Assembly Teamed Process Research - Spire will conduct manufacturing R&D to improve crystalline and polycrystalline Si PV module manufacturing processes with a goal of substantially reducing module manufacturing costs. Areas that will be addressed include processing

Table 2: PVMaT Phase 3A Participants

Subcontractor	Subcontract Title	Principal Investigator
Spire Corporation Bedford, Massachusetts	*Automated Solar Cell Assembly Teamed Process Research*	M. Nowlan
Springborn Laboratories, Inc. Enfield, Connecticut	*Photovoltaic Manufacturing Technology (PVMaT)*	W. Holley

rates, process control, yield, throughput, material utilization efficiency, and increased use of automation. These issues are being addressed for thin (≤ 200-μm) silicon wafers. To conduct these efforts, Spire will team with Solec International (a PV module manufacturer) and the University of Massachusetts-Lowell/Center for Productivity Enhancement (automation specialists) who will act as lower-tier subcontractors. The effort is being addressed in two, 1-year phases.

Springborn Laboratories Photovoltaic Manufacturing Technology (PVMaT) - Springborn will try to solve problems related to the PV module encapsulant ethylene-vinyl-acetate (EVA) discoloration and/or degradation. Areas that will be addressed include a case history study and problem definition, identification of discoloration and/or degradation mechanisms, development of EVA-stabilization strategies, accelerated testing of new laminates, and pilot scale production and field-testing of new laminates. To conduct these efforts, Springborn is teaming with the SSI; Photocomm, Inc.; United Solar Systems Corp.; Solarex Corp.; Texas Instruments; Solec International, Inc.; UPG; APS; Global Photovoltaic Specialists, Inc.; Arizona State University; Arizona Public Service Company; and the University of Connecticut. The effort is being addressed in three 1-year phases.

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PERSPECTIVES AND OPPORTUNITIES IN POLYCRYSTALLINE THIN-FILM PHOTOVOLTAIC TECHNOLOGIES

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ABSTRACT

During the last 2 years we have seen great turmoil in photovoltaics (PV) in general and in polycrystalline thin films (PTF) in particular. Companies have left the field (e.g., AMETEK) or sustained delays or major reorganizations (Siemens Solar, Boeing); others (ACX Technologies, Energy Photovoltaics, Martin Marietta, Solar Cells, Inc. and Solarex) have entered it, and some others (Photon Energy, now Golden Photon) have found new and stronger owners. Major technical advances have occurred in PTF (solar cell efficiencies have risen by about 2% absolute, to nearly 16%; modules of substantial size (7200-cm^2, 8-ft^2) are being made at efficiencies near or above the state-of-the-art for thin films) and some major technical issues have been encountered. We have seen a series of excellent performance results (as with CdTe), and we have seen manufacturability issues humble the still very promising CIS technology. The challenges of developing and commercializing a successful thin film remain. This paper describes the opportunity of PTF technologies to do so and the technical and market contexts that are likely to play a decisive part in whether they succeed.

TODAY'S COMMERCIAL STATUS

With a minor exception, polycrystalline thin-film (PTF) technologies based on CIS, CdTe, and silicon-film are not commercially available. The exception is about 1 MW/year of CdTe cells fabricated by Matsushita Battery for Texas Instruments calculators and other consumer applications [1]. These cells have been in use for almost a decade. But in terms of mainstream PV for power applications, no PTF modules can be bought off-the-shelf.

Commercialization of PTF power modules is underway along several fronts. Several companies have agreements with PVUSA to deliver 20 kW systems for the PVUSA "emerging module technologies" program. However, system deliveries for this program have been plagued by significant delays (1 to 3 years). The delays have been caused by a variety of issues, including some related to processes and others having to do with module-level shortcomings. In any case, no PTF modules have yet been delivered to PVUSA, causing a loss of credibility for the various PTF groups.

A similar set of PTF module delivery agreements have now been made between NREL and various U.S. companies. These call for about 1 kW to be delivered to NREL for testing. In some cases, this testing is part of the PVUSA qualification process. In others, it represents an independent effort to assist industry to overcome product-introduction issues without encountering the kind of public disappointment associated with failing to deliver a system for PVUSA. Because new products based on PTF technologies are in their developmental phase, this kind of "behind the fence" approach is probably realistic. Indeed, it is just an extension of an existing process by which U.S. companies (many of them funded by U.S. DOE through NREL) interact with NREL to test their PTF modules as they are developed. For example, we have had about 150 W of CIS modules from Siemens Solar outdoors at NREL for over a year, and others (CIS and CdTe) for several years.

The PTF technologies remain in a precommercial stage. Current plans exist by two U.S. CdTe companies to manufacture modules. Golden Photon, Inc. (GPI) has announced a new facility in Golden, Colorado; and Solar Cells, Inc. (SCI) has announced a facility in Toledo, Ohio. No U.S. CIS company has made an official announcement of a commercial manufacturing facility, and introduction of silicon-film awaits further developments at AstroPower. Indeed, it is unlikely that commercialization of CdTe will go smoothly, since the introduction of a new PV technology has many challenges. Recent experience in CIS (and ongoing difficulties in amorphous silicon, e.g., stability) show that new thin films face numerous barriers.

The economics of PV, and of thin films in particular, do not support an easy transition to successful commercialization. This is because thin films have been developed as a means of reducing the cost of PV to compete for large power markets. However, the initial entry of thin films is at much higher prices that cannot yet compete for these presumed large markets. The problem is that initial production of thin films occurs at (1) lower than expected efficiencies (due to the relative immaturity of manufacturing capability) and (2) at low volumes that fail to take advantage of economies-of-scale. In addition, the start-up costs of many years of R&D (without any offsetting sales revenues) as well as the need to keep a major ongoing R&D staff (to reach potential performance and cost goals) are serious financial burdens. Thus, instead of being inexpensive and immediately penetrating very large power markets (U.S. peak shaving and developing countries rural electrification), thin films must instead compete for traditional PV markets against established PV options. These and other market-related factors make it hard for new PTF companies to muster the kind of investment needed to ensure success. The serious PTF

companies remain relatively ahead of their time in comparison with mainstream U.S. commercial ventures. Their saving grace is that they may be correct in their technological positioning, with the concomitant reward for their investment risk.

U.S. government cost-shared programs are playing a substantial role in the development of PTF options [2-9]. For example, the recent emergence of CdTe as a commercial possibility results from the technological incubation of the last decade, carried out by the private sector with U.S. DOE/NREL support. This support continues through the NREL Polycrystalline Thin Film Program (subcontracts with GPI and SCI, and with several U.S. universities) and through potential support from other U.S. DOE-sponsored programs (e.g., possible funding from PVMaT, PV Bonus and others). The formal U.S. support of CdTe has an important role, especially considering the fragility of initial commercialization efforts and the need for ongoing technical progress to achieve true, longer term competitiveness with conventional energy sources.

Probably the best hope of the PTF commercialization effort is that it is based on (1) a set of technical options that allow truly low cost to eventually be achieved and (2) a significant track record of technical achievements at the cell, module, and processing levels. These achievements, and the cost question, are addressed in the following sections.

MODULES, PROCESSES, AND RELIABILITY

Table 1 shows a recent compilation of the most efficient PTF modules of various sizes. The module efficiencies at relatively small sizes (10%-11% at about 1000 cm^2) are better than any other thin films. Similarly, the efficiencies at larger sizes (over 7.5% at about 7000 cm^2) are also substantially better than any other thin films. In practice, thin films will need efficiencies of about 8% to have a competitive edge in the existing market. The efficiencies of the prototypes in Table I show that an 8% near-term goal is within reach. More details are given in references [10,11].

Table I. Performance of Polycrystalline Thin Film Photovoltaic Modules

Group	Material	Area (cm^2)	Eff (%)	Power (W)
Solar Cells Inc.	CdTe	6844	7.7%	53.0
Siemens Solar	$CuInSe_2$	3883	9.7%*	37.8*
Golden Photon	CdTe	3323	6.4%*	21.3*
Siemens Solar	$CuInSe_2$	938	11.1%*	10.4*
Matsushita Battery	CdTe	1200	8.1%	9.7
BP Solar	CdTe	706	10.1%	7.1
Golden Photon	CdTe	832	8.1%*	6.8*

* NREL measurements; all aperture-area efficiency

Figure 1 shows the CdS/CdTe deposition system at SCI. SCI is a small, Toledo, Ohio, company that is about 2 years old. The success of SCI is built on their previous experience in the glass and thin film businesses (through Glasstech and Glasstech Solar) as well as the experience of their staff in CdTe (one of the PIs, Peter Meyers, came from AMETEK). Since inception, SCI has received support from the U.S. DOE/NREL program.

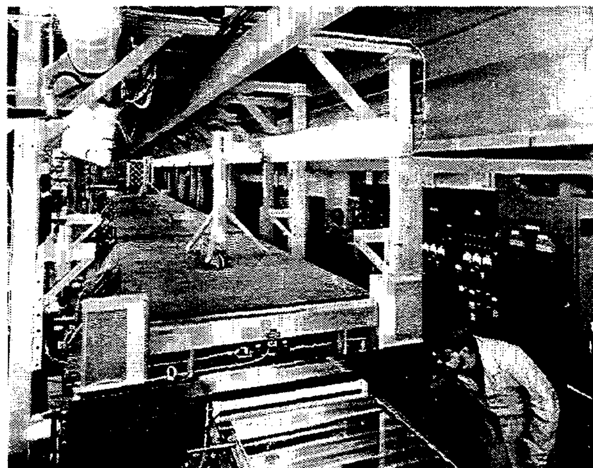

Fig. 1. The CdS/CdTe layers of the Solar Cells, Inc. module fabrication line are based on a high-rate evaporation process that produces the active semiconductor layers in about 1 minute.

The potential cost of thin-film modules depends to a large extent on the processes used to make the thin films. This is because module efficiency, process material utilization, process capital cost, and process yield are determining cost factors for thin films. All are dependent on the processes by which key layers are made. In the case of CdTe, a number of attractive processes are being used: spraying, modified close-spaced sublimation, electrodeposition, and screen printing; in the case of CIS, Siemens Solar has not revealed its processes, although it has patents in the area of sputtering and selenization. Other companies use various combinations of sputtering the metals followed by selenization in hydrogen selenide or selenium (or layer homogenization of Cu, In, Se). CdTe manufacturing appears more promising; but, in fact, experience is so limited that the lack of problems may simply be a reflection of the early stage of development.

In addition to the key absorber layer, several other semiconductor and metal layers must be deposited in order to make an excellent PV device. CdS is the preferred heterojunction partner for CIS and CdTe, although deposition conditions differ widely in the two cases. No preferred method of CdS deposition currently exists. The CdTe companies use high rate evaporation, spraying, electrodeposition, and solution growth to deposit CdS. The CIS companies use solution growth and evaporation. Because the CdS layer is a key part of thedevice in terms of performance, the issue of finding a low-cost, highly controllable process to make it requires ongoing attention.

Both CIS and CdTe devices require a transparent conductor (TC) top layer to carry off current while being transparent to light. The problem is solved differently in each case. CIS cells uses a top layer of conducting ZnO, frequently deposited by sputtering or MOCVD. The CdTe technology is usually made with a glass superstrate geometry, which means that the TC can be put down first. A major U.S. glass company, Libbey-Owens-Ford (LOF) makes tin-oxide coated float glass for thermal applications. This same low-cost, coated glass can be adapted with little change as the superstrate for CdTe devices. This allows the CdTe technology to take advantage of a ready-made, low cost supply of glass with the needed TC coating. LOF uses a form of chemical vapor deposition to deposit its tin-oxide, and the deposition is done on a "football field"-sized float glass line, achieving true economies-of-scale. The success of the LOF tin-oxide glass is an excellent indication of the potential of thin films to meet ambitious low-cost goals [12].

Various metal layers and metallic interconnects are also needed to make PV modules. In most cases, metal contacts are sputtered from flat DC magnetrons or from rotating cylindrical magnetrons. The latter can reach higher rates and use their target materials more efficiently. Figure 2 shows a rotating cylindrical magnetron depositing Mo on glass at Martin Marietta for subsequent CIS deposition (also by rotating cylindrical magnetrons). Although metals and contacts are relatively straightforward and familiar from previous thin film processing, they are a nontrivial part of the developmental process. For example, issues with the glass substrate (dirt, imperfections) and with the back contact (Mo berms, adhesion) for CIS have been cited as central to delays in introducing CIS products [13]. These "details" may yet form the focus of major developmental efforts.

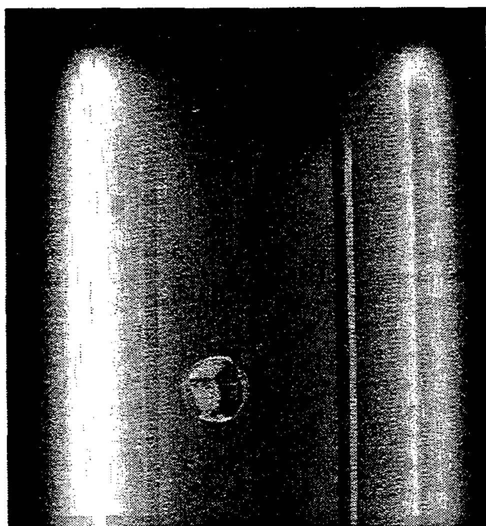

Fig. 2. Martin Marietta is developing CIS deposition based onthe use of high-rate rotating cylindrical magnetrons. Various layers (Mo, Cu, In, and others) can be deposited by this innovative process.

Finished modules require some form of interconnection among neighboring cells, and then encapsulation. Scribing is the key step in the interconnection process; and it is relatively slow and demanding. Scribing can introduce defects and areas that are vulnerable to stress (potentially causing degradation). Special concerns exist about scribing Mo prior to CIS deposition in the sense that CIS growth defects can be caused by the Mo debris [13].

Encapsulation is an area of much interest, as current schemes seem both over-engineered and too costly. In many cases, two sheets of glass are sealed together to provide the environmental isolation. Frames are usually used, although their need is debated. Future, lower-cost schemes include using plastic as one of the sealing materials. The CdTe superstrate structure could easily be adapted to this approach by using a "spray on" sealant to replace the glass at the back, if an effective sealant could be found. This is a challenge for CdTe, which has been known to be sensitive to performance losses due to water vapor.

We have had encapsulated CIS and CdTe modules outdoors at NREL for several years. In most cases, the CIS modules have been perfectly stable. Data for two sets of Siemens Solar CIS modules (earlier ones, 0.1-m^2; later ones, 0.4-m^2) are shown in Figure 3. This kind of outdoor stability is still the exception rather than the rule for new PV of any sort, and it is an important strength that sets apart the CIS technology from any other thin film. Some degradation mechanisms have been identified for specific CIS modules that have problems during manufacture. These must be identified and eliminated to assure system-level reliability.

Module Outdoor Stability

at the NREL PV Outdoor Test Facility

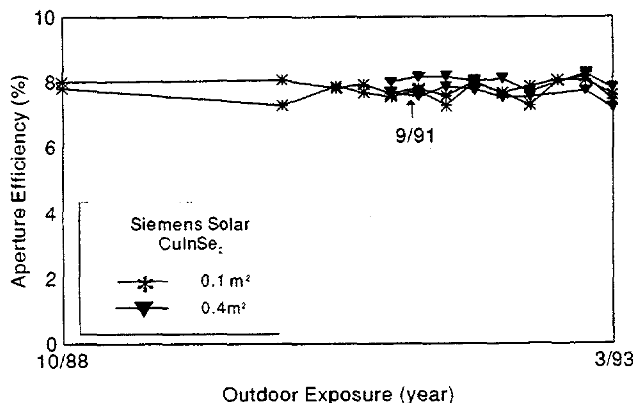

Fig. 3. NREL has been testing state-of-the-art ARCO Solar/Siemens Solar CIS modules outdoors for over four (4)years, with no sign of degradation. This is a unique result among thin films.

The CdTe technology has a mixed record in terms of reliability. We have much NREL data from stable and unstable modules, and similar data from other sources (e.g., BP Solar, Refs. [14-16]). Numerous modules appear unchanged after several years outdoors. They are a reasonable indicator that CdTe can be stable if properly

made and sealed. We also have many unstable modules. They indicate that serious issues exist. The current hypothesis is that most of the module stability problems are due to encapsulation design and poor quality control. Work must be done at both the cell and module level to isolate degradation mechanisms and eliminate them or reduce their impact.

SOLAR CELLS, NEW PROCESSES, AND TECHNOLOGY BASE

Progress during the last 2 years in CIS and CdTe cell efficiencies has been outstanding. Figure 4 shows reported, active-area efficiencies for these technologies. Summary tables on the performance of these devices have been published [2]. The recent improvement in PTF efficiencies has come from the special contributions of several universities: e.g., the EuroCIS consortium (University of Stuttgart, Royal Institute of Technology (Sweden), Swedish Institute of Microelectronics, Ecole Nationale Superieure de Paris) in CIS; and the University of South Florida in CdTe.

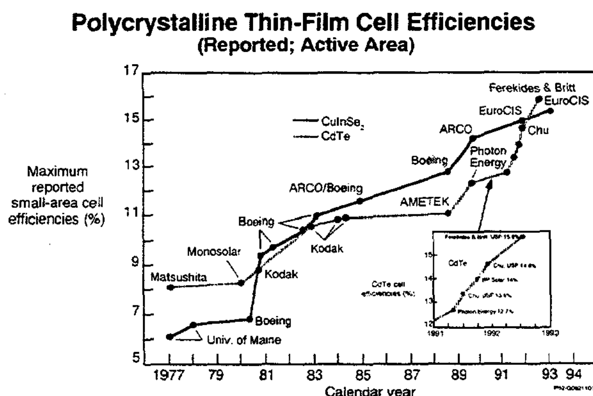

Fig. 4. The best reported active-area cell efficiencies in CIS and CdTe have now both surpassed 15% efficiency.

The EuroCIS group has found new ways to optimize CIS-based cells made by multiple-source evaporation. Besides the obvious value of their increased efficiencies (now reported to be 15.4% on an active-area basis, Ref. 17), their major contribution may have been to bring the use of alloying elements (Ga for In, S for Se) into the mainstream of CIS technology. Their work builds on previous innovative work in Ga alloying done byBoeing [18,19]. Most of the best CIS cells now being made are actually alloy cells with Ga or S. These include cells made by Boeing, EuroCIS, NREL, and Siemens Solar. International Solar Electric Technology of Inglewood, California has developed a potentially, low-cost, non-vacuum method to deposit the precursors Cu and In followed by selenization. Active-area efficiency of 11% has been obtained by this innovative process.

The NREL staff has investigated some important models of CIS formation [20-24]. The fabrication effort at NREL focuses on two issues: 1) Fabrication of device structures based on $Cu(In,Ga)Se_2$ and $CuIn(S,Se)_2$ in order to achieve efficiencies over 16%; and 2) Validation of different reaction pathways needed to make the different alloys/layers in ways that are potentially more manufacturable. Using various processes and approaches, the NREL researchers have already gained significant insight into the formation mechanisms of the thin film multinaries. Their aim is to understand the fundamental mechanisms controlling the formation of device-quality films, independent of the reaction pathways and processes. Knowledge gained from this approach is likely to aid the effort to resolve manufacturing problems associated with yield, adhesion, compositional variations, and manufacturing tolerances. It should also allow for higher cell/module efficiencies.

The use of S or Ga alloys has some important implications. Using Ga or S to replace In or Se raises the band gap of CIS-based materials. By doing so, several aspects of module manufacturing can be simplified. For example, devices with a higher band gap absorber produce lower current densities (but higher V_{oc} and FF), allowing module cells to be wider without incurring greater resistance losses. Having fewer, wider cells simplifies module scribing, reduces the number of sensitive scribe areas, and increases module active area. In addition, a higher band gap (and higher V_{oc}) reduces the sensitivity of the device to temperature losses and has a better match with the solar spectrum. All cells/modules lose efficiency with higher temperature, but the loss is inversely proportional to the voltage. Higher voltages will allow alloyed CIS devices to perform better at outdoor operating temperatures. Finally, the use of a higher band gap absorber reduces another major problem: it makes it easier to deposit a TC such as ZnO. There are several problems with the use of ZnO on conventional, low band gap CIS. Specifically, long-wavelength light is highly absorbed in conductive ZnO when that ZnO is heavily doped. This is because free electrons in the ZnO absorb long-wavelength photons. To avoid this loss mechanism, ZnO for CIS cells is currently lightly doped (fewer free electrons), but relatively thick (about 1.5 μm). This compromise requires more ZnO and longer ZnO deposition times. It also results in a wavelength-independent loss mechanism, whereby the thick ZnO absorbs a small fraction of the entire spectrum. All of these problems can be avoided with a somewhat higher band gap absorber. This is because the higher band gap absorber does not use low energy photons. Thus the ZnO can be heavily doped and made thinner without affecting the device performance (higher band gap cells make up for lost currentwith higher voltages and fill factors). The development of alloys as a mainstream part of the CIS technology is an important contribution to the technical art. Another value of alloys is that they can take pressure off the need for large quantities of In and Se. Reducing the amounts of these relatively rare materials could be of value if the technology becomes very successful (multiple GW/yr production). Despite all these advantages, it is not yet clear whether the somewhat increased complexity of using alloys in manufacturing will deter their general use.

Progress in CdTe cell efficiencies emerged from work by Ting and Shirley Chu at USF [25-28]. The Chus retired in 1992, after producing a world-record 14.6% efficient CdTe cell. They left their students Chris Ferekides and Jeff Britt to carry on their work. The transition turned out spectacularly well, with Ferekides and Britt fabricating several record CdTe cells subsequent to the Chu's retirement (see Figure 5) [29]. They made many cells over 15% efficiency (all verified at NREL) and two with 15.8% efficiency. Theirs were the first non-single-crystal thin-film cells in the world to surpass 15%. Figure 5 shows the excellent cell result of 15.8% and measured at NREL. Four cells were measured in the range of 15.7% to 15.8%. Achieving these efficiencies was an important demonstration of the potential of CdTe. Combined with the EuroCIS results, it suggests that our thoughts about the performance limits of PTF materials need to be revised upward. For instance, the possibility of 18% to 20%, single-junction thin-film cells, heretofore deemed unrealistic by mainstream PV scientists, now appears to be very possible. Thus, the attainment of ambitious cost goals, which depend on achieving very high **production module** efficiencies (over 13% and possibly over 15%), seem more plausible.

Univ. of South Florida, Glass/CdS/CdTe, Global AM1.5

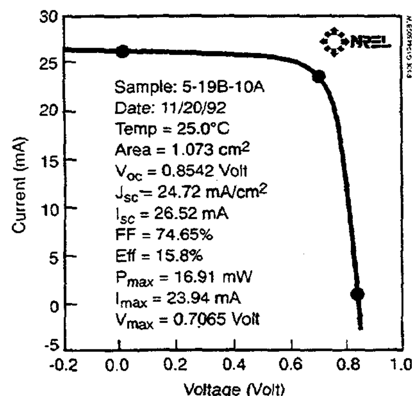

Fig. 5. The USF group of Ferekides and Britt made a number of world-record thin-film CdTe cells with efficiencies of 15.7% to 15.8%, that were verified at NREL during 1992. This is one such light I-V curve.

The USF CdTe cells address a number of technical problems: CdTe contacting, thin CdS, and possible degradation barriers.The achievement of very high fill factors (many over 72%, some as high as 75%) was done with a new contacting approach [29]. Similarly, various degradation barriers have been investigated by USF. Figure 6 shows an analysis of two USF high-efficiency cells performed at Colorado State University (CSU) by James Sites. The analysis compares various device parameters (e.g., series and shunt resistance) over a period of 3 months. In the first case, the unencapsulated cell degraded from 13.4% to 12.5%, with most of the loss in the FF. No performance loss occurred in the more recent, 15%-efficient protected cell (also note the very high FF, 75.5%). Speaking of a similar set of six high-performance cells, Sites [30] states, "we saw no change outside experimental error in the six cells we tracked this summer. Three were kept in desiccant and three in air. In contrast, the Spring 1991 record efficiency cell showed a significant increase in series resistance which was responsible for decreases in fill factor and efficiency." Progress toward stable contacts and protective layers to improve the robustness of CdTe cells are valuable USF contributions.

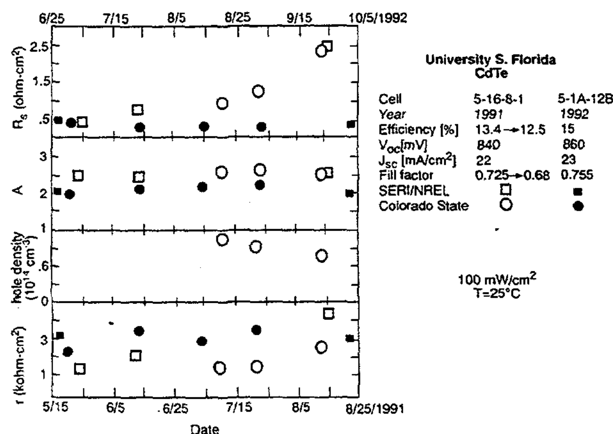

Fig. 6. CSU examined a number of unencapsulated USF CdS/CdTe cells for stability. Improvements made between 1991 and 1992 resulted in increased robustness to air exposure.

RESEARCH AND TECHNICAL ISSUES

Although we discussed some of these issues in earlier sections, we feel that the research and technical issues for CIS and CdTe warrant further discussion. However, it appears to us that none of the issues discussed below are potential barriers for enhancing the technologies for commercialization and eventual market entry.

There are some issues that are generic to the CIS technology (e.g., the addition of Ga or S to increase the band gap of CIS and have a better match with the solar spectrum; and some issues that are process dependent). For example, we know that grading the CIS absorber layer with Ga by evaporation is possible. Increases in V_{oc} have been observed (the recent NREL results, $V_{oc} = 0.687$ V, [23]) by this approach. Can similar grading be done by selenization method? In yet anotherexample, adhesion of CIS to the Mo electrode does not appear to be a problem in evaporation; however, we do see peeling of the CIS film for the selenization processes (especially those based on using hydrogen selenide), mainly due to the volume expansion and stress in the films. The addition of Te and Ga interlayers improves the adhesion of CIS to Mo. Achieving large-area stoichiometric and uniform films in manufacturing is still a formidable challenge and needs to be addressed with a great deal of attention. Also, work must be directed to replace the H_2Se gas with Se vapor source for module fabrication and to improve throughput, reproducibility and yields.

In the case of CdTe, too, there are generic as well as process-dependent issues. Although 10 processes have

yielded cell efficiency of 10% to 16%, only four techniques have been used for module fabrication - namely, electrodeposition, high-rate evaporation, spraying and screen-printing/sintering. CdTe is a self-compensating material. The role of impurities is still unknown. Thus, obtaining good, reproducible, and optimum doping of CdTe is a research issue for the various deposition techniques. Achieving stable contacts for both cells and modules receives considerable attention. Contacts such as graphite (Cu and Hg-doped), Ni/Al, and Cu/Ni have demonstrated fairly robust performance. Chemical and heat treatments have resulted in type conversion, junction formation and enhanced grain growth (especially for CdTe grown at low temperatures, e.g., by electrodeposition). Although large-area modules with reported power output of 53 Watt have been demonstrated, high throughput, yield, and reproducibility need to be demonstrated. Two schemes have been used to encapsulate the modules. Those with a graphite contact normally require a spacer between the two pieces of glass, while the ones with the metal contacts use EVA/glass encapsulation. Safe handling of Cd has been demonstrated at several facilities, that are currently developing CdTe modules using the latest OSHA regulations. Recycling of broken and spent modules are discussed in the following section.

ES&H AND RECYCLING

A number of environment, safety, and health issues exist for the manufacturing and commercial use of CIS and CdTe. In most cases, these concerns are similar to those for other PV. In all cases where CdTe or CdS are present, the presence of Cd complicates the situation.

Some of the main concerns are

- Possible uses of toxic gases;
- Manufacturing safety issues, especially those related to Cd or other health threats;
- The existence/disposal/recycling of waste modules at various stages during production;
- The presence/disposal/recycling of unused materials (CdS, CdTe, Cu, In, Se, CIS, contact metals, etc.) during various process steps;
- Cleaners and solvents;
- Transportation/regulations concerning various feedstocks and recycling products;
- A number of product-level issues, including
  - Product distribution/transportation;
  - Broken/returned product;
  - Eventual product disposal/recycling;
  - Product safety (e.g., fires, breakage).

Most of these issues closely parallel those for other forms of PV. Moskowitz and coworkers have written extensively on the general subject of PV-related manufacturing issues and on Cd-issues [34-39]. Others have written illuminating comparisons between PV and conventional energy sources [40, 41].

An important criteria for waste classification is the U.S. Environmental Protection Agency's (EPA's) EP Toxicity test. The test is carried out by grinding a module to particle size and then suspending the particles in solution. Various materials (including Se, Ag, Pb, and Cd) are then measured against a standard. This test has been conducted on a very limited sample of CIS and CdTe modules. It is important to realize that the results are not necessarily characteristic of future commercial modules. Similarly, it is not clear whether other PV (specifically Si modules with Pb or Ag in them) could pass the test. In the early PTF tests, the CIS modules passed by a wide margin for both Se and Cd (despite the presence of CdS, which, however, is very thin - about 300 Å). The CdS/CdTe modules failed by a small margin to pass for Cd. In fact, the margin was so narrow that future modules (wherein small metallic Cd and CdO inclusions could be excluded) may pass the test. However, because the CdTe manufacturers already assume the need for recycling and for other similar strategies, passing the EP Toxicity test is not essential.

Moskowitz and coworkers have recently begun collaborations with the National Institute of Environmental Health Sciences (NIEHS) to investigate the oral toxicity of CIS and CdTe. Early results show a surprising tolerance for large oral doses of CIS materials (no toxic effects observed for any of the tested doses and no organ abnormalities) and an expected sensitivity to Cd in CdTe and CdS. The latter caused toxic effects (as expected) but appeared to be less soluble in biological systems than other cadmium compounds [42].

Besides clear-cut health issues, the presence of Cd in CdS and CdTe poses some unique and less-quantifiable concerns:

o Public reaction to CdTe manufacturing and product use;
o International regulatory climate and barriers.

These factors have played a visible role in the progress of the PTF technologies - especially the CdTe technology - and may yet play a significant role in their future. Various reports have been written on Cd-related issues [3,34-39,43,44]. In most cases, the authors view Cd-related issues as within the normal range expected for any large-scale commercial PV technology.

An important reason for this is that the small amount of Cd in thin-film modules (about 5 gms/m^2) limits potential impacts. For example, during 1 year of output, a 1-m^2 CdTe module (10% efficient, average U.S. sunlight) would produce about 200 kWh of electricity. Put in terms of output per gram of Cd, themodule would produce 40 kWh/gm of Cd during that same annual period. For comparison, the total annual amount of U.S. electricity is about 2.5×10^{12} kWh. To generate (using CdTe PV) an amount of electricity equal to the U.S. total would require deploying 12,500 km^2 of modules with about 60,000 metric tons (MT) of Cd in them. In practice, it would take many years to deploy such a large amount of PV. If one assumed a 30 year period for deployment (probably unrealistically quick), about 2000-3000 MT/yr of Cd would be needed (depending on losses during production). The world's use of Cd today for existing purposes is over 15,000 MT annual [45]. Thus, transforming the U.S. energy infrastructure (a huge undertaking) would not significantly change the global annual use of Cd. For another similar order-of-magnitude example, consider that today the U.S. throws away about 2000 MT/yr of Cd from

Ni/Cd batteries. Not only would CdTe PV not be thrown away (it would last 30 years and then be recycled), but its use would have much greater impact (a transformed world energy infrastructure versus the use of home electronics) that the comparison suggests the use of Cd in PV is, environmentally, totally different from any other current use of that material; and it can be sequestered for extended period of time (30 years).

Processes already exist for recapturing and recycling Cd-containing materials [38]. For example, most of the Ni/Cd batteries used in industry are recycled. (Batteries in toys and other consumer items are not often recycled, and they are the source of the Cd entering the waste stream.) Because the volume of the industrial Ni/Cd batteries is very large compared to the volume of Cd in CdTe PV, they form a substantial proof-of-concept for Cd recycling. For those working in the CdTe technology, continued efforts toward reduced process wastes, thinner layers, recycling, and biomonitoring are essential. For those in CIS, another path is possible. To minimize Cd concerns, some CIS groups have worked to replace CdS with other heterojunction partners. This work has been relatively successful, indicating that CdS can be replaced and high efficiency cells can still be fabricated. However, alternates to CdS are not yet integrated into any CIS commercialization effort.

LONG-RANGE GOALS AND COSTS

The long-term cost goals of PTF modules are in the range of $\$50/m^2$ [8,46]. At power outputs of 10% and 15% (100 W_p/m^2 and 150 W_p/m^2, respectively), this would mean that module costs would be about \$0.5 and $\$0.33/W_p$, respectively . (The \$/W costs are simply recalculations of these costs ($\$/m^2$ / W_p/m^2 yields $\$/W_p$).) Combined with systems costs that reflect larger volume production for larger markets, the cost of installed PV could fall to under $\$1/W_p$, implying costs of about 6 ¢/kWh for PV generated electricity [8].

Are these cost goals possible? When the product-level technology (which includes all the process development needed for manufacture) has adopted all the technical capabilities now observed in laboratory experiments, the commercial modulesshould be about 80% of the efficiency of the best cells. Today's best cells are about 16% efficient, so this implies modules of about 13% efficiency with today's technology. In terms of module production costs, various studies [47-54] of materials costs, combined with energy inputs, labor, and capital costs support very ambitious cost projections. All of the cited cost studies agree that ultimate manufacturing costs can be as low as $\$40$-$\$50/m^2$. The studies include those on specific PTF technologies provided by U.S. manufacturers to the U.S. DOE/NREL PV Manufacturing Initiative as part of their final reports [51-54]. These provide the most up-to-date information on module cost projections. Because the modules are the major cost-driver for systems (in terms of cost and output per unit cost) the progress in module technology is the essential factor behind the cost projections for systems.

But the road to low-cost PV remains a long one. Numerous challenges remain, not the least of which is the high cost of today's PV (Figure 7). Even the success of this generation of new PV technologies, such as the PTF

PV System Costs

\$/Wp versus cents/kWh

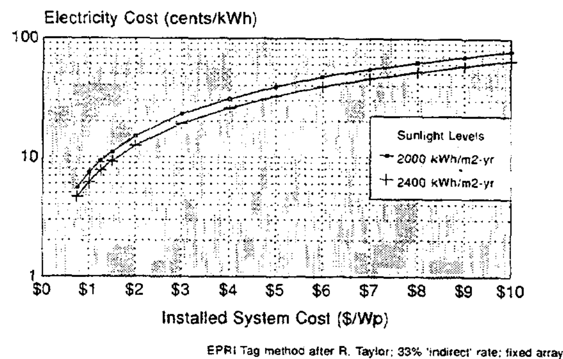

Fig. 7. Utility systems installed at various costs (in $\$/W_p$) imply various electricity prices for the consumer (depending also on local sunlight). Note that today's installed systems, at about $\$8/W_p$ imply electricity at 50-60 ¢/kWh for utility systems [based on analysis from Refs. 8,46]. Today's high cost of PV is the driving force behind developing new technologies such as those based on PTFs.

technologies reviewed in this article, does not by itself assure the global impact of PV, because the price of PV will still remain much higher than conventional alternatives until major technological improvements have time to reach commercial products. Technology development work in PTF will still be needed to:

1. Make modules in production that are as efficient as today's best cells (up to 15%);
2. Replace many of today's chosen processes with those that are less expensive in terms of material use and capital costs;
3. Invent novel module designs that improve costs through reduced complexity and improved ease of manufacture;
4. Optimize manufacturing lines, given optimal processes and module designs;
5. Fully implement recycling strategies at all stages of the product lifecycle;
6. Accelerate cost-reductions in Balance-of-System (BOS) components to meet the costs needed to make total system costs equivalently low.

If most of these issues can be well addressed, PTF-based PV modules would drop below $0.50/W (module efficiencies of 13% and costs of $50/m^2 imply module costs of $50/130 W, or about 40 ¢/W). If systems costs come down in a similar way due to improved designs and economies-of-volume production, installed system costs of about $1-$1.5/W would be possible. Figure 7 then implies that electricity costs would be about 6-10 ¢/kWh, depending on local sunlight.

The goal of truly low cost PV assumes that there are major markets that will allow PV to evolve toward larger and larger production volumes (to achieve economies-of-scale) despite PV's relatively high cost. These markets include very large, rural markets in developing countries, peak shaving in sunny/humid developed locations, and finally general use of PV to reduce reliance on nonrenewable resources (e.g., for intermediate, daytime electricity). The PTF PV technologies should be able to reach the earliest large market (developing countries) once first-generation scale-up has been fully achieved. At that time, module prices should be near $2/W, and BOS may be in that price range as well. Installed system costs should then be about $4/W, and electricity costs would be near 20-30 ¢/kWh (see Figure 7, which does not take into account any environmental credits).

Entry of PV into the large, developing country market could be politically supported, because the use of PV has strong, positive social and economic implications in these countries. By improving farm and nonfarm productivity, PV systems for rural use would slow the flight of rural poor to the cities. It would have the kind of social impact that many planners at the U.N. and elsewhere are seeking in terms of reducing world tensions while improving food supply and lifestyles. One can easily imagine a world in which PV fills this role. As such, PV development could become self-sustaining. Given the kind of progress seen in technologies like CdTe (despite shoestring funding, on a scale relative to their possible impacts), one could then be confident that PV would achieve its potential and become the next major revolutionary element in energy production.

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