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ABSTRACT

Total-area conversion efficiency of 15%-15.8% have been achieved for thin-film CdTe and CIS solar cells. Modules with power output of 5-53 W have been demonstrated by several groups world-wide. Critical processes and reaction pathways for achieving excellent PV devices have been elucidated. Research, development and technical issues have been identified, which could result in potential improvements in device and module performance. A 1-kW thin-film CdTe array has been installed and is being tested. Multimegawatt thin-film CdTe manufacturing plants are expected to be completed in 1-2 years.

INTRODUCTION

In this paper, we report on the progress made in thin-film cadmium telluride (CdTe), and copper indium diselenide ($CuInSe_2$, CIS) photovoltaic (PV) technologies during the past year. Recently, we have highlighted the perspectives and opportunities in polycrystalline thin films; namely, CdTe and CIS (1). Dramatic increases have occurred in both thin-film CdTe and CIS solar cells. Total-area cell efficiencies in the range of 15.5% to 15.8% have been achieved in both these emerging and promising thin-film technologies. Several critical processes and reaction pathways have been identified to achieve high quality films, that also result in excellent thin-film PV devices. At the module level, new groups have made contributions in advancing the state of the art, e.g., Solar Cells, Inc., (SCI) of Toledo, Ohio and Golden Photon, Inc., (GPI) of Golden, Colorado. Other groups such as Energy Photovoltaics, Martin Marietta, and Solarex are at various stages of development of thin-film CIS modules. International Solar Electric Technology (ISET) of Inglewood, California, has successfully fabricated its first 900-cm^2 (1-ft^2) CIS modules. As reported earlier, Siemens Solar Industries (SSI) of Camarillo, California, has fabricated thin-film CIS modules with the highest power output of 37.8 W (2).

Stability data performed on CIS modules for several years are very encouraging. A 1-kW CdTe PV system has been installed by SCI in Toledo, Ohio. A similar 1-kW CIS system is currently being installed at NREL's outdoor test facilities using SSI modules. Multimegawatt manufacturing plants have been announced by GPI and SCI, that are expected to be completed in 1–2 years.

MATERIALS AND PROCESSES

Although over the years, several polycrystalline thin-film materials such as CdTe, CIS, CuO, Cu_2S, and Zn_3P_2 have been investigated for PV performance, only two (CdTe, CIS) have emerged as strong potential candidates for low-cost, widespread use in PV applications. The success of these materials may be attributed to the numerous choices available for the deposition of these thin films. Tables I and II summarize the deposition methods used to grow thin-film CdTe and CIS, respectively. At least 15 deposition processes have been used to grow thin-film CdTe, and most of these have been used to fabricate devices with efficiency over 10%. The processes resulting in high quality CdTe films and devices are atomic layer epitaxy (3), close-spaced sublimation (4), electrodeposition (5), evaporation (6), laser ablation (7), metal organic chemical vapor deposition (8), molecular beam epitaxy (8), screen printing/sintering (9), sputtering (7), and spray (10).

Table I

Growth of Thin Film CdTe

- Atomic Layer Epitaxy
- Electrodeposition
- Spray
- Close Spaced Sublimation
- Screen Printing
- Chemical Vapor Deposition
- Hot Wall Evaporation
- Ion-Assisted Evaporation
- Photo-Assisted Evaporation
- Laser Ablation
- Thermal Evaporation
- Sputtering
- Sputtering/Laser-Assisted Annealing
- Molecular Beam Epitaxy
- Metal Organic Chemical Vapor Deposition

Table II

Growth of Thin Film $CuInSe_2$

- Coevaporation
- Electrodeposition/ Selenization
- Electron Beam/ Selenization
- Hybrid Selenization
- Sputtering/Selenization
- Hybrid Evaporation/Sputtering
- Reactive Sputtering
- Spraying
- Sputtering/Laser-Assisted Annealing
- Sputtering/Rapid Isothermal Processing
- Close Spaced Vapor Transport

In the case of CIS, several processes have been used for the growth of thin-films. But only 3 processes have yielded device efficiency over 10%. They are evaporation (11,12) and modifications thereof, sputtering/selenization (13), and rapid isothermal processing (14). More recently, NREL researchers have done extensive work to elucidate the various reaction pathways for obtaining device-quality thin-film CIS. This is summarized in Table III. Fabrication techniques and growth models have been reported elsewhere (15,16). The addition of Ga and/or S to CIS (0.95 eV) has been the key to achieving high quality CIS, and higher band gaps are obtained depending upon the Ga or S content of the films (17).

Table III

Reaction Pathways for CIGS Films

I. Cu + (In,Ga) + Se - CIGS — Device Quality

II. Cu + (In,Ga) + Se — CIGS + Cu_xSe_y - Cu-rich
CIGS + Cu_xSe_y + (In + Ga) + Se — CIGS - Device Quality

III. (i) Cu + Se — Cu_xSe_y
Cu_xSe_y + (In, Ga) + Se — CIGS - Device Quality

(ii) (In,Ga) + Se — (In, Ga) + Se_y
$(In,Ga)Se_y$ + Cu + Se — CIGS - Device Quality

IV. Cu_xSe_y + $(In,Ga)Se_y$ — CIGS - Device Quality

V. Cu + (In,Ga) — Cu(In,Ga) - Intermetallics
Cu(In,Ga) + Se — CIGS - Device Quality

DEVICES AND MODULES

Major technical advances have occurred in improving the total-area solar cell efficiency of thin-film CdTe devices to 15.8%. These devices were fabricated by Chris Ferekides and Jeff Britt at the University of South Florida (USF) using the close-spaced sublimation technique (18,19). Several devices in the range of 15% to 15.8% have been obtained by the USF group. The solar cell structure in its superstrate configuration consists of a 7059 boro-silicate tin-oxide coated glass on which is deposited a thin layer of solution-grown CdS. The thin CdS layer helps improve the blue response of the devices by achieving higher currents (2). Currents up to 26 mA/cm^2 have been achieved with this structure by GPI. Device- quality thin-film CdTe, which is the main absorber layer of the solar cell is deposited by several methods (Table I). This is followed by the $CdCl_2$ treatment (20) and a heat treatment at 400°–425°C for 15–20 min. This results in type conversion and grain growth of the thin-film CdTe (21,22). The back contact used to complete the device fabrication is either graphite (Cu or Hg doped) or metals (Cu/Ni, Ni/A1, Ni). Au contacts are highly unstable, and are not recommended in a device structure. Current research is focused on optimizing high efficiency devices on low-cost sodalime glass (23), which is the main superstrate used by industry to make modules.

Thin-film CIS devices are generally fabricated in the substrate configuration. One micron of Mo is deposited on low-cost sodalime glass by e-beam evaporation or sputtering. This is followed by the CIS absorber layer and the thin-film CdS by solution growth as the heterojunction partner. Finally, ZnO, which is the transparent conductor (TC), is deposited by sputtering or MOCVD. The highest total-area conversion efficiency of 15.5% has been obtained recently by NREL using a hybrid selenization process with CIGS. The Ga/In ratio is about 25:75. The highest voltage of 687 mV, also achieved by NREL (16), has a so-called back surface field (BSF), which is believed to serve as a minority-carrier mirror for efficient carrier collection in the rear of the device.

For large-area modules the performance data is summarized in Table IV. In the case of large-area, thin-film CdTe modules, four groups world-wide are actively developing module fabrication with sizes varying from 1200–7200 cm^2 (1–8 ft^2), using various deposition techniques for the absorber layers. In the United States, GPI uses a spray technique (10), while SCI uses a modified close-spaced sublimation method (24,25). The best reported power output of GPI is about 26 W (3600 cm^2), and that by SCI is 53 W (7200-cm^2). Both companies have announced plans to construct large multimegawatt manufacturing plants in the United States. These plants are expected to be on line in about 1–2 years. In England, BP Solar is actively developing the manufacture of thin-film CdTe modules by electrodeposition. Although 7-W (900-cm^2, 1-ft^2) have been reported so far (5), much larger modules (5400-cm^2, 6-ft^2) are in the developmental stages at BP Solar. Matsushita Battery of Japan uses the screen printing/sintering method to fabricate its thin-film CdTe modules. To date, 10-W (1200-cm^2) modules have been fabricated by Matsushita Battery (9).

Table IV

Performance of Polycrystalline Thin Film Photovoltaic Modules

Group	Material	Area (cm^2)	Eff (%)	Power (W)
Solar Cells Inc.	CdTe	6844	7.7	53.0
Siemens Solar	$CuInSe_2$	3883	9.7*	37.8*
Golden Photon	CdTe	3323	6.4*	21.3*
Siemens Solar	$CuInSe_2$	938	11.1*	10.4*
Matsushita Battery	CdTe	1200	8.7	10.0
BP Solar	CdTe	706	10.1	7.1
Golden Photon	CdTe	832	8.1*	6.8*
ISET	$CuInSe_2$	846	5.7*	4.8*

*NREL [illegible] efficiency

Thin-film CIS modules have been fabricated by SSI and ISET in the United States so far. SSI fabricated large-area, thin-film CIS modules of ~0.4 m^2 (~4 ft^2). The best achieved have a power output of 37.8 W, while a smaller module of ~0.1 m^2 had an output of 10.4 W. Simplified and improved processing of CIS is now being pursued by SSI (26). ISET's thin-film CIS modules, which are in the early stages of development, have power outputs as high as 4.8 W (13). Other groups such as Energy Photovoltaics, Martin Marietta, and Solarex are also in the process of fabricating 900-cm^2 (1-ft^2) thin-film CIS modules. No company as yet announced a manufacturing facility for CIS modules. CIS modules have been tested outdoors at NREL for more than 4 years. Within experimental error, the SSI modules varying in size from 0.1–0.4 m^2 do not show any changes in performance. This is one of the key strengths for the emerging thin-film CIS technology.

RESEARCH, DEVELOPMENT, AND TECHNICAL ISSUES

Thin-film CdTe is a self-compensating material with an optimum band gap of 1.45 eV, which is ideally suited to match the solar spectrum.. A list of the issues for thin-film CdTe technology is compiled in Table V. Issues such as doping continue to be a research problem. Although p-type films with resistivity of 200–300 Ω-cm have been achieved by doping it with Sb (27), the doping process is not consistent and reproducible. The role of impurities is also not known. Thin-film CdTe solar cells with efficiencies of 10% to 16% have been achieved with 10 deposition methods (28). Most of the devices use either graphite (Cu or Hg doped), Cu/Ni, or Ni/Al contacts. Fairly robust performances have been demonstrated by these devices. To prevent the ingress of moisture, thin-film

Table V

Technical Issues
CdTe Technology

Topic	Issue
• Doping	• Can conductivity be enhanced?
• Contacts	• Can contacts be improved and stablized; or alternate structures be developed
• Interface	• Is there an alloy formation at the CdS/CdTe interface?
• Heat Treatments	• What are the effects of the critical chemical and heat treatments?
• Module Design	• Can large-area module be as efficient as small cells?
• Encapsulation	• Are edge sealants required for stable modules?; can the effect of moisture ingress be elimnated?
• Cd Usage	• Can Cd be used safety in the work place?; can modules be recycled at end of useful life?

Table VI

Technical Issue
CIS Technology

Topic	Issues
• Adhesion	• Can the Mo/CIS adhesion be improved?
• Contacts	• Can alternate contacts be developed to replace Mo?
• Se Vapors	• Can a less hazardous Se vapor source replace H_2Se gas?
• Structure	• Can superstrate structures be developed?
• Stoichiometry	• Can large-area stoichiometric CIS films be achieved?
• Wet Process	• Can wet process be eliminated?
• Mfg Process	• Can we develop a process which gives compositional uniformity and high yields?

CdTe modules requires focus on excellent encapsulation and edge sealants. Two schemes have been used to encapsulate the modules. The ones with the metal contact normally have an EVA/glass encapsulation, while the ones with the graphite contacts have a space between the two pieces of glass. Safe handling of Cd (29) has been demonstrated in several facilities developing thin-film CdTe modules using the latest OSHA rules. In separate papers and reports, we have addressed the issue of recycling of broken and spent modules (1,30,31).

Table VI summarizes the issues in the case of thin-film CIS technology. Peeling of the CIS films grown by selenization is still a formidable challenge. Improvements have been made by the addition of Ga (32) or Te (33) at the CIS/Mo interface. Simplied interconnect schemes need to be developed to eliminate problems arising from berms created during laser scribing of the Mo contact. Also, trying to achieve spatial uniformity and stoichiometric films over large areas needs to be demonstrated. Alternate techniques to modify or replace the existing selenization process for module fabrication should be investigated to improve reproducibility, throughput, and yields. NREL researchers have developed a hybrid method of fabricating efficient thin-film CIGS solar cells, that provides new and improved avenues for reproducible device fabrication. These possibilities are being explored with the United States CIS companies.

PV SYSTEMS AND TESTING

SCI has recently installed a nominal 1-kW thin-film CdTe array (Figure 1) at its outdoor test facilities in Toledo, Ohio (24). Twenty-four modules have been used in this installation. The modules have a glass/EVA/glass encapsulation with Al frames. Data are currently being collected and will be reported in several months. Another nominal 1-kW thin-film CIS array will be installed at NREL's outdoor test facilities using SSI modules. This array will be ready for operation in 1–2 months. Thirty-six modules will be used for this array configuration. Typical module output is about 30 W. Glass/EVA/glass has also been used for encapsulation for these thin-film CIS modules, with reinforced injection mold (RIM) frame. Once the system is installed and operational, data will be collected and reported subsequently.

SUMMARY

Thin-film CdTe and CIS-based solar cells have demonstrated remarkably high total-area conversion efficiency of 15.5% to 15.8%, that was independently verified by NREL. Numerous deposition techniques and new and improved reaction pathways have been identified for fabricating high quality devices. Six groups world-wide have made

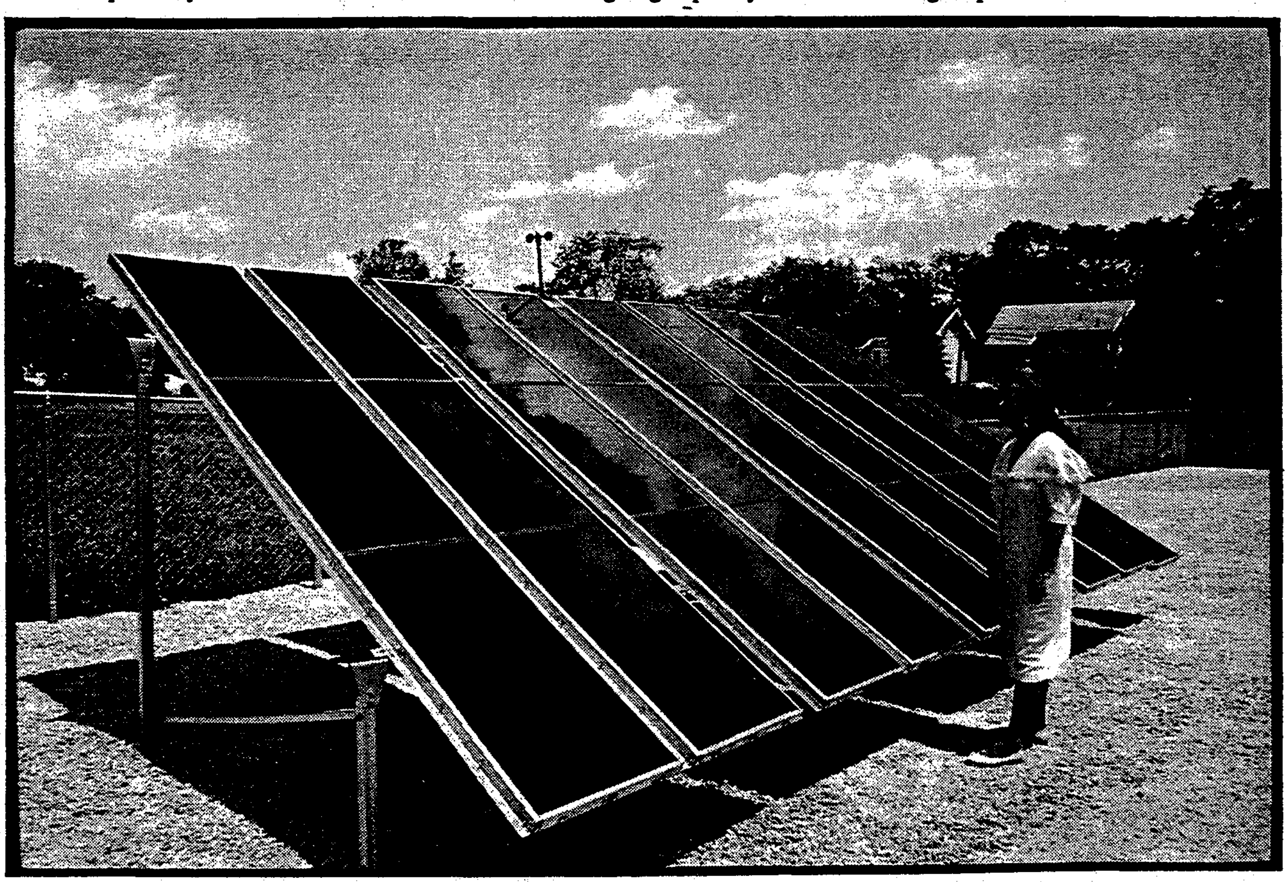

Figure 1. A 1-kW thin-film CdTe array installed at Solar Cells, Inc. in Toledo, Ohio

prototype polycrystalline thin-film modules with sizes from 900–7200 cm^2 (1–8 ft^2), with power output varying from about 5–53 W. Several research, development, and technical issues have been identified and further research should result in improved device and module performance, lower cost, and ease of manufacture. A 1-kW thin-film CdTe array has been installed and is being tested, while a 1 kW thin-film CIS array will be installed at NREL in the next two months. Multimegawatt manufacturing facilities are currently being installed in the United States by GPI and SCI, and should be producing low-cost, thin-film CdTe modules in 1-2 years.

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