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Research on Polycrystalline Thin-Film Submodules Based on $CuInSe_2$ Materials

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EXECUTIVE SUMMARY

Objectives: The principal objective of the three year cost-shared research program at Solarex is to develop all pertinent processes and technologies required to achieve the goal of 12% CIS sub-module (with areas >900 cm^2). We have focused our effects on four tasks: (I) Window Layers, Contacts, Substrate, (II) CIS Absorber Layer, (III) Device Structure and (IV) Submodule Design and Encapsulation. In each task we have concurrently addressed (a) basic material improvements, (b) fabrication and characterization of CIS solar cells and (C) scale-up of processes to large area substrates.

Task I: Windows Layers, Contacts, Substrate

The window layers consists of two thin layers, CdS and ZnO. The CdS layer is deposited by chemical solution growth and the ZnO layer is deposited by either low pressure chemical vapor deposition (LPCVD) or by sputtering from an Al-doped ZnO target.

The thickness of the CdS layer affects the transmission between 400-500 nm and has been optimized. Short-circuit current densities above 40 mA/cm^2 have been achieved with < 400 A thick CdS layer. The CdS process has been scaled-up to 12" x 13" substrates. The long wavelength transmission of LPCVD deposited ZnO layer is found to be a strong function of diborane dopant concentration. Reduction of diborane dopant gas in ZnO deposition resulted in an increase in short-circuit current density from 35.8 mA/cm_2 to 39.1 mA/cm_2, mostly due to reduction in long wavelength losses. This process has been scaled-up to 6" x 6" substrates. Sputtered ZnO films have been scaled-up to 12" x 13" substrates. These films have sheet resistance of about 13 ohms/sg. but have higher absorption losses than LPCVD deposited ZnO films of similar thickness.

Tasks II: CIS Absorber Layer

We have developed a novel process called Elemental Deposition and Compound Formation (EDCF) to prepare CIS thin films. The process constitutes of deposition of Cu, In and Se layers at room temperature followed by heat-treatment in an inert atmosphere. CIS films have been prepared which have proper stoichiometry and p-type conductivity. The process has been scaled-up to 8" x 8" substrates and the spatial compositional uniformity has been mapped-out. Scale-up from 1 cm^2 to > 50 cm^2 shows excellent uniformity whereas further scale-up to > 400 cm^2 shows

some variation in film composition. We attribute the variation on 8" x 8" substrate (> 400 cm^2) to variations in uniformity of temperature during the compound formation step. Auger depth profile of these films indicate compositional uniformity in thickness. X-ray analysis shows strong (112) peak intensity and lacks any extraneous peaks indicating highly oriented chalcopyrite grains devoid of Cu_xSe and 1:2:3.5 phases.

Task III: Device Structure

Solar cells have been fabricated on EDCF prepared CIS films with the following device structure:

Light = > metal grid/ZnO/CdS/CIS/Mo/glass

The best solar cell had an active area conversion efficiency of 10.2% with the following parameters:

V_{oc} = 0.427V, J_{sc} = 37.41 mA/cm^2 and F.F. = 0.641

Task IV: Submodule Design and Encapsulation

The CIS submodule interconnect scheme has been developed. We have developed laser scribing of the Mo film and mechanical scribes for the CIS scribe and the ZnO scribe. Laser scribing of glass/Mo substrates yields poor results due to extensive cracking, flaking and burning along the scribe edges. An interlayer of specular tin oxide between glass and Mo improves the laser scribing. The interaction of the laser beam and the glass/tin oxide/Mo composite is more favorable in terms of optical, mechanical and thermal aspects resulting in a clean ablation. The process has been scaled-up to 12" x 13". All three scribes have been demonstrated on 8" x 8" substrate. Small area submodules (area ~25 cm^2) with active area efficiency of 7.3% have been fabricated on CIS material deposited at the Institute of Energy Conversion with all other layers and all scribing done at Solarex.

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1.0 INTRODUCTION

Thin-film $CuInSe_2$ (CIS) is an attractive material for low-cost photovoltaic applications. The highest reported conversion efficiency of CIS devices has now reached 15.2% [1]. Many approaches are being pursued to develop this material with several organizations reporting efficiencies > 12% All the high performance CIS solar cell results have been reported on CIS material prepared either by co-evaporation of Cu, In and Se onto heated substrates with temperatures between 400-500 C [2] or by selenization of Cu and In films by H_2Se gas [3]. The first approach is difficult to scale-up in large areas and the second approach used toxic H_2Se gas for the selenization of metal layers to form CIS.

At Solarex we have been developing processes which is compatible with large area deposition and also avoids the uses of toxic gas. We have explored three processes for the deposition/information of CIS material: (i) Three Source Co-sputtering of Cu, In and Se, (ii) Hybrid Process of Metal Sputtering and Se Evaporation and (iii) Elemental Deposition and Compound Formation (EDCF).

Most of our effects have been concentrated on development of EDCF process for CIS deposition. This process entails preparation of CIS material in two steps. The first step is the deposition of Cu, In and Se either by sputtering or by sputtering/evaporation at room temperature. The second step is to subject the elemental stack to a proper heat-treatment in an inert gas [4,5].

Large area, high efficiency modules based on this absorber material also require the scale-up of window and contact layers and formation of viable segment interconnects. We have scaled-up CdS deposition by chemical deposition method, developed ZnO by low pressure chemical vapor deposition (LPCVD) and by sputtering from a ZnO target, improved the adhesion of Mo to glass and Mo, developed laser scribing for Mo and mechanical scribing for CIS and ZnO to form viable interconnects.

In this report we summarize the efforts made in scale-up of window layers, CIS material properties, device performance, elements of CIS module fabrication and the design and fabrication of a large area CIS machine.

2.0 TASK I: WINDOW LAYERS, SUBSTRATES AND CONTRACTS

2.1 Window Layers

The CIS window layer is composed of two materials, cadmium sulfide and zinc oxide. Together they form the junction to the CIS and allow for efficient current collection while acting as the transparent-front contact. The goal of the window layer research has been two-fold. First, the optimization of the window layers to get the maximum performance from the CIS device and second, to develop a cost effective method for depositing the films on large area modules.

2.1.1 Cadmium Sulfide

2.1.1.1 *Process*

The cadmium sulfide (CdS) films are deposited by the solution growth technique (6). In this process, a cadmium salt is reacted with sulfide ion in an aqueous solution, where they combine to form the CdS film. The feedstock material are typically: cadmium chloride, ammonium chloride, ammonium hydroxide and thiourea. The chemical concentrations have been optimized so that the cadmium and sulfide ions are slowly generated in the solution allowing for greater control of the film growth. This also prevents the spontaneous precipitation of CdS. Since the process proceeds by an ion-by-ion deposition mechanism, the CdS film is stoichiometric and is highly resistive, greater than 10^8 (ohm-cm). This mechanism also makes it very difficult to dope the films in situ.

2.1.1.2 *Optical Characteristics*

Because of the stoichiometry, the optical characteristics are dominated by the film thickness. As the film thickness is increased, the short wavelength transmission decreases. The increase in thickness does not affect the sub-band gap transmission. **Figure 2-1** compares transmission spectra of different CdS film thickness. The effect of this absorption is seen in the Q.E. of the completed CIS device. **Figure 2-2** shows the Q.E. of three CIS samples, processed identically except for the CdS thickness. The CdS thickness include <400A, 500A and 1000A. There is a corresponding decrease in J_{sc} with an increase in CdS film thickness, all due to the short wavelength absorption of the CdS film.

CdS TRANSMISSION AS A FUNCTION OF FILM THICKNESS

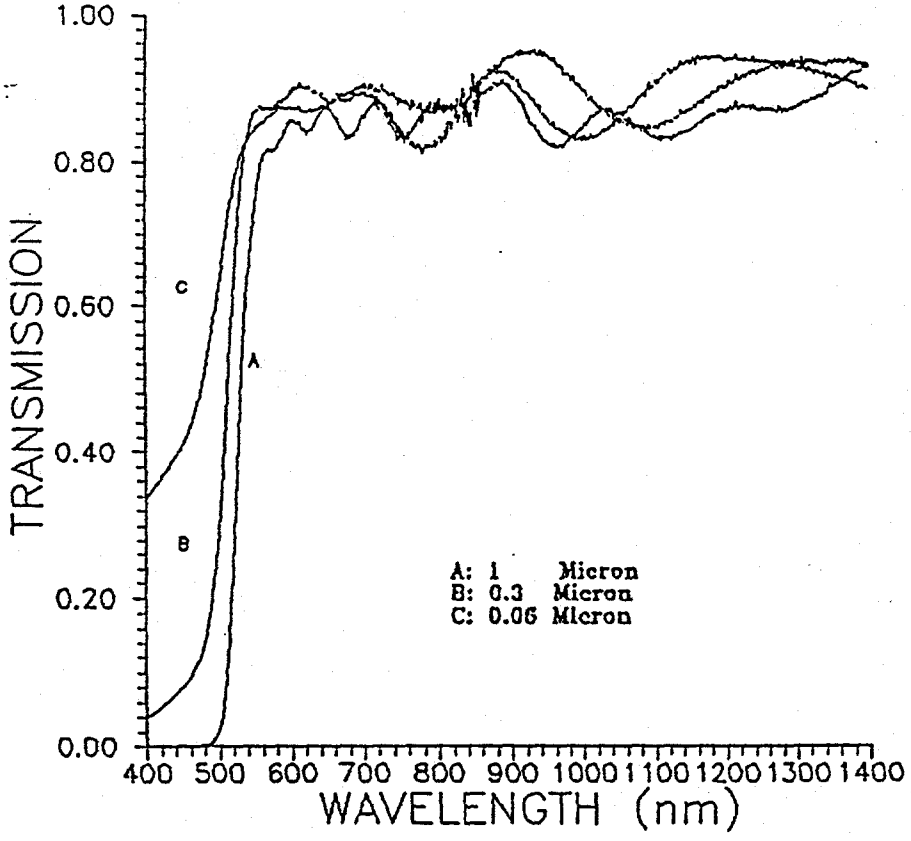

Figure 2-1

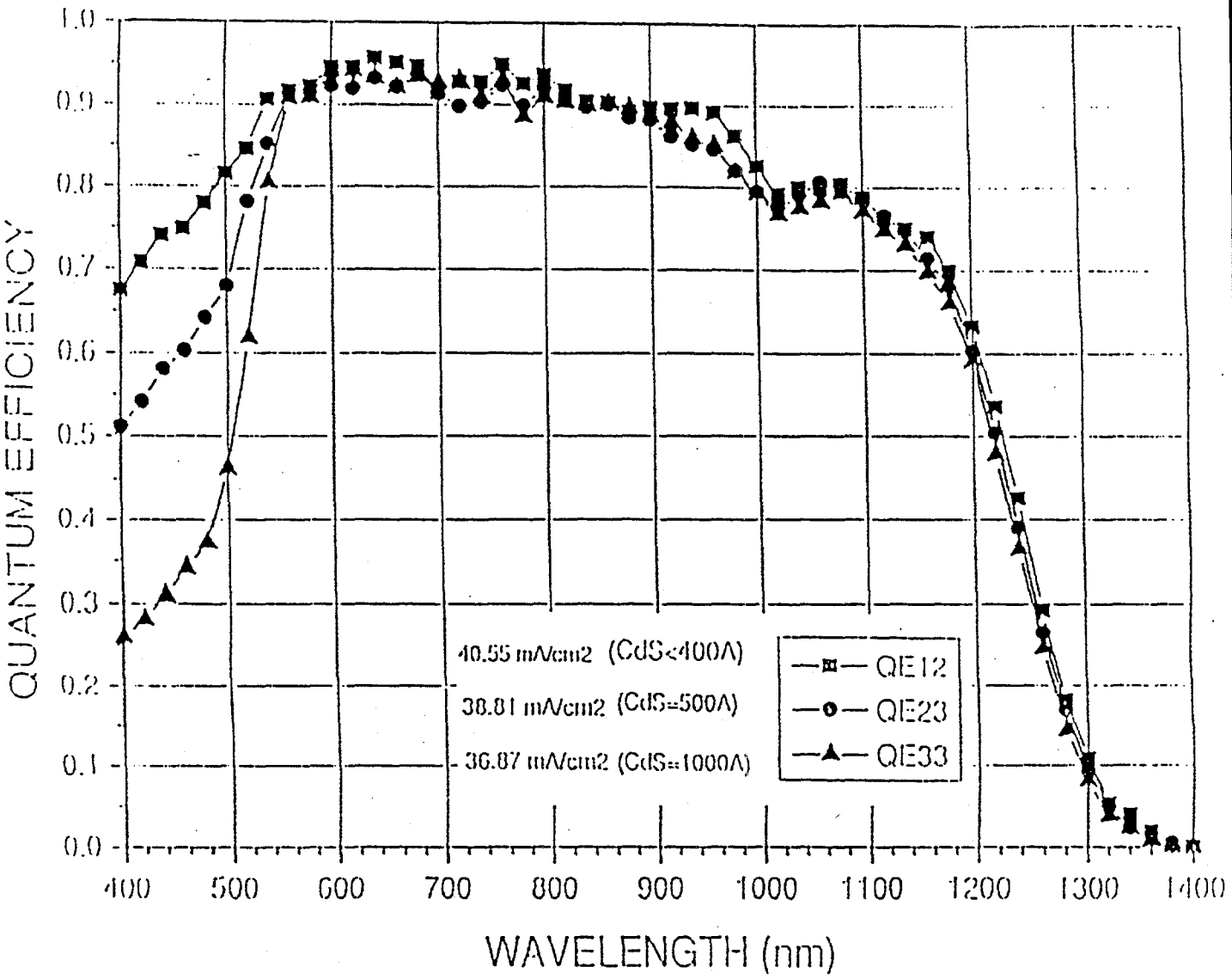
SPECTRAL Q.E. OF CIS SOLAR CELL
SHOWING EFFECT OF CdS THICKNESS
QUANTUM EFFICIENCY
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
400
500
600
700
800
900
1000
1100
1200
1300
1400
WAVELENGTH (nm)
40.55 mA/cm2 (CdS<400A)
38.81 mA/cm2 (CdS=500A)
36.87 mA/cm2 (CdS=1000A)
QE12
QE23
QE33

Figure 2-2

2.1.1.3 *Doping*

Due to the solution growth deposition mechanism, it is very difficult to incorporate dopants into the CdS film during the deposition. Indium (III), aluminum (III) and boron were added to the CdS bath during deposition in a range of concentrations. The dark conductivity of the films were measured using a four point probe arrangement with increased dark conductivity as the criteria for successful doping. The dark conductivity values show that there is no change in film conductivity between films deposited with and without dopant added to the deposition solution. The only observable effect is an inhibition of the film growth reaction when indium or aluminum is added to the bath solution. The effect becomes more severe as the concentration of dopant increases. It should be noted that this is strictly a surface effect in that it does not inhibit the precipitation reaction in solution, only the film growth on glass and substrate surfaces. The typical dark conductivities ranged from 10^8 to 10^{10} ohm-cm.

2.1.1.4 *Scale-up*

With the simple beaker design, (7), uniform CdS films can be deposited onto glass substrates up to 230 cm^2. But for larger areas, the use of a scaled up beaker design does not fulfill the requirement of being cost effective or functional. Some of the process limitation include:

1. This is a batch process - each deposition requires fresh solution, while at the same time the spent solution must be discarded - to keep the chemical consumption and waste to a minimum a system that uses the smallest quantity of solution would be desirable.

2. Deposition temperature and chemical corrosiveness limit the selection of tank materials - the material must be able to withstand exposure to strong bases and acids at elevated temperatures. This limits the construction materials to Pyrex glass, Teflon, stainless steel and polypropylene.

3. Stirring/Agitation - to get a uniform temperature distribution and constant flux of the chemical specie to the substrate, a method of agitation is needed.

With these constraints in mind, the design chosen for large area deposition is a narrow rectangular tank, with dimensions slightly larger than the substrate. **Figure 2-3** is schematic of the deposition tank.

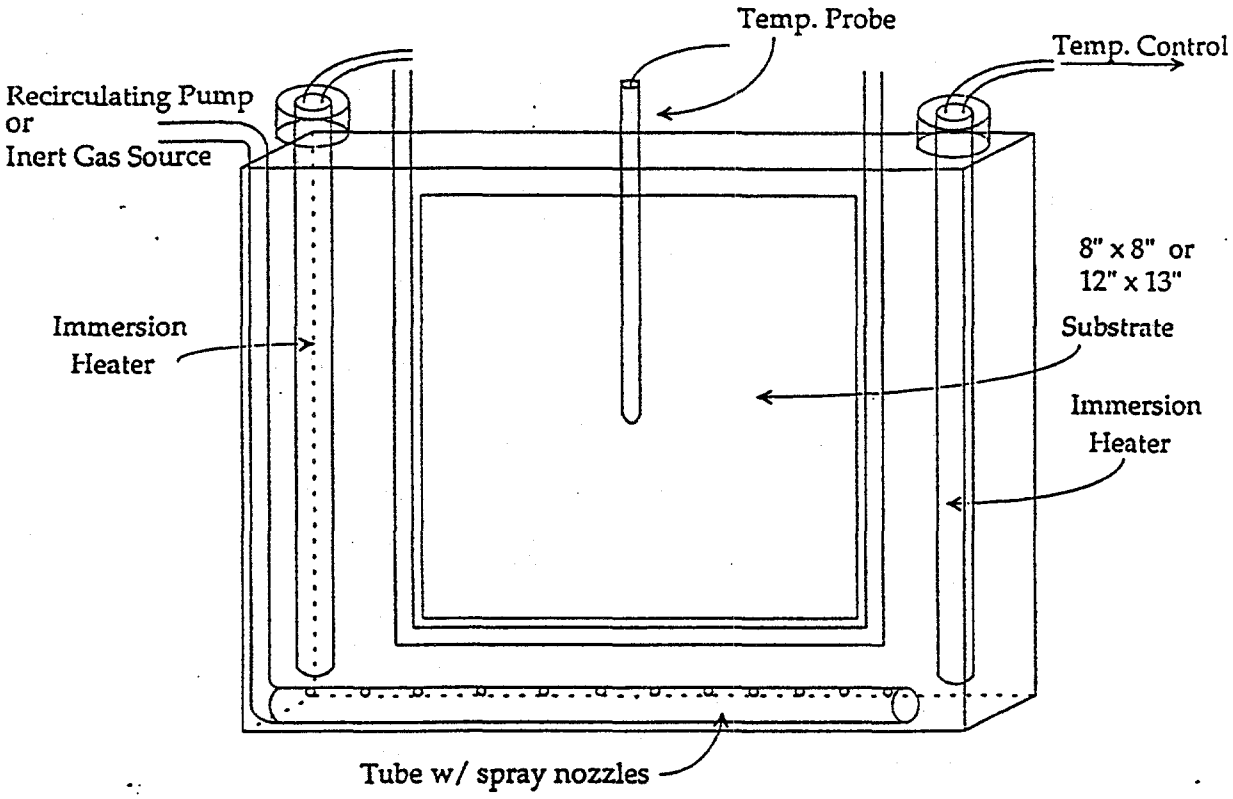

Figure 2-3 CdS chemical bath deposition tank schematic.

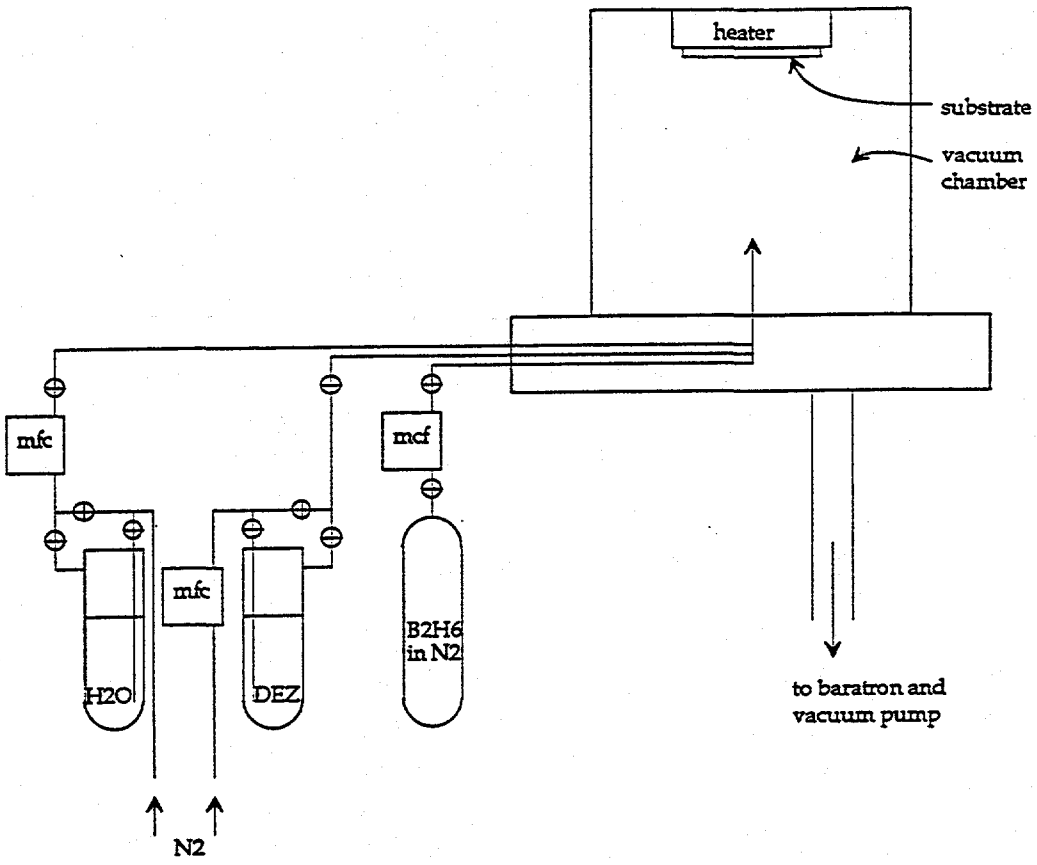

Figure 2-4 ZnO LPCVD deposition System Schematic.

The narrow rectangular design should minimize the volume of solution per unit area used in each deposition and allows for the deposition of more than one substrate at a time. Heating is provided by two quartz immersion heaters that are thermostatically controlled. For the 400 cm^2 substrate, the tank is made of Pyrex glass, while for the 1000 cm^2 substrate, a polypropylene tank is used.

In a narrow tank, a mechanical stirrer does not provide uniform agitation. As an alternative, a flow of solution can be generated from the bottom of the tank either by 1) recirculation of the solution through a long perforated tube located in the base of the tank; or 2) bubble an inert gas through a gas dispersion tube located again, at the base of the tank. The agitation rate can be controlled by restricting the flow of the gas or recirculating fluid. For preliminary runs, the bubble agitation method is used, with satisfactory results, but in the future it may be better to use the recirculation system since this provides a more homogeneous mixing of solution. The CdS deposition rate from the tank baths is much faster and goes to completion much sooner when compared to the small beaker bath. This increased rate may be due to either 1) a higher degree of agitation, that may increase the rate of the precipitate formation, a process similar to flocculation; or 2) a greater loss of NH_3 evaporation. The vapor is carried to the atmosphere by bubble agitation. Deposition conditions are being reoptimized to account for the changes in the process.

2.1.2 Zinc Oxide

Zinc oxide (ZnO) is deposited by either low pressure chemical vapor deposition (LPCVD) or RF sputtering. The LPCVD process has been specifically developed for use with CIS devices, while the sputtered ZnO is used for large area CIS modules.

2.1.2.1 *LPCVD ZnO Process*

In the LPCVD process, diethylzince (DEZ) and deionized water are used as the feedstock materials. Both are contained in individual stainless steel bubblers held in a controlled temperature bath. Diborane is used as the dopant and nitrogen is the carrier gas for all three compounds. The chemical flux is regulated by mass flow controllers. **Figure 2-4** is a schematic of the system. All three gases meet at the base of a stainless steel reactor column and are directed upward towards the heated substrate. The DEZ reacts with the water forming $Zn(OH)_2$, which loses a molecule of water forming ZnO when heated:

1. $(C_2H_5)_2Zn + 2\ H_2O$ ----> $Zn(OH)_2 + 2\ C_2H_6$
2. $Zn(OH)_2$ + heat ----> $ZnO + H_2O$

The deposition rate is determined by the substrate temperature and by the flux of DEZ to the substrate.

2.1.2.2 ***Optimization for CIS***

Acting as a front contact, the ZnO must have low resistivity and have good transmission across a wide spectrum. The effect of dopant concentration and substrate temperature were studied since these two factors seemed to most strongly effect the transmission and resistivity.

The film characteristics investigated include:

1. ZnO growth rate
2. Resistivity
3. Haze
4. Transmission spectra from 400 nM to 1400 nM

The substrate temperatures ranged from 150 to 190° C and at each temperature three different dopant concentrations were used, recorded as their flow rates: 10, 30 and 50 sccm of 1% diborane in nitrogen. All films were approximately 0.9 um thick. The test conditions and film data are compiled in **Table 2-1**. The DEZ and H_2O flow rates are held constant since their flow ratios have been previously optimized.

2.1.2.3 ***ZnO Growth Rate***

The growth rate at fixed DEZ flow increases linearly with increasing temperature. The deposition rate ranges from 1000A/minute at 150°C up to 2800 A/minute at 190°C. At lower temperatures, the rate is limited by the dissociation of the reacting species at the substrate, while at higher temperatures, the reactions become limited by the flux of chemicals to the heated surface (8). **Figure 2-5** shows the growth rate of the film versus temperature. Although not shown, the rate begins to level out with increasing temperature. This is probably due to the formation of ZnO being limited by the flux of the reactive species to the substrate.

TABLE 2-1

Effect of Deposition Temperature and Dopant Concentration

ZnO Film Characteristics (as deposited)

Run #	Substrate dep. temp.(°C)	Dopant Flow (sccm)	Sheet Resistance (ohms/sq.)	Thickness (um)	Resistivity (ohm-cm)	Trans. (%)	Haze (%)	Trans. @1400 nm	Dep. rate (Å/min)
1464	150	10	28-30	0.80	$2.3X10^{-3}$	87.1	0.3	92	888
1462	152	30	22-24	0.86	$1.97X10^{-3}$	86.6	2.6	83	1011
1465	152	50	27-30	0.87	$2.4X10^{-3}$	86.9	1.7	78	1023
1456	161-162	10	32-34	0.78	$2.5X10^{-3}$	87.5	2.8	92	1418
1457	162-163	30	19-21	0.80	$1.6X10^{-3}$	87.3	2.3	83	1454
1458	161	50	19-24	0.74	$1.6X10^{-3}$	87.5	1.6	77	1345
1455	171	10	22-24	0.80	$1.8X10^{-3}$	86.9	4.7	93	1777
1460	171	30	15-16	0.83	$1.3X10^{-3}$	87.0	3.2	80	1844
1454	171	50	18	0.82	$1.4X10^{-3}$	87.3	1.8	75	1822
1471	181	10	18-20	0.79	$1.5X10^{-3}$	87.5	4.1	88	2257
1467	181	30	11-12	0.95	$1.1X10^{-3}$	86.4	2.3	66	2375
1466	181	50	13	0.91	$1.2X10^{-3}$	85.0	1.4	57	2275
1477	189	10	14-15	0.98	$1.4X10^{-3}$	88.0	3.2	82	2800
1473	188-192	30	14-15	0.99	$1.4X10^{-3}$	86.5	1.1	55	2828
1475	189-190	50	18-19	0.96	$1.7X10^{-3}$	85.8	0.9	53	2750

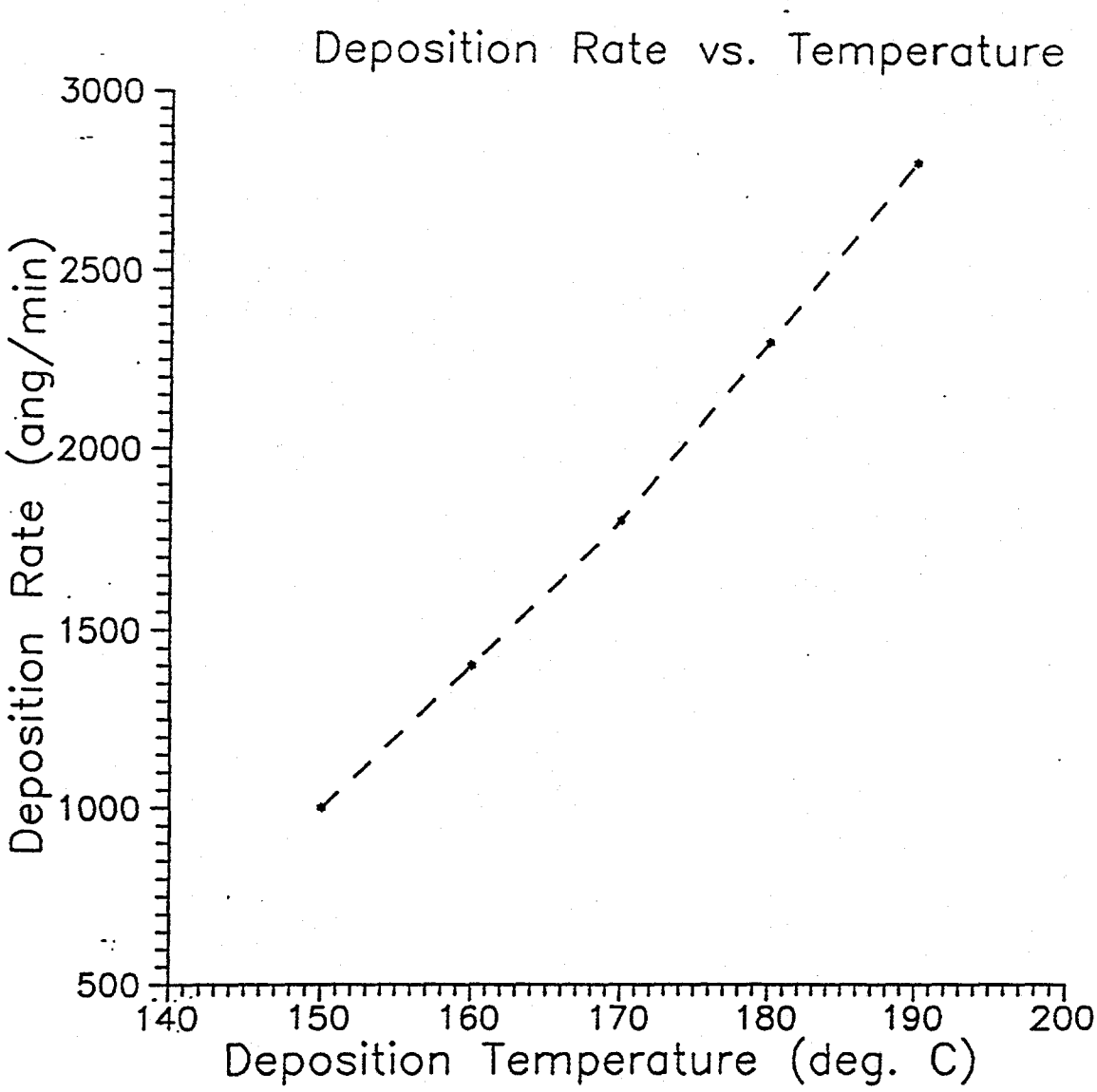
Deposition Rate vs. Temperature
Deposition Rate (ang/min)
3000
2500
2000
1500
1000
500
140
150
160
170
180
190
200
Deposition Temperature (deg. C)

Figure 2-5

2.1.2.4 ***Resistivity***

Figure 2-6 shows the change in resistivity with temperature. As the temperature increases, there is corresponding decrease in resistivity up to temperatures of 180°C, after that, it begins to increase. This is true for all dopant concentrations. The films with 10 sccm diborane have higher resistivities overall, while there is little difference between films deposited with 30 and 50 sccm dopant.

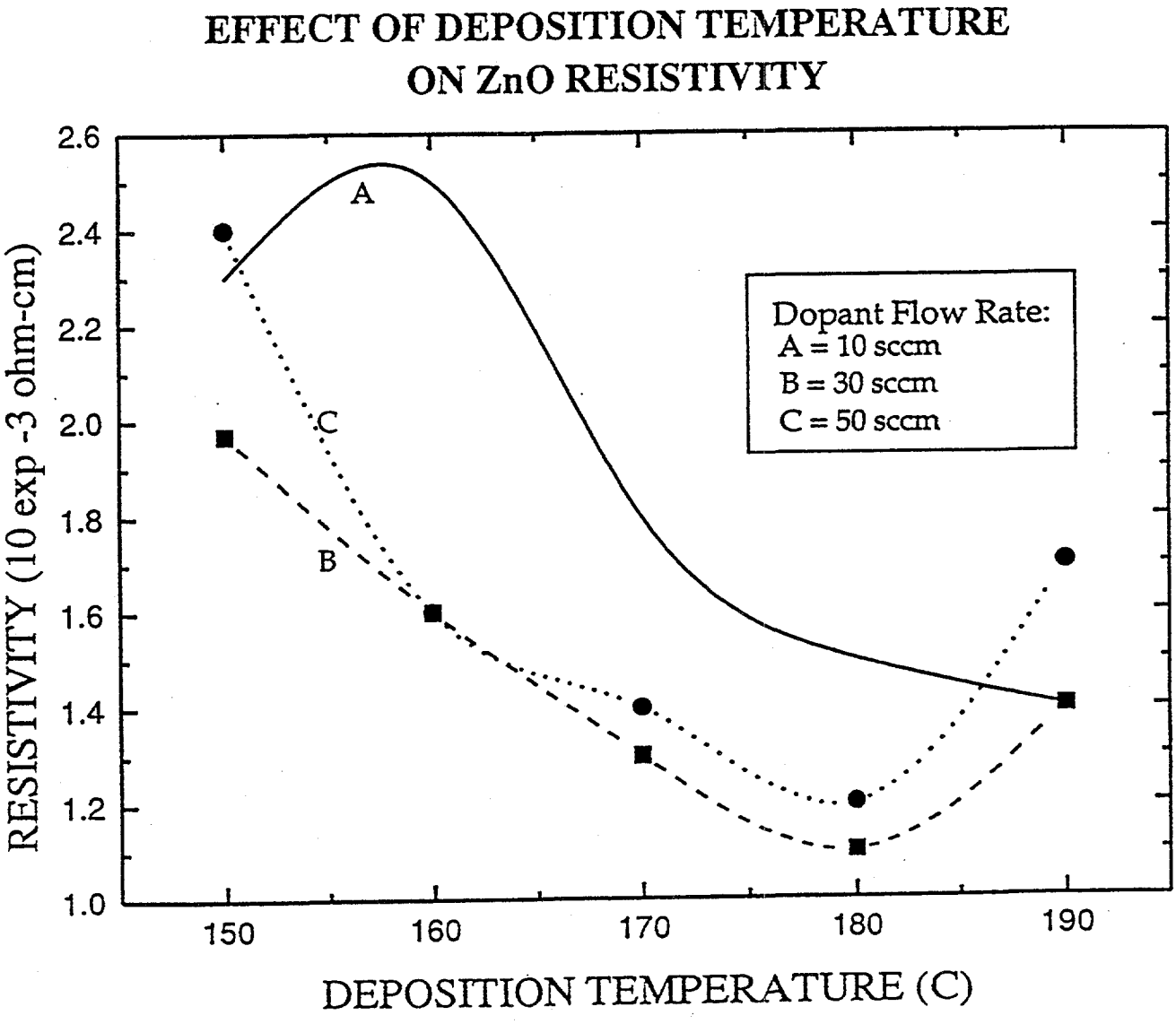

Figure 2-6

2.1.2.5 ***Haze***

The haze is measured using a commercial hazemeter (BKY Gardner Co.). The percent haze versus temperature is shown in **Figure 2-7**. The haze of all films increases up to deposition temperatures of approximately 170°C, then it starts to decrease. This effect is probably related to the change in the reaction kinetics, as the flux of the DEZ is not fast enough to keep up with the reaction rate. It can also be seen that by increasing the dopant flow rate, the film texture decreases. This may be advantageous in that a particular haze can be obtained by adjusting the dopant level.

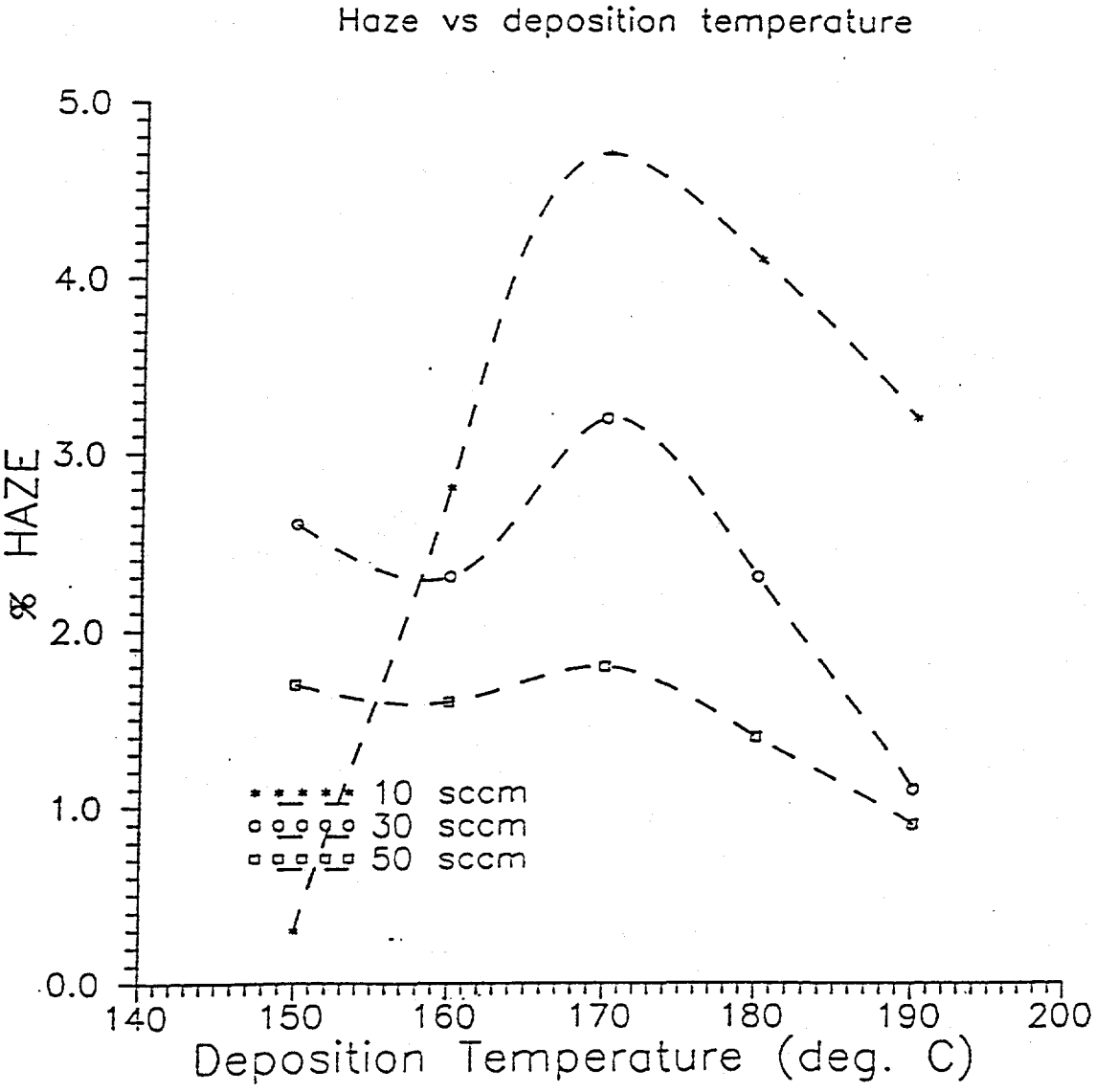

Figure 2-7

2.1.2.6 *Transmission Spectra*

The transmission spectra for all films is run from 400 to 1400 nm. The spectra is strongly influenced by absorption in the long wavelength region. **Figure 2-8** shows the transmission value at 1400 nm and how it is related to dopant concentration and deposition temperature. The long wavelength transmission is a function of the doping concentration up to depositions temperatures of 170°C, after that the transmission rapidly decreases as a function of the deposition temperature. The increased absorption is attributed to greater incorporation of boron into the films, but this increased concentration of dopant does not necessarily translate into a less resistive film as seen in the resistivity data.

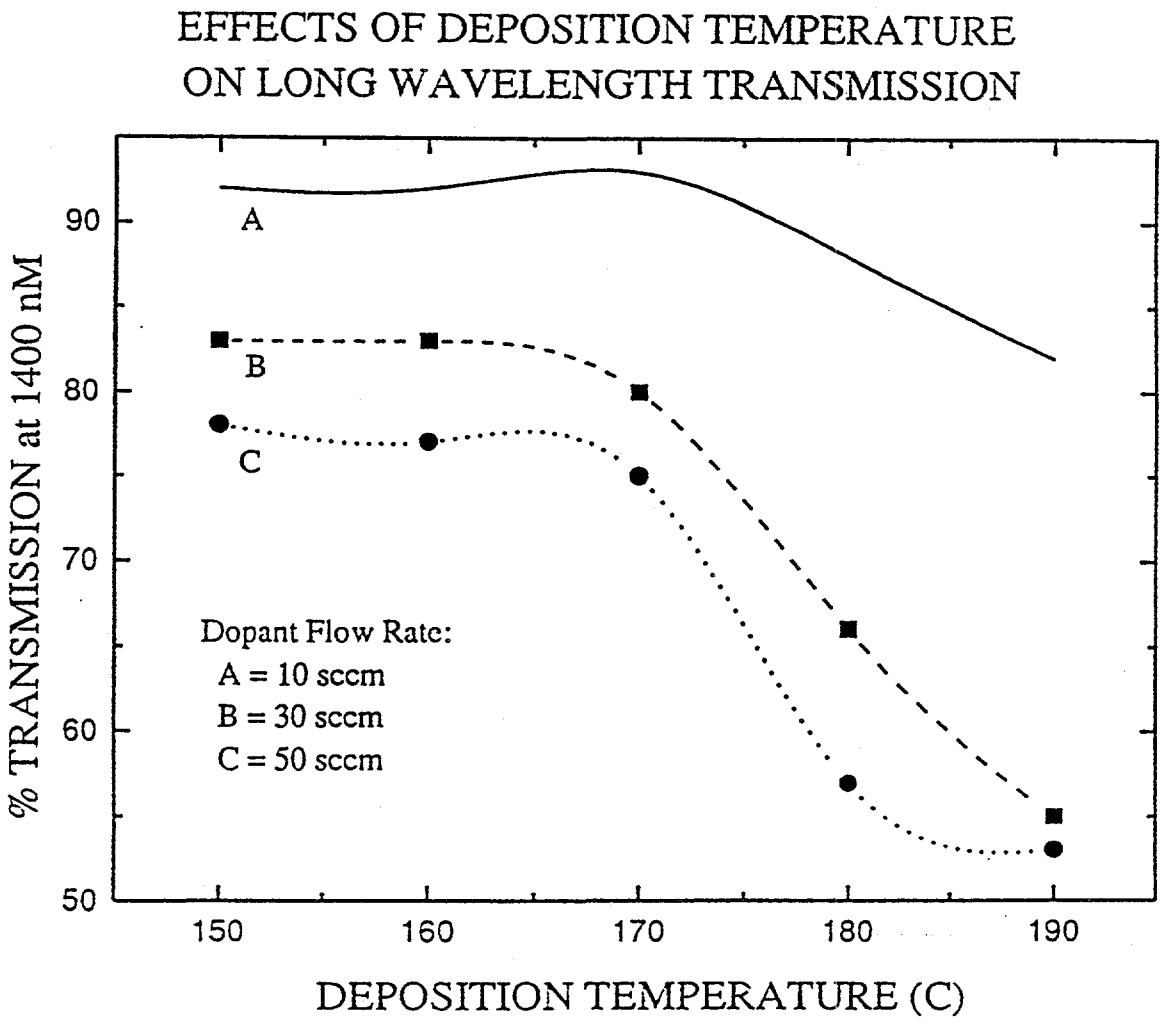

Figure 2-8

2.1.2.7 *Scale-up*

The LPCVD system is originally designed to handle substrates up to 60 cm^2. By enlarging the reactor column and the heated substrate holder, the deposition area is increased to 230 cm^2. Because of the size limitations of the LPCVD chamber, this is the maximum allowable deposition area. The ZnO uniformity across a 230 cm^2 substrate is shown in **Figure 2-9**. The substrate is soda lime glass and the sheet resistance, visible transmission and film thickness are shown for each quadrant. For the 400 cm^2 and 1000 cm^2 substrates, RF sputtered ZnO is used. The ZnO target contains 2% (by weight) aluminum as dopant. The sputtered ZnO films are highly specular and have resistivities less than $9X10^{-4}$ ohm-cm. **Figure 2-10** is a comparison of sputtered and LPCVD ZnO. Both have similar sheet resistance. Although the LPCVD film is thicker, it has much better long wavelength transmission. It should be noted that the sputtered films have been optimized for low resistivity, and not for use with CIS.

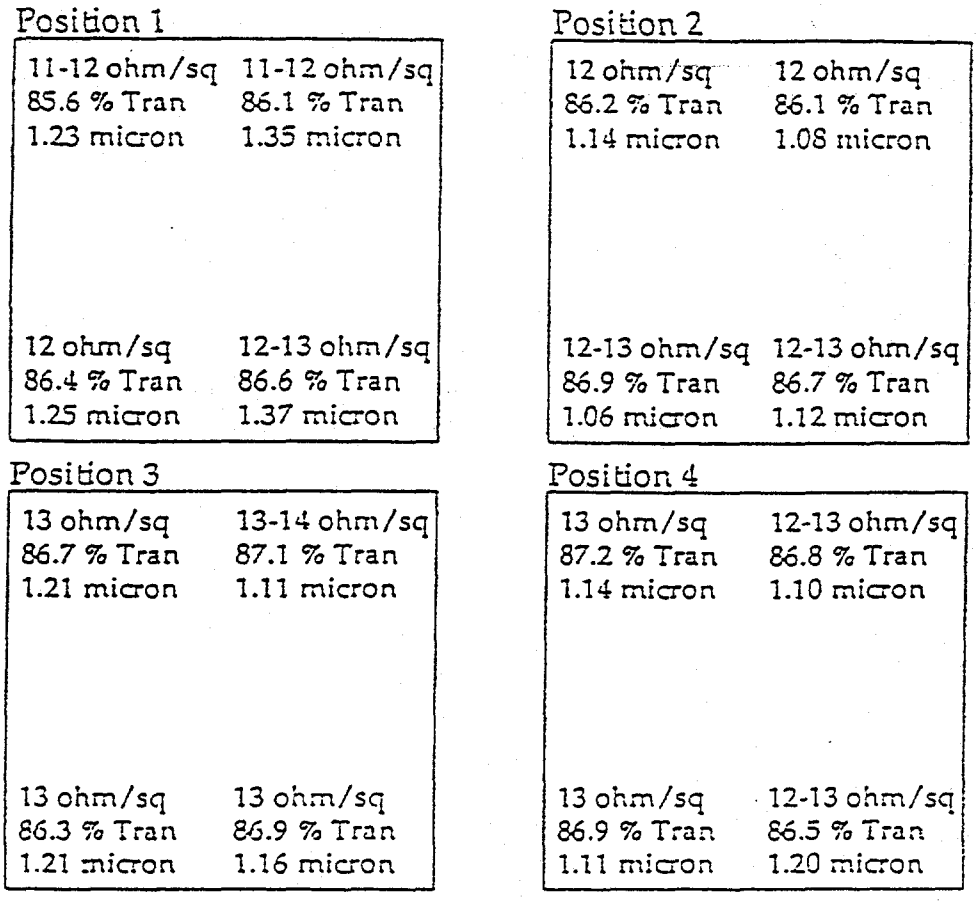

Figure 2-9 ZnO Uniformity across a 230 cm^2 substrate.

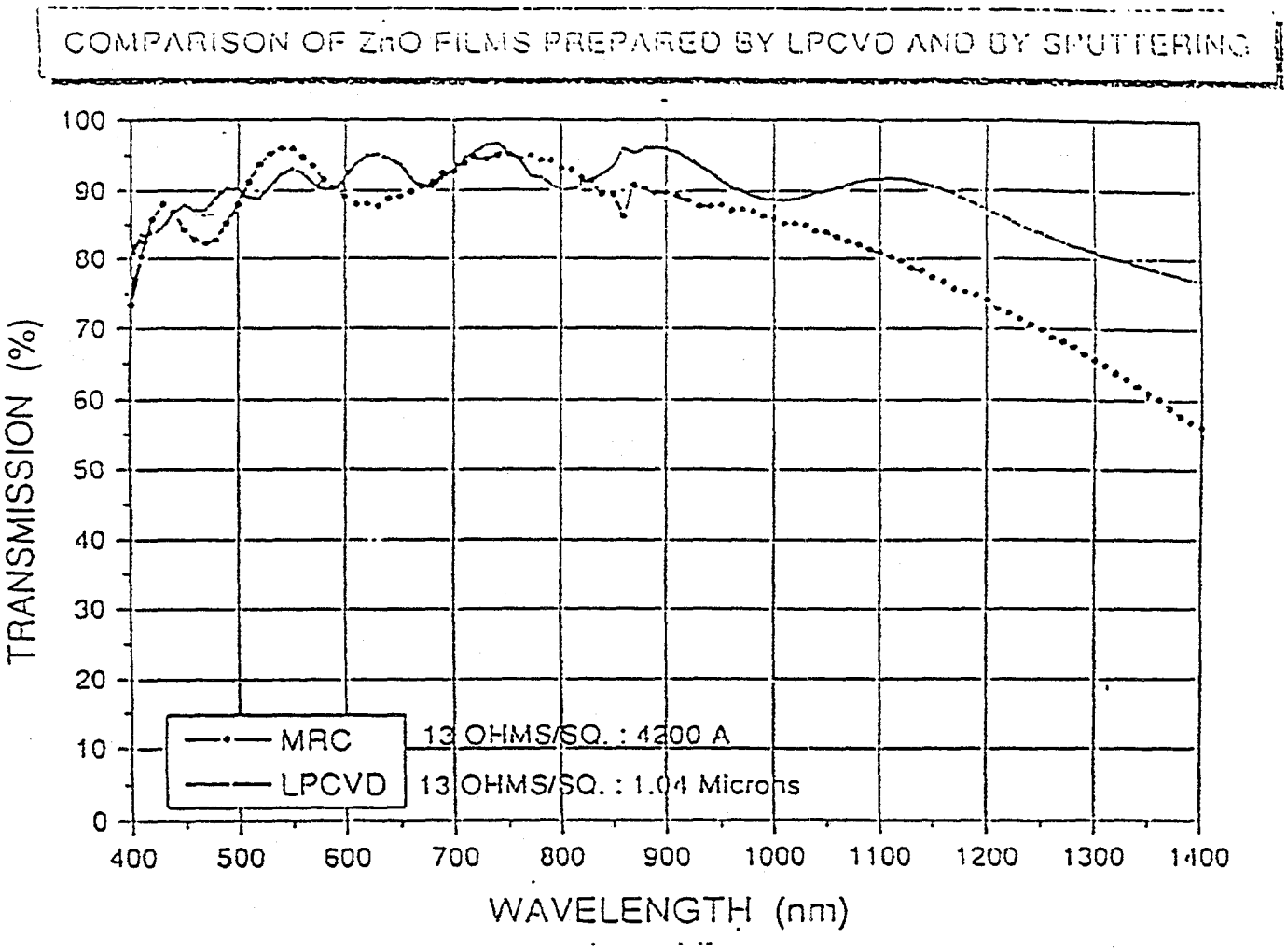
COMPARISON OF ZnO FILMS PREPARED BY LPCVD AND BY SPUTTERING
TRANSMISSION (%)
100
90
80
70
60
50
40
30
20
10
0
400
500
600
700
800
900
1000
1100
1200
1300
1400
WAVELENGTH (nm)
MRC
13 OHMS/SQ. : 4200 A
LPCVD
13 OHMS/SQ. : 1.04 Microns

Figure 2-10

2.1.2.8 *Alternative Oxidants*

As an alternative to the water feedstock, gaseous oxygen (O_2) is used as the oxidant. Since the O_2 reacts so readily with DEZ, the system is modified so that the O_2 is introduced at the heated substrate. In this process, the DEZ is directly oxidized by the O_2 to form ZnO:

$$(C_2H_5)_2Zn + 7\ O_2 \text{ ----> } ZnO + 4\ CO_2 + 5\ H_2O \qquad (9)$$

From this mechanism, it can be seen that the O_2 must be available in large excess in order for the products to form. The deposition rate is much slower when compared to the rate of films deposited using H_2O, 100 A/min versus 1800 A/min. The process is not as efficient, since much of the DEZ is converted to ZnO powder before reaching the heated substrate. The films are highly specular and very adherent.

2.1.3 Combined Effects of CdS/ZnO Window Layers

In order to better understand the effect of the CdS and ZnO layers on the CIS, the transmission of the combined ZnO and CdS layers are studied. In this experiment, three different ZnO layers are deposited on four different thickness of CdS. The substrate material is soda lime glass. The deposition data is tabulated in **Table 2-2**. The three types of ZnO used include: a thick, low resistivity film, a thinner film with the same amount of dopant and a thin film with a minimum dopant level. Previous data has shown that the thicker ZnO films with the high levels of dopant are the least resistivity, but they are also more absorbing in the long wavelength region. Because this region is still active for CIS, the increased absorption strongly affects the PV characteristics. What happens is that the window layer become a compromise where transmission is sacrificed for low resistance. The goal is to minimize the transmission losses, while maintaining low resistivity.

The transmission spectra of the combined layers is shown in **Figures 2-11, 2-12 and 2-13**. Each spectra shows the transmission of the four different thickness of CdS at each ZnO condition: 7, 13 and 25 ohms/sq., respectively.

In order to compare the transmission loss, the ratio of film transmission at certain wavelengths is compared for the different deposition conditions. The closer the value is to one, the lower the amount of absorption and the better the transmission. In the short wavelength region, the ratio taken is 425:512 nm and in the long wavelength region, the ratio is 1400:1200 nm. The transmission values of the films are compared in **Table 2-3**. From this data, it is seen that the

short wavelength transmission is controlled by the CdS thickness and is independent of the ZnO film characteristics. As the CdS thickness increases, the short wavelength transmission ratio decreases, yet the long wavelength are relatively constant for a given CdS thickness. In the long wavelength region, the transmission is dominated by the long wavelength absorption due to the ZnO. Here the long wavelength ratio does not vary with CdS thickness but changes with the type of ZnO. The films with the least amount of dopant show the least amount of absorption while the thicker films show the most absorption.

TABLE 2-2
Combined CdS/Zno Layers

ID #	CdS Thick. (um)	ZnO Dep. Temp(°C)	ZnO dopant Flow (sccm)	ZnO Sheet resistance (ohm/sq.)	ZnO Thick. (ohm/sq.)	ZnO resistivity (ohm-cm) ZnO re-sist.	ZnO Haze (%)	ZnO Trans. (%)
1634	0.03	181	30	7-8	1.43	$1.14X10^{-3}$	3.9	83.4
1635	0.05	181	30	7-8	1.46	$1.09X10^{-3}$	4.1	83.3
1636	0.09	182	30	8-9	1.42	$1.42X10^{-3}$	3.7	83.3
1637	0.19	182	30	7-7	1.46	$1.02X10^{-3}$	8.2	82.8
1643	0.03	181	30	13-15	0.79	$1.10X10^{-3}$	1.2	86.8
1644	0.05	182	30	12-12	0.92	$1.10X10^{-3}$	2.2	86.4
1645	0.09	182	30	13-14	0.83	$1.12X10^{-3}$	1.9	86.7
1646	0.19	180	30	12-12	0.88	$1.06X10^{-3}$	2.5	86.4
1650	0.03	173	10	24-25	0.78	$1.87X10^{-3}$	4.4	87.3
1649	0.05	173	10	24-25	0.79	$1.82X10^{-3}$	4.5	87.0
1652	0.09	174	10	22-23	0.82	$1.84X10^{-3}$	5.1	87.0
1643	0.19	175	10	25-25	0.70	$1.75X10^{-3}$	4.1	87.4

TABLE 2-3
CdS/ZnO Transmission

ID #	% Trans. @ 425 nm	% Trans. @ 512 nm	Ratio 425/512	% Trans. @ 1400 nm	% Trans. @ 1200 nm	Ratio 1400/1200
1634	76	85	0.89	40	63	0.65
1635	56	76	0.73	40	63	0.64
1636	38	68	0.55	36	58	0.61
1637	17	60	0.28	35	58	0.61
1643	80	88	0.91	64	78	0.82
1644	58	77	0.75	68	78	0.88
1645	40	69	0.58	67	71	0.94
1646	17	64	0.26	58	77	0.75
1650	76	87	0.87	93	93	1.00
1649	56	79	0.70	94	91	1.03
1652	35	68	0.52	89	81	1.21
1647	18	61	0.29	83	79	1.05

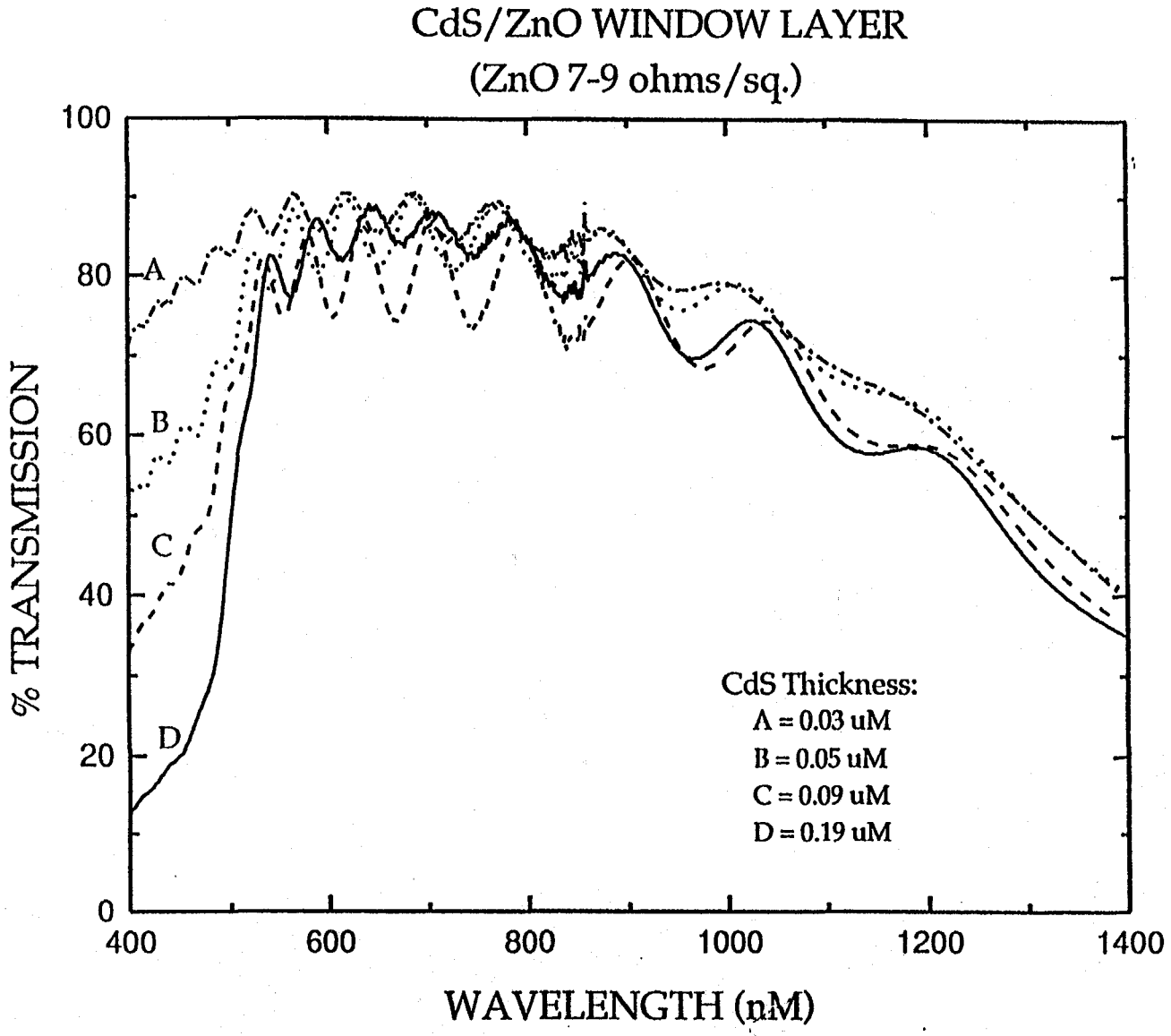
CdS/ZnO WINDOW LAYER
(ZnO 7-9 ohms/sq.)
% TRANSMISSION
WAVELENGTH (nM)
100
80
60
40
20
0
400
600
800
1000
1200
1400
A
B
C
D
CdS Thickness:
A = 0.03 uM
B = 0.05 uM
C = 0.09 uM
D = 0.19 uM

Figure 2-11

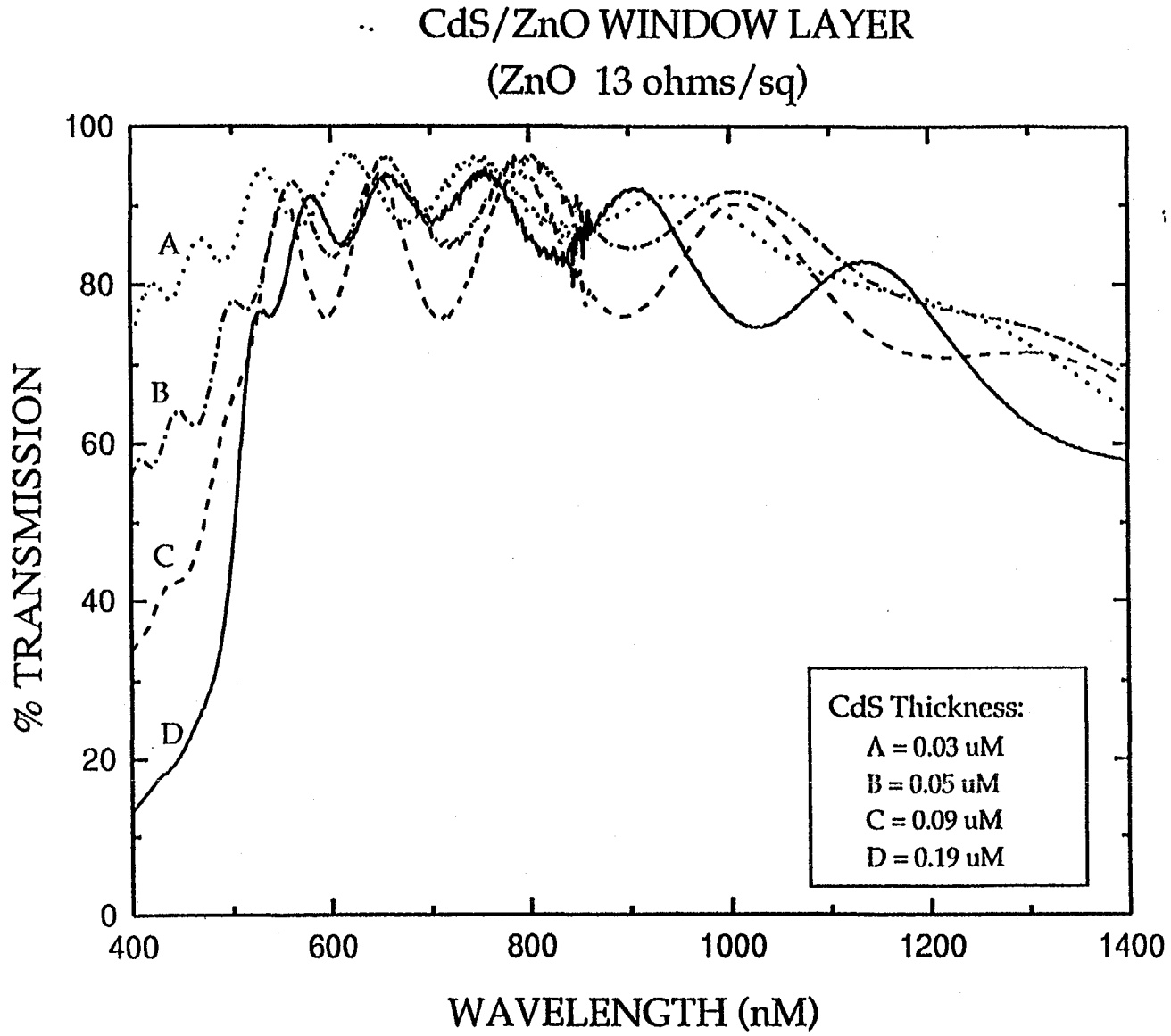
CdS/ZnO WINDOW LAYER
(ZnO 13 ohms/sq)
% TRANSMISSION
WAVELENGTH (nM)
100
80
60
40
20
0
400
600
800
1000
1200
1400
A
B
C
D
CdS Thickness:
A = 0.03 uM
B = 0.05 uM
C = 0.09 uM
D = 0.19 uM

Figure 2-12

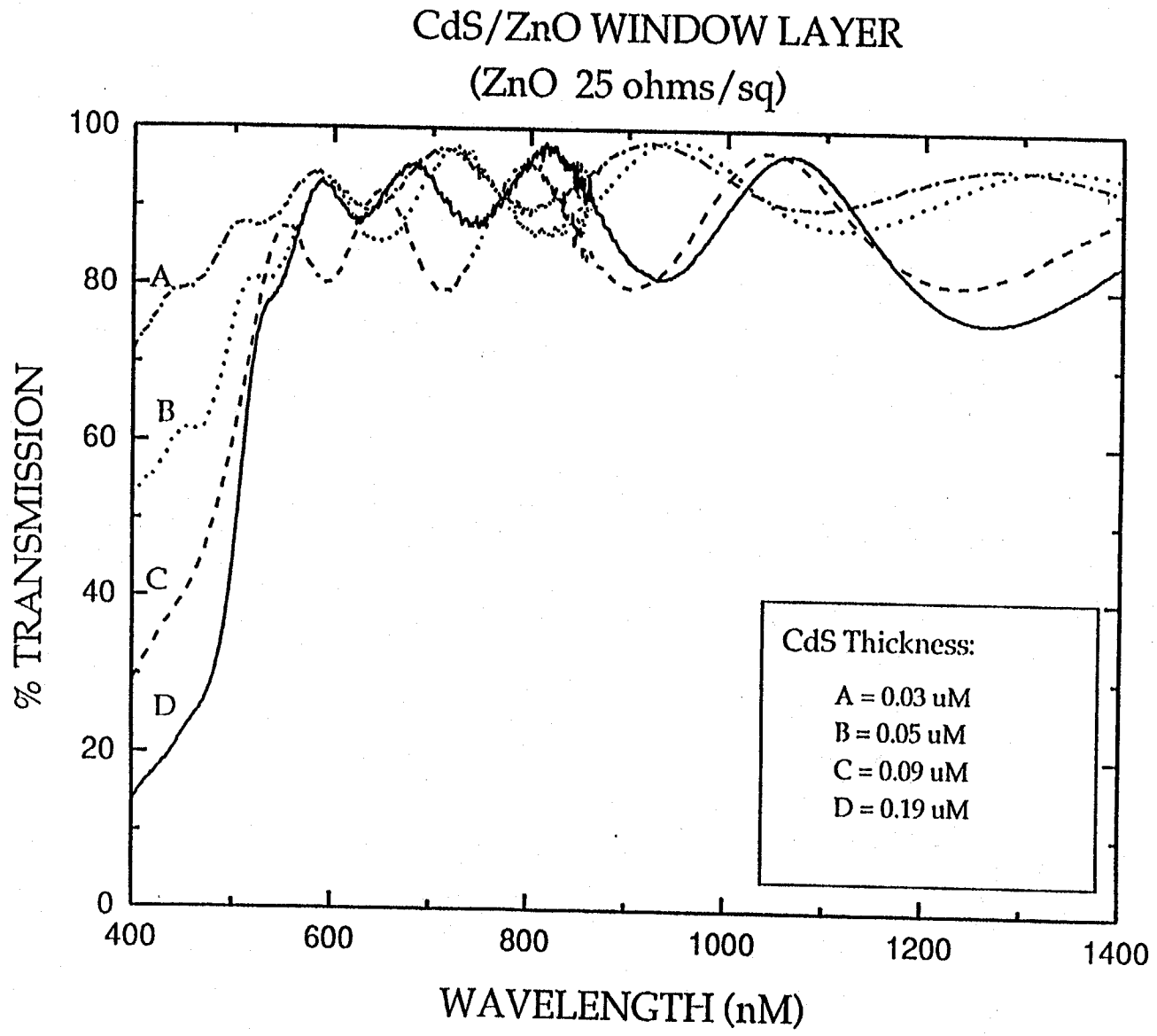
CdS/ZnO WINDOW LAYER
(ZnO 25 ohms/sq)
% TRANSMISSION
100
80
60
40
20
0
400
600
800
1000
1200
1400
WAVELENGTH (nM)
A
B
C
D
CdS Thickness:
A = 0.03 uM
B = 0.05 uM
C = 0.09 uM
D = 0.19 uM

Figure 2-13

2.1.4 Substrates and Contacts

The different substrate material used include:

molybdenum on Corning 7059 glass and soda lime glass
molybdenum\NiCr on soda lime glass
molybdenum\CTO (specular and textured) on soda lime glass

Soda lime glass is the preferred substrate material since it matches the thermal coefficient of expansion of the CIS much better than Corning 7059 glass, lessening stresses on the CIS during heat treatments. There is also no need to use a high quality optical glass as the substrate.

Molybdenum is normally sputtered onto the substrate, but evaporated molybdenum has also been used. The purpose of the intermediate NiCr and CTO layers is to improve the adhesion of the molybdenum to the glass substrate. The CTO layer also improves laser scribing during module fabrication.

3.0 TASK II: ABSORBER LAYER

The goal of this task is to identify a manufacturable process for the formation of device quality CIS. The constraints are many; the process must be applicable to deposition on very large area, it must be inexpensive, and it should avoid the use of volatile toxic compounds. The CIS deposition methods which have been evaluated during this period include:

1. Three source Co-sputtering of Cu, In and Se
2. The 'Hybrid' process - Metals sputtering with Se evaporation
3. Elemental Deposition and Compound Formation (EDCF) process

3.1 Three Source Co-sputtering of Cu, In and Se

This process is analogous to the three source evaporation used by the Boeing group and others to produce very efficient small area CIS and CIGS cells. As in the coevaporation method the elemental flux was incident on heated substrates (400°C to 450°C). During the sputtering process the physical properties of Se, such as low thermal conductivity, allowed hot spots to develop on the surface of the Se target. This, in turn, caused some difficulty in controlling the sputter rate and uniformity of the Se. Stoichiometric films of CIS were nonetheless produced using this approach before other methods were pursued.

3.2 Hybrid process - Metals sputtering with Se evaporation

This approach avoided the difficulty of sputtering Se. Moreover, evaporation of the Se is easily controlled and occurs readily at a low (~375°C) temperature. This process also results in a ternary flux to the substrate surface, like the Boeing process. Unfortunately, at sputtering pressures the evaporative flux of Se is scattered significantly. Thus the actual delivery of Se to the substrate is reduced, and scattered Se reacts with the surface of the Cu and In sputtering targets. This condition is undesirable, as it led to poisoning of the metal targets with Se and subsequent variation in metal deposition rate.

Few good devices were made with material produced using either of the above processes, in contrast to devices typically resulting from the three source evaporation method. Inadequate control, related to issues mentioned above, could be responsible. It also should be remarked that neither of the above processes provide an elemental flux which is instantaneously stoichiometric as in the case of three source evaporation.

In effect, uniformity during sputter deposition is usually obtained through motion of the substrate. In the presence of multiple sputtering targets the flux of any one element inevitably varies periodically with the substrate motion.

3.3 Elemental Deposition and Compound Formation

The largest share of our effort to date has focused on Elemental Deposition and Compound Formation which entails deposition of the elements sequentially onto a substrate, at low temperature, followed by thermal conversion to chalcopyrite CIS at high temperature. The sequential deposition , rather than codeposition relaxes many constraints. In our process the elemental "stack" is easily produced by sputtering of the metals and evaporation of the Se. This is a manufacturable process, easily applicable to large area substrates and avoids use of volatile toxic compounds. The complication in this approach lies in conversion of the elements to CIS.

Using the EDCF process copper and indium metallic layers are sputter deposited onto a molybdenum/soda-lime glass substrate. The copper-indium precursors which have been studied range from complete mixtures of Cu-In via codeposition, discrete layers of these metals, multiple alternating layers Cu and In, and layers having special compositions of Cu-In intended to form specific phases (e.g. the phase) in the Cu-In binary system. Low temperature heat treatments to aid precursor formation, in vacuo, have also been introduced at this point, followed by deposition of the Se layer by evaporation. The current equipment at Solarex is capable of deposition of the elemental stack onto substrates as large as 12"x13". The stoichiometric uniformity obtained using the current equipment for various substrate sizes is shown in **Figure 3-1.**

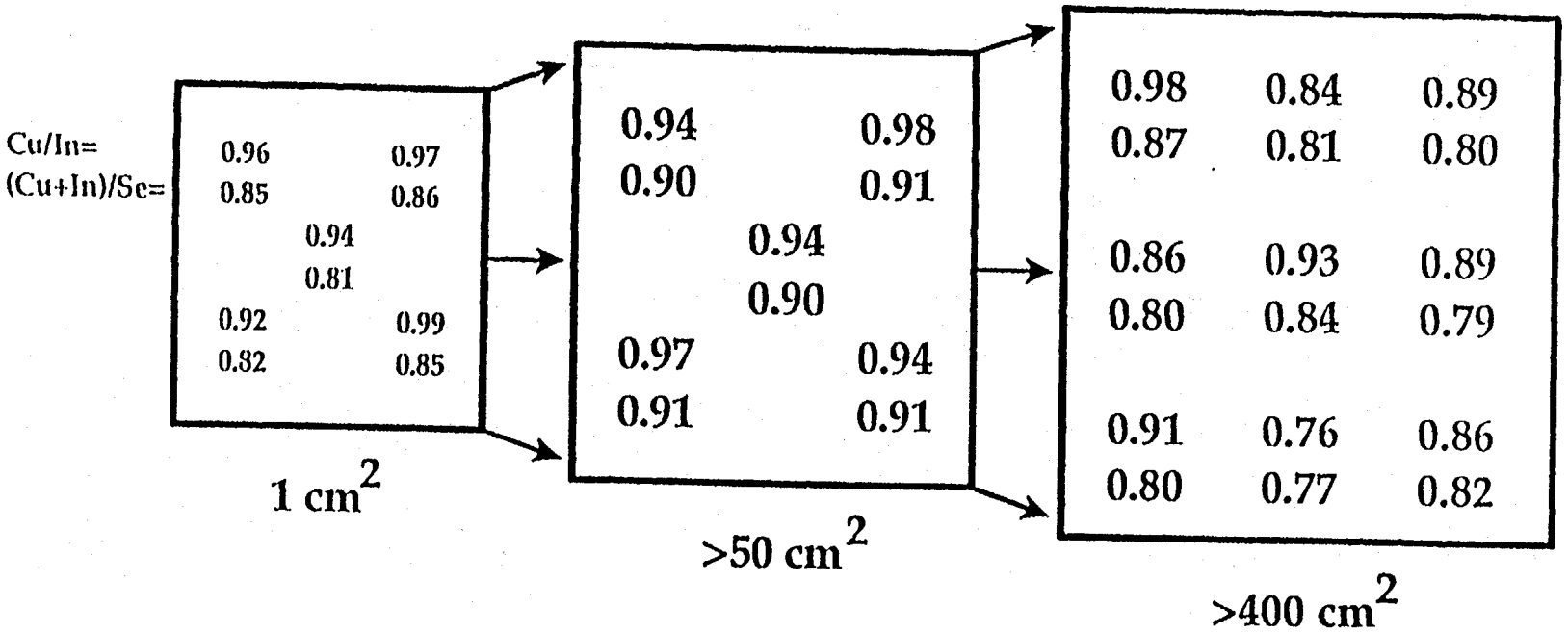

Figure 3-1. Composition Uniformity on three sizes of substrates.

Although compound formation of chalcopyrite CIS is induced simply by heating the elemental stack, many other undesirable results are possible such as formation of copper selenides and indium selenides. Other important factors include variation of stoichiometry on a microscopic scale, indium loss during conversion, grain formation, and the nature of the grain boundary. This step is complex - the chemical pathways available to the elements in the stack are influenced by diffusion (both liquid and solid state), evaporation, nucleation, reaction and possibly segregation.

Variables which have been determined to be important in the formation of good quality CIS are the heat treatment temperature, the variation of the temperature profile vs. time, and the starting precursors. Another crucial factor in this process is the availability of Se to the compound surface at elevated temperatures. The selenium on top of the stack changes from solid to liquid to vapor as the temperature during compound formation rises, thus allowing significant Se loss. Special provisions must be made to confine the Se vapor near the compound surface long enough to allow proper CIS formation.

Proof of concept for the EDCF process was obtained using elemental stacks of copper, indium and selenium as described above and heat treatment in a conventional tube furnace. Selenium confinement was attained by sealing the 1"x3" samples inside an evacuated glass ampule prior to heat treatment and compound formation. Small area devices of reasonable efficiency could be obtained, the best one being over 10% in conversion efficiency. In order to extend the EDCF approach to larger substrates, and to improve the process control and reproducibility, the compound formation step was moved to a load-locked, stainless steel, high vacuum chamber capable of 12"x13" substrate size. Provisions were made to heat the substrate and Se confinement was accomplished through a combination of physical means and an ambient of inert gas at a substantial pressure.

Larger substrates (up to 8"x8") were successfully taken through the conversion process to CIS using the load-locked equipment. In addition, many functional small area CIS cells and several submodules up to about 25 cm^2 have resulted. However, the control and reproducibility obtained in the compound formation step using this larger equipment is not yet sufficiently improved. Currently this is a major focus of effort.

The Typical parameters for the compound formation step are found in **Table 3-1**

TABLE 3-1	
Entry Temperature	250 - 350°C
Temperature Ramp	Linear
Heat Treatment	375 - 475°C
Ambient	Argon

3.3.1 Film Adhesion

Good adhesion of the constituent layers of the thin film solar cell to the substrate is one requirement of successful PV manufacture and use. Problems with adhesion in thin film CIS based cells has been observed by other groups, either on a macro or a microscopic scale. Peeling of CIS films produced using the EDCF process has occurred under some conditions. When this poor adhesion has occurred it seems to have been related to a high void density in the CIS material at the CIS/molybdenum interface, excessive selenization of the molybdenum itself, or use of LPCVD deposited ZnO having high stress on a weakly adhered CIS film. The first two problems are related to the compound formation conditions, and are under study. The latter problem has been avoided in our laboratory by using sputtered ZnO, and should not be an issue after proper conditions are found for the compound formation. Although the sputter deposition of ZnO takes longer, the optical and electrical properties are comparable to those of the LPCVD ZnO.

3.3.2 Materials Measurements

The ultimate indicator of absorber material quality is device performance. In addition to device results, which will be discussed in section 4, we make use of several materials measurements. We have used electron microprobe analysis (EMPA), Auger electron spectroscopy, x-ray diffraction (XRD) and photoluminescence measurement. CIS material formed using the EDCF process is routinely characterized by scanning electron microscopy (SEM) and energy dispersive analysis by x-rays (EDAX), giving useful information on elemental composition, grain size and morphology. Using such analysis we have determined necessary dependencies such as that of final compound composition on starting composition of the elemental stack for a given heat treatment schedule (**Figures 3-2 and 3-3**). It is evident by examination of **Figure 3-3**, for example that indium loss occurs during compound formation which is related to the starting quantity of Se in the stack. Less indium loss for higher starting Se content in the stack could

result if greater starting Se favors the formation of InSe over In_2Se which is suspected of being more volatile than the former.

The dependence of grain size on Cu/In ratio has also been studied using SEM analysis (**Figure 3-4**). It is apparent that the large grains usually associated with good device behavior are favored at copper rich compositions for the EDCF process. This behavior is similar to that reported for other processes such as 3-source evaporation. In general, the CIS films formed by EDCF show a mixed morphology, i.e. large grains are surrounded by numerous smaller grains. However, various heat treatment parameters and compositions can result in films which consist almost exclusively of large grains (**Figure 3.5**).

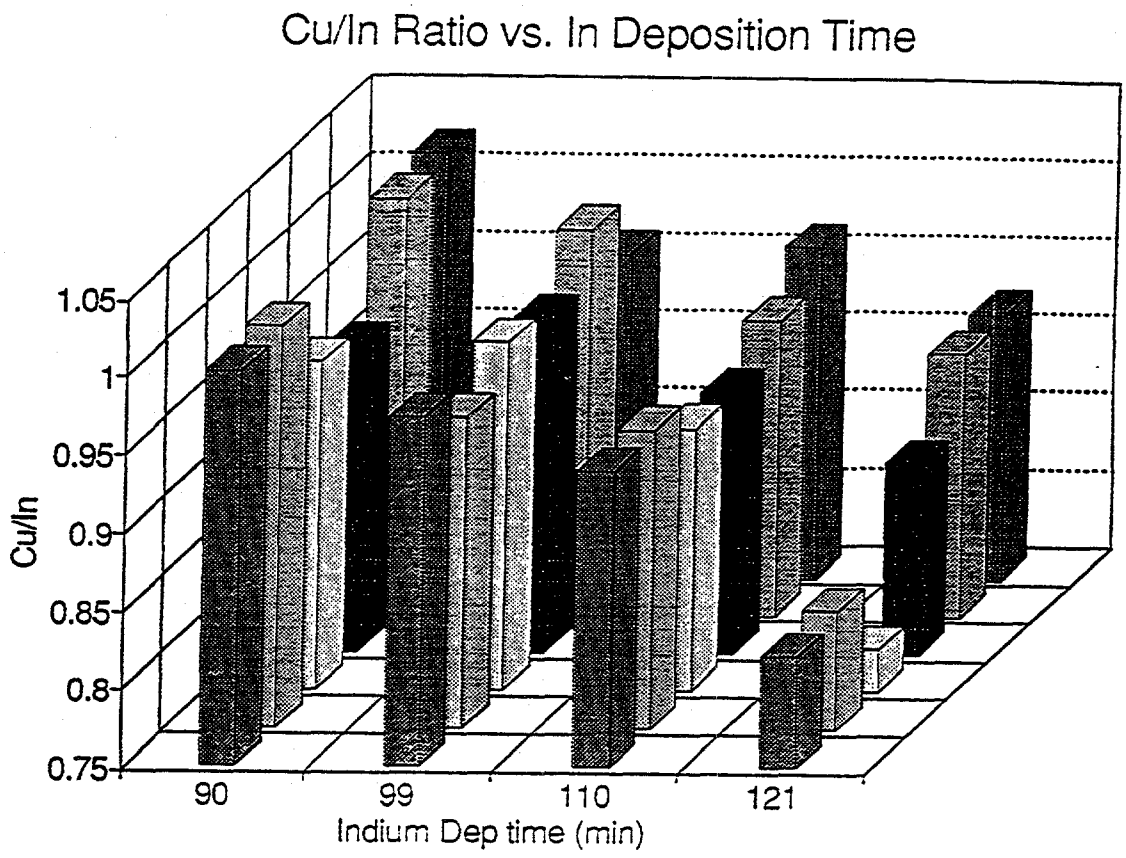

Figure 3-2 Copper to indium ratio in the CIS film as a function of indium content in the elemental stack, for 6 different heat treatment schedules. Starting copper content in the stack was constant.

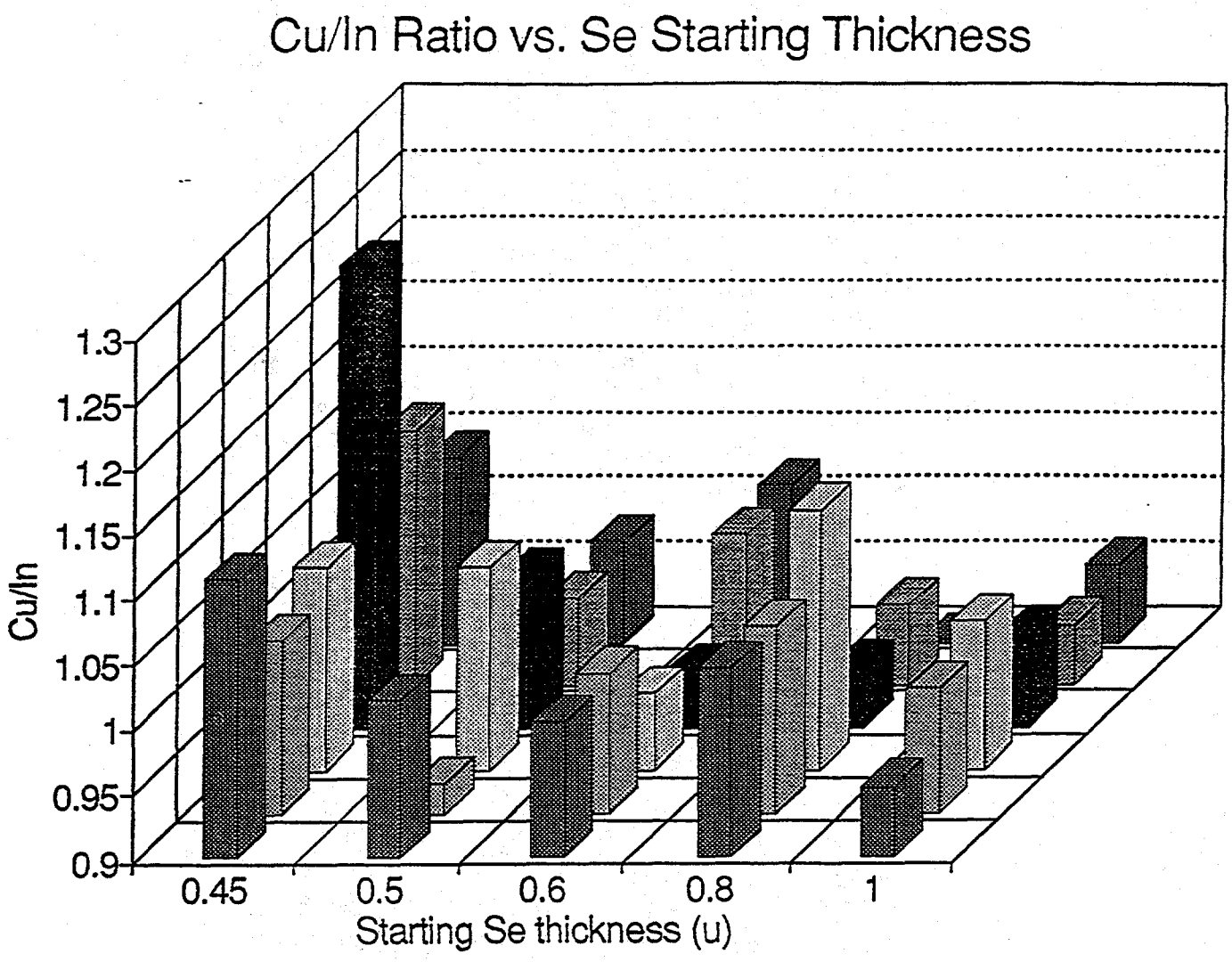

Figure 3-3 Copper to indium ratio in the CIS film as a function of starting Se thickness in the stack for 6 different heat treatment schedules.

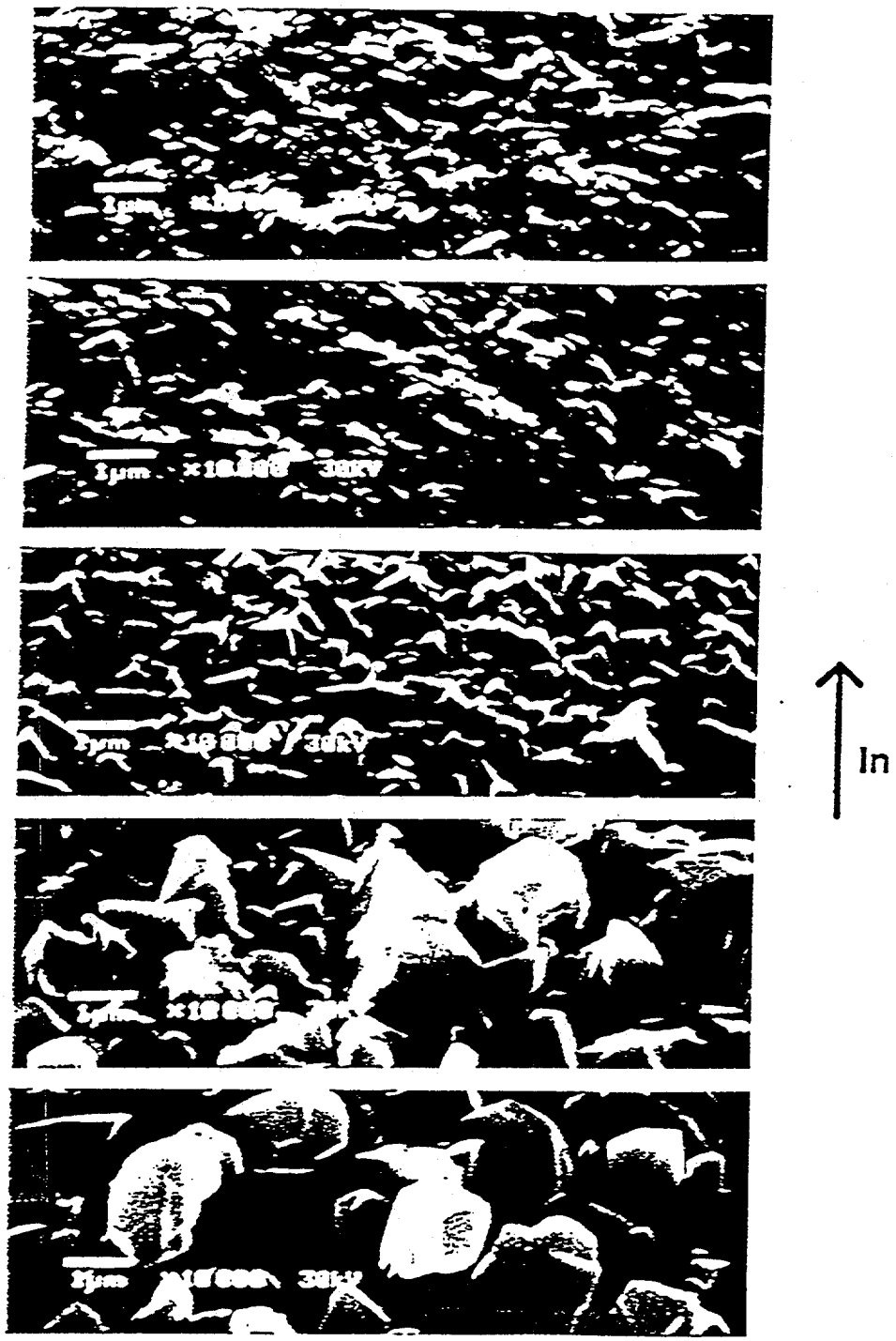

Figure 3-4 CIS grain size for films with different Cu/In ratios.

Figure 3-5 Large grain CIS deposited by EDCF.

Auger depth profile measurements have shown that the Cu, In and Se composition of the film is uniform throughout the thickness of the film as seen in **Figure 3-6**. The only impurity detected in these EDCF films was oxygen. X-ray diffraction data, shown in **Figure 3-7** indicate that these CIS films are typically chalcopyrite with 112 orientation. At least half of the samples studied with XRD show no peaks whatsoever which would indicate the presence of a second phase. Of the remaining samples, some of the minor peaks are identified with small amounts of a second phase. Other minor peaks do not have clear identification and are probably indicative of indium selenide, selenium or an oxide.

The above measurements can indicate that necessary, but not sufficient conditions have been met in a particular CIS film. Another shortcoming of the above measurements is their indirect relationship to the electronic properties of the film. The only measure of electronic film properties used routinely during this period was a quick test to determine the conductivity type of the majority carrier. Although the commercially available 'type-meter' used was designed for crystalline Si wafers and gave only a qualitative 'p', 'n' or null reading, it was reliable in terms of a quick screen for dead material.

The development of additional electronic measurements of CIS film quality has been initiated. The purpose is to identify parameters that are relate strongly to device behavior, yet are easily accessible through film measurement. One potentially useful measurement is that of dark conductivity vs. temperature, made through the film thickness and on the actual substrate used for device fabrication. **Figure 3.8** shows the dark conductivity vs. temperature of two CIS films. Obvious differences between these two films are apparent by the conductivity measurement, yet these same films are very similar by other measurement such as EDAX composition. Another electronic film measurement under development would directly assess carrier concentration in CIS on the conductive molybdenum substrate. More data should strengthen the correlation between electronic film properties and device behavior.

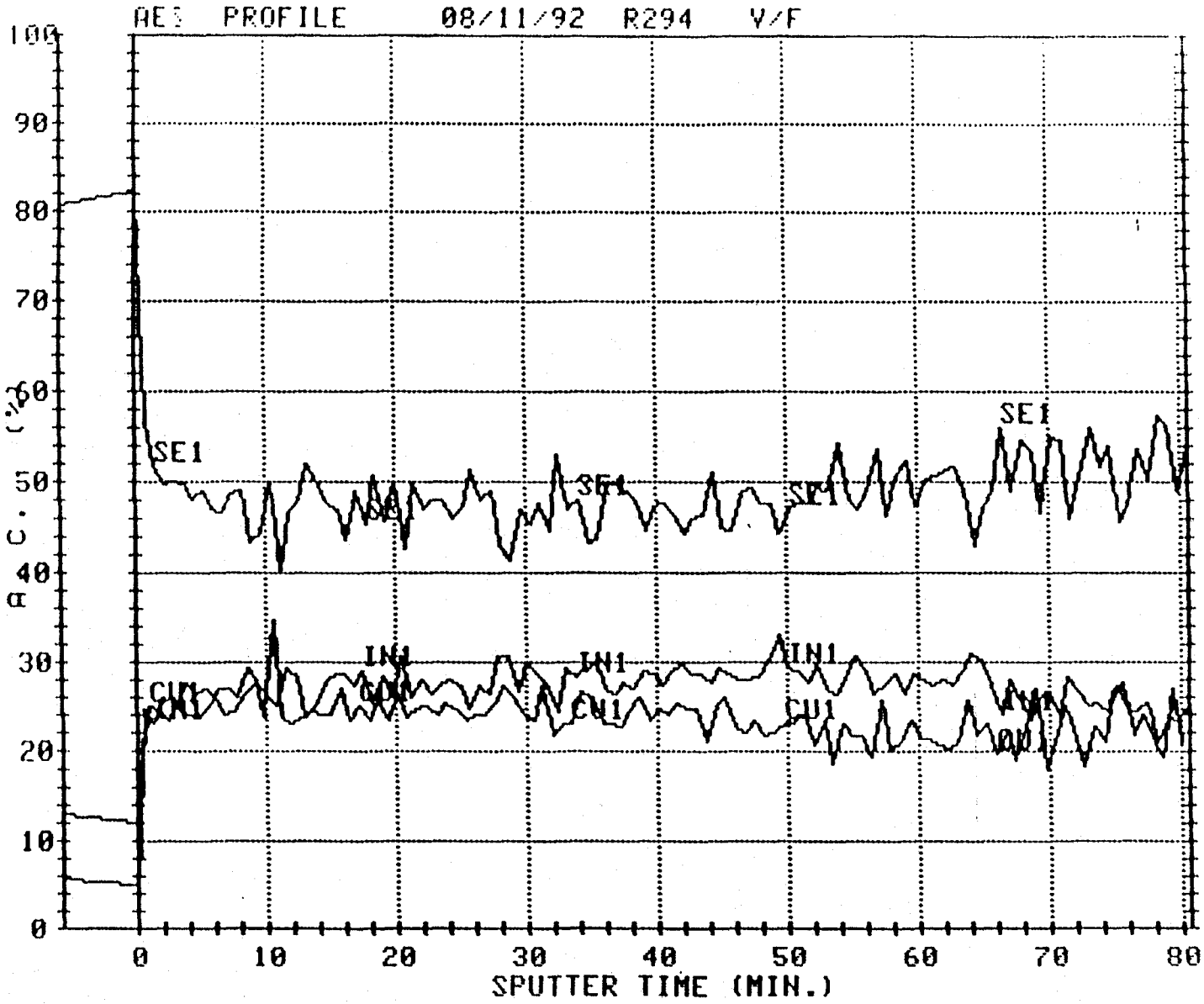

Figure 3-6 Auger depth profile showing uniform Cu, In and Se content.

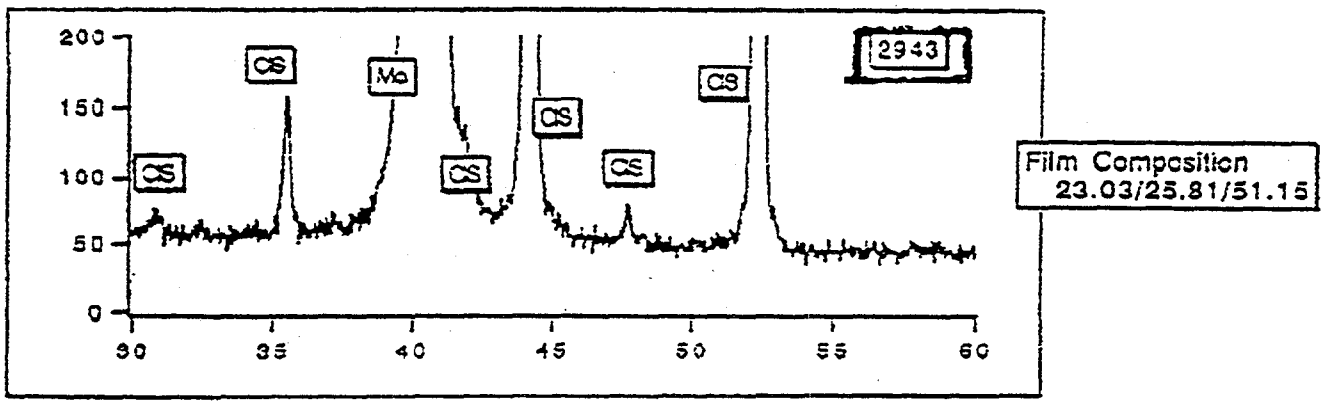

Figure 3-7 X-ray diffraction spectra showing only chalcopyrite peaks.

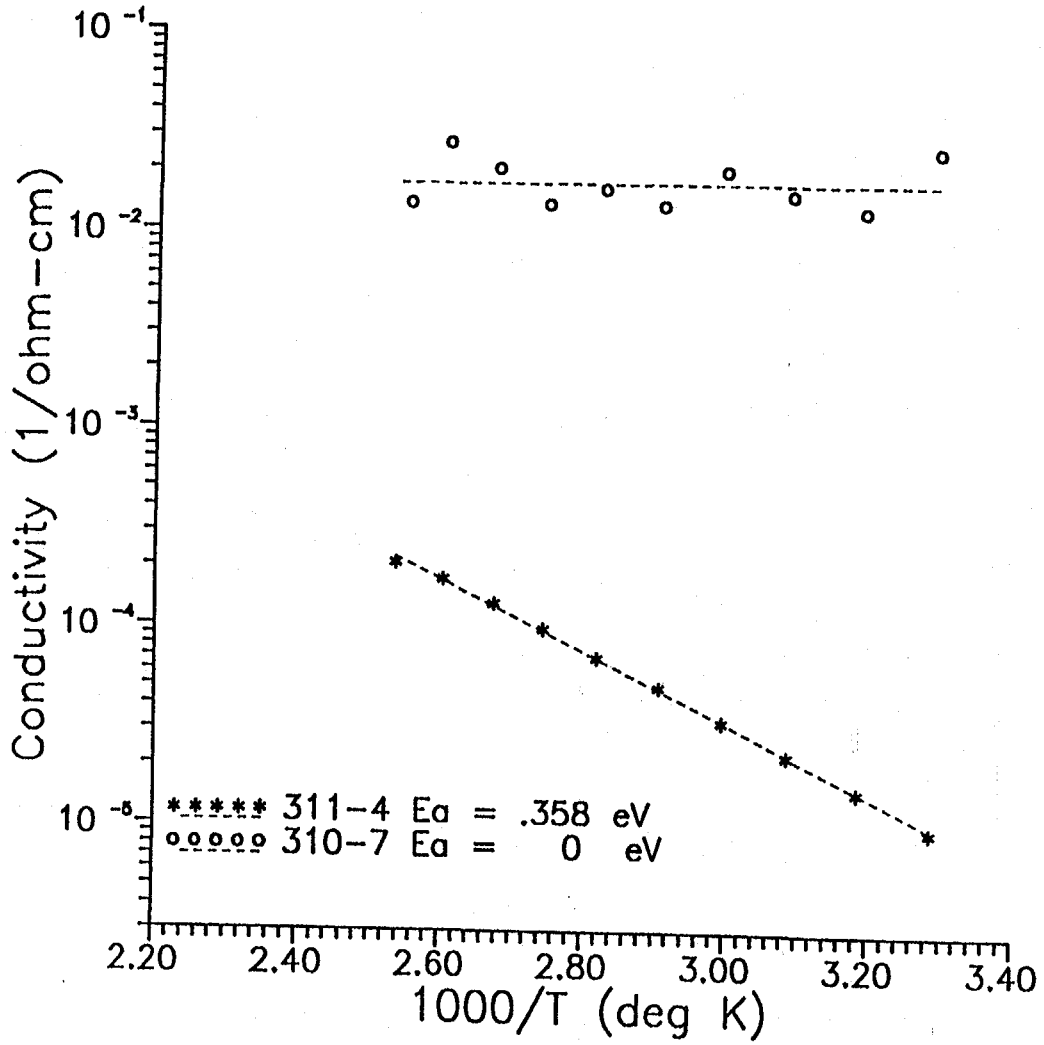

Figure 3-8 The dark conductivity of two p-type CIS films indicating a mid-gap Fermi level for one and degenerate conductivity for the other.

4.0 TASK III: DEVICE STRUCTURE

Solar cells have been fabricated on EDCF prepared CIS films with the following device structure

Light=>metal grid/ZnO/CdS/CIS/Mo/Glass

as shown in **Figure 4-1.** In this device structure, the window layer consists of two layers -thin CdS (~500Å) and ZnO (~8000Å). The CdS layer is deposited by chemical solution growth and the ZnO film is deposited by low pressure chemical vapor deposition (LPCVD). Both the processes have been described in Task 1. Devices are fabricated on 3" x 3" substrates. The individual devices are delineated by mechanical scribing. Optimization of CdS film thickness and ZnO deposition parameters have been carried out. **Figure 4-2** shows the effect of CdS thickness on the quantum efficiency of CIS devices with optimized ZnO layer. The CIS material used for this study was prepared at the Institute of Energy Conversion, Delaware. Short-circuit current densities above 40 mÅ/cm^2 have been demonstrated with our optimized window layers. The photovoltaic parameters of several solar cells fabricated on CIS prepared by EDCF are tabulated in **Table 4-1** A comparison of photovoltaic parameters of several solar cells measured at Solarex and at NREL are summarized in **Table 4-2**

During Phase II our best solar cell was fabricated by the EDCF method. The best solar cell had an active are conversion efficiency of 10.2% with the following parameters: Voc = 427 mV, Jsc = 37.41 mÅ/ cm^2 and FF = 0.641. The J-V characteristics and the corresponding quantum efficiency versus wavelength measurements of this device are shown in **Figures 4-3a** and **4-3b** respectively.

4.1 CIS Device Modeling

Computer simulation and device modeling of graded bandgap CIS solar cells done at Drexel University is included in Appendix A.

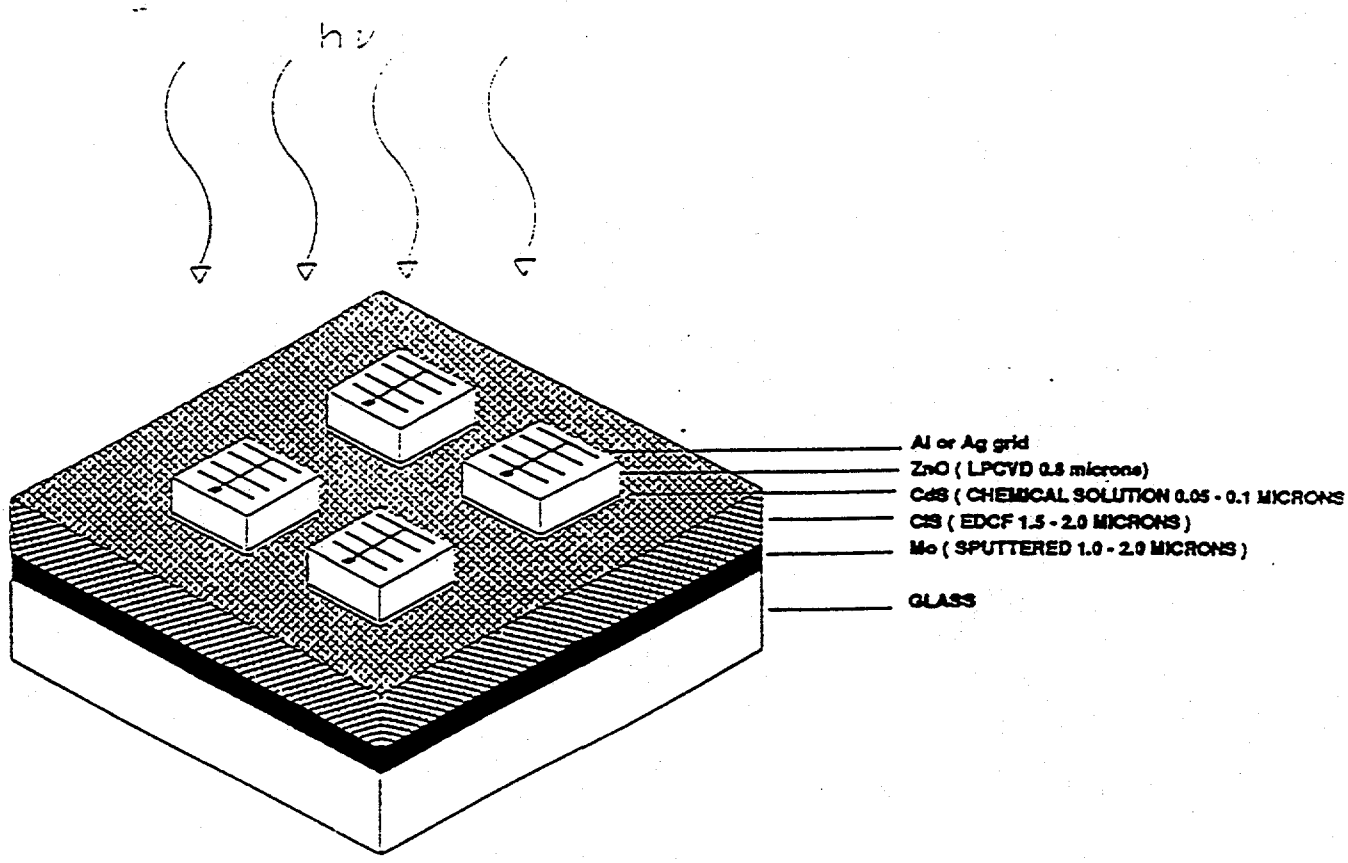

Figure 4-1 Device Structure.

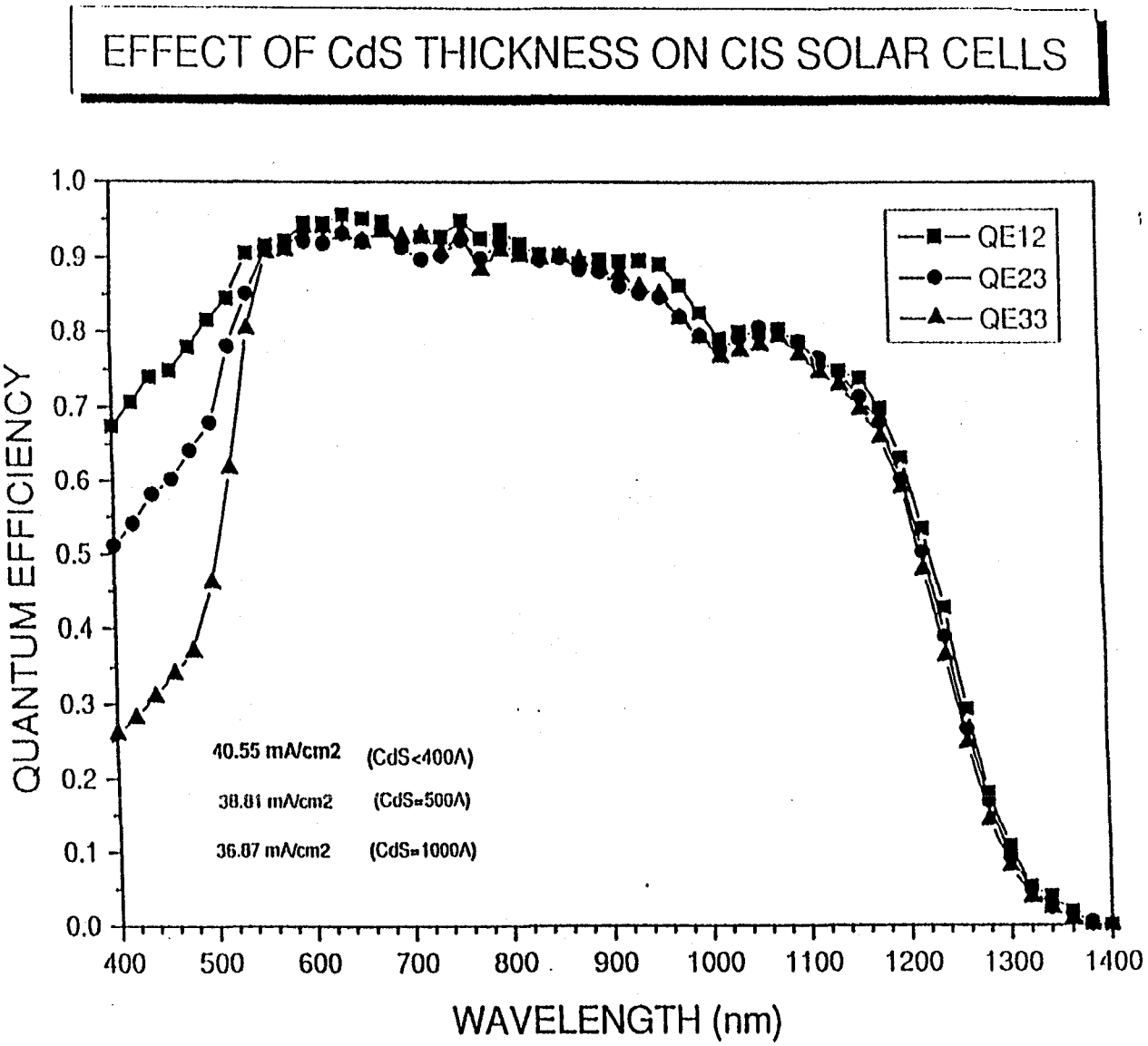

Figure 4-2 Effect of CdS Thickness on CIS Solar Cells.

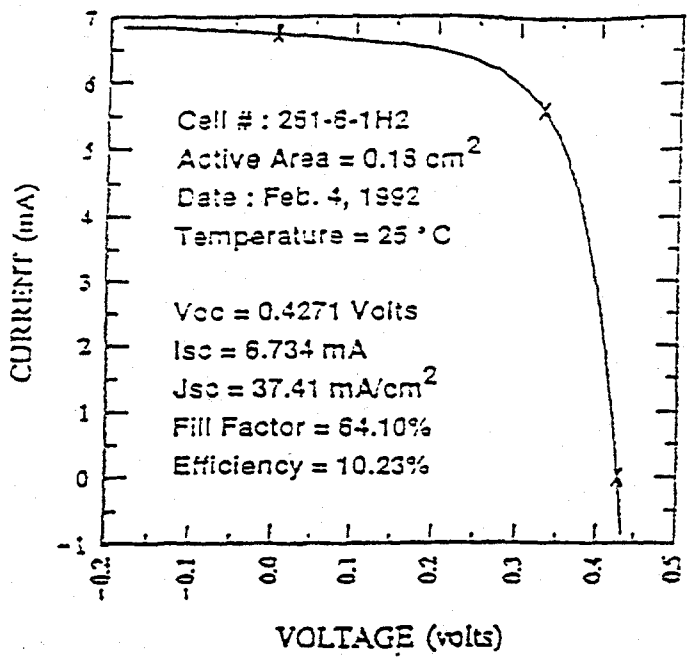

Figure 4-3a J-V characteristic of 10.2% efficient device.

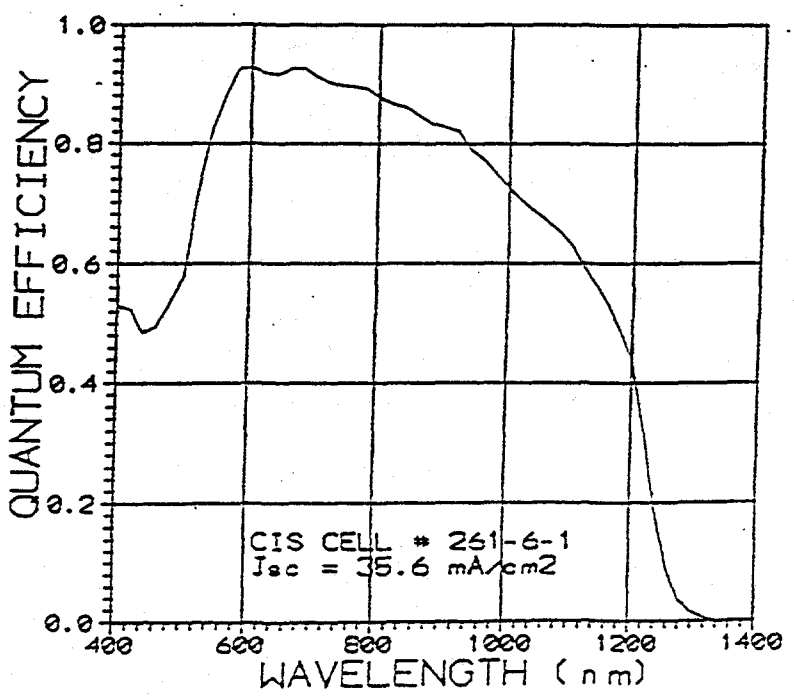

Figure 4-3b Quantum efficiency of 10.2% efficient device.

Table 4-1 Photovoltaic parameters of a number of solar cells fabricated on CIS prepared by the EDCF process.

Cell #	V_{oc}	J_{sc} (mV)	FF (mA/cm^2)	Efficiency (%) Active Area
256-5-3	347	35.6	.527	6.5
261-4-4	422	35.3	.600	9.0
261-4-2	400	35.7	.590	8.5
261-4-3	407	36.2	.620	9.2
261-6-1	418	32.7	.635	8.7
261-6-1	411	37.3	.609	9.3
261-6-1	430	34.3	.629	9.3
275-2	393	31.9	.487	6.1
275-6	422	33.1	.576	8.0
278-2	360	31.6	.539	6.1
279-1	361	35.4	.511	6.5
282-4-1	369	34.5	.528	6.7
282-4-2	366	32.6	.581	6.9
284-3-2	427	31.0	.485	6.4

Table 4-2 Comparison of solar cell measurements made at Solarex and at NREL

Cell #	V_{oc} (mV)	I_{sc} (mA)	J_{sc} mA/cm^2	FF	Effi-ciency (Active Area)	Total Area (cm^2)	Ac-tive Area (cm^2)	Measured At
261-6-1-H2	427	6.734	37.41	0.641	10.23	0.243		NREL
	430	6.168	34.30	0.629	9.30	0.245	0.18	SOLAREX
261-6-1-H1	410	9.260	38.10	0.624	9.75	0.312		NREL
	411	9.065	37.30	0.609	9.30	0.308	0.243	SOLAREX
261-6-1-L3	419	5.856	33.84	0.644	9.13	0.185		NREL
	418	5.655	32.70	0.635	8.70	0.191	0.173	SOLAREX
261-4-3-S3	416	7.090	35.47	0.610	9.00			NREL
	407	7.250	36.20	0.620	9.20	0.250	0.200	SOLAREX
261-4-2-S2	410	12.650	36.14	0.590	8.74	0.410	0.350	NREL
	400	12.500	35.70	0.590	8.47			SOLAREX
261-4-4-S4	422	11.800	34.70	0.580	8.49	0.410	0.340	NREL
	422	12.000	35.30	0.600	9.00			SOLAREX

5.0 TASK IV: SUBMODULE DESIGN AND ENCAPSULATION

Progress in CIS Integrated Modules at Solarex

The objective of the CIS module program at Solarex is to produce large area (>1000 cm^2) monolithic, interconnected high efficiency modules based on copper-indium diselenide as an absorber. In this program, preference is given to processes which are likely to be easily commercialized - those based on low cost that are easily scalable to large area and minimize inherent safety hazards. The elemental deposition and compound formation (EDCF) method incorporates these advantages, and has been used to fabricate all modules described in this section, unless otherwise denoted.

5.1 Solarex Module Design

The present CIS module structure used at Solarex is substrate/CIS/CdS/ZnO, with light incident on the top contact of ZnO. At present, a metallic grid on top of the ZnO is not used, thus avoiding the attendant loss due to shading and simplifying the fabrication. The voltage dropped laterally along the ZnO top contact is limited by forming narrow module segments which are serially interconnected. This approach also produces a level of voltage at the module output which is suitable for most PV applications. The serial interconnect between module segments is formed by interrupting (scribing) both the substrate contact, the absorber (CIS) and CdS layers, and the top (ZnO) contact sequentially at appropriate steps in the deposition. The scribes in the substrate and the ZnO electrically isolate the top and bottom segment contacts from the adjacent segment. The scribe through the absorber layer, with subsequent ZnO deposition, forms an interconnect between the top contact of one segment and the bottom contact of the adjacent segment, as shown in **Figure 5-1**. Presently, the substrate scribe is accomplished using a laser, and the interconnect and ZnO (top contact) scribe are done through mechanical means.

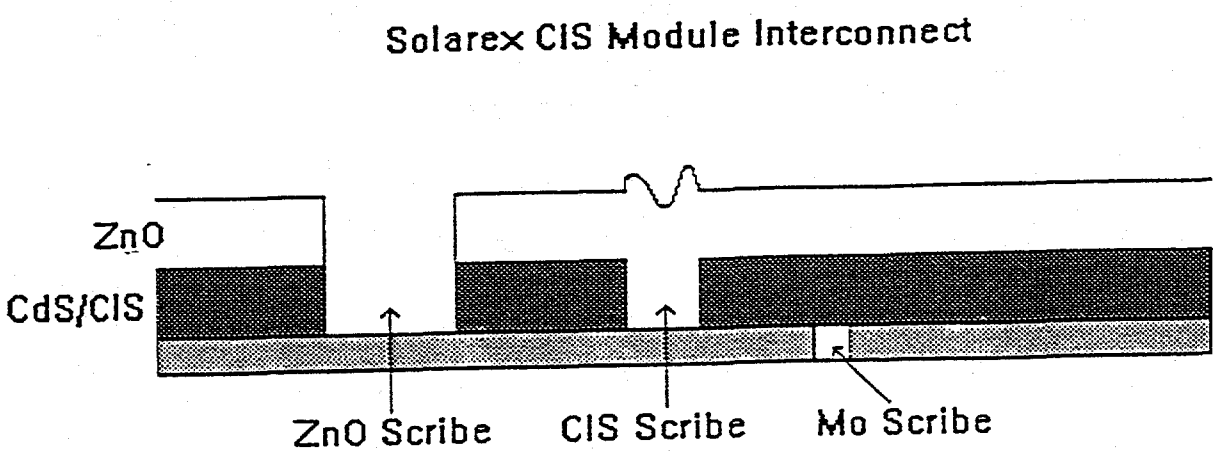

Figure 5-1 Diagram of segment interconnect scheme used at Solarex for CIS modules (not to scale).

5.2 Design Optimization

Several trade-offs exist which impact module design, including top contact resistivity and transparency, segment width, and total scribe width. Generally, the transparency of a conducting layer such as ZnO varies directly with its sheet resistivity, due to doping or thickness effects, as discussed in other sections of this report. Thus, it is not possible to obtain the most desirable situation-high transparency concurrent with low resistivity. However, once the top contact characteristics are optimized, for a top contact having a given sheet resistivity, the optimum segment width for a given total scribe width can be found. Two power loss mechanisms are under consideration: power lost due to lateral voltage drop along the top transparent contact, causing ohmic loss as well as incomplete carrier collection, and simple area loss due to the inactive area consumed under and between the top, bottom and interconnect scribes. The magnitude of these losses has been calculated, excepting the incomplete collection loss, by Gupta et al. Using this formulation and estimating the short circuit current density and total scribe width to be 38 mA/cm^2 and .018" respectively, an optimum segment width can be estimated to be in the region of .200", depending on top contact sheet resistivity (see **Figure 5-2**). The modules produced at Solarex to date are not completely optimized from this point of view. A segment width greater than optimum (0.300") was chosen to minimize the number of scribes and fabrication difficulty during the start-up phase of the CIS module program.

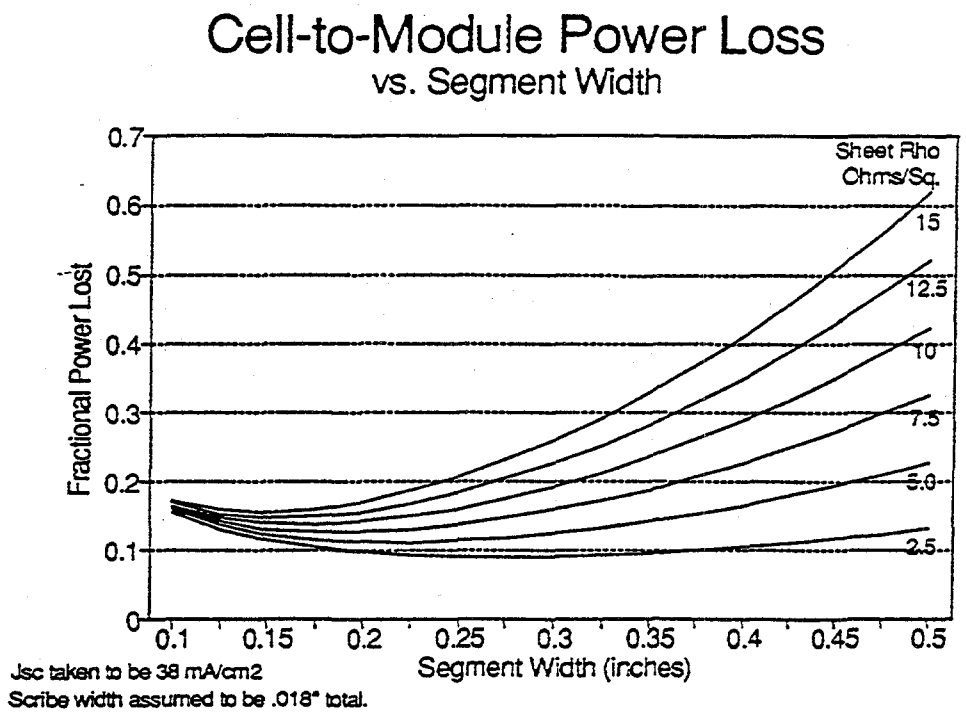

Figure 5-2 Estimated power loss as a function of segment width for various top contact sheet resistivity after Gupta et al (10).

5.3 CIS Scribing at Solarex

The substrate scribe is presently accomplished using a Nd:YAG laser with appropriate optics and translation mechanism. A mechanical scribing apparatus has been designed to create scribes in the absorber layer after CIS and CdS deposition and also in the ZnO and absorber layer after ZnO deposition, forming the interconnect and top contact scribes respectively. The mechanical scribing apparatus relies on undirectional movement of a fine blade using slight pressure during traverse across the module. An integrated CIS scribing station, having both the laser and mechanical scribing capability, is under construction at Solarex, depicted schematically in **Figure 5-3**. The substrate is translated in X-Y motion underneath either a laser beam or an adjacent mechanical scribing blade. The laser beam is actuated by a shutter, and the mechanical blades are actuated vertically on precision Z-axis slides as needed. Completion of this integrated CIS scribing station is expected by years end, and will facilitate CIS module fabrication with greater precision and reproducibility.

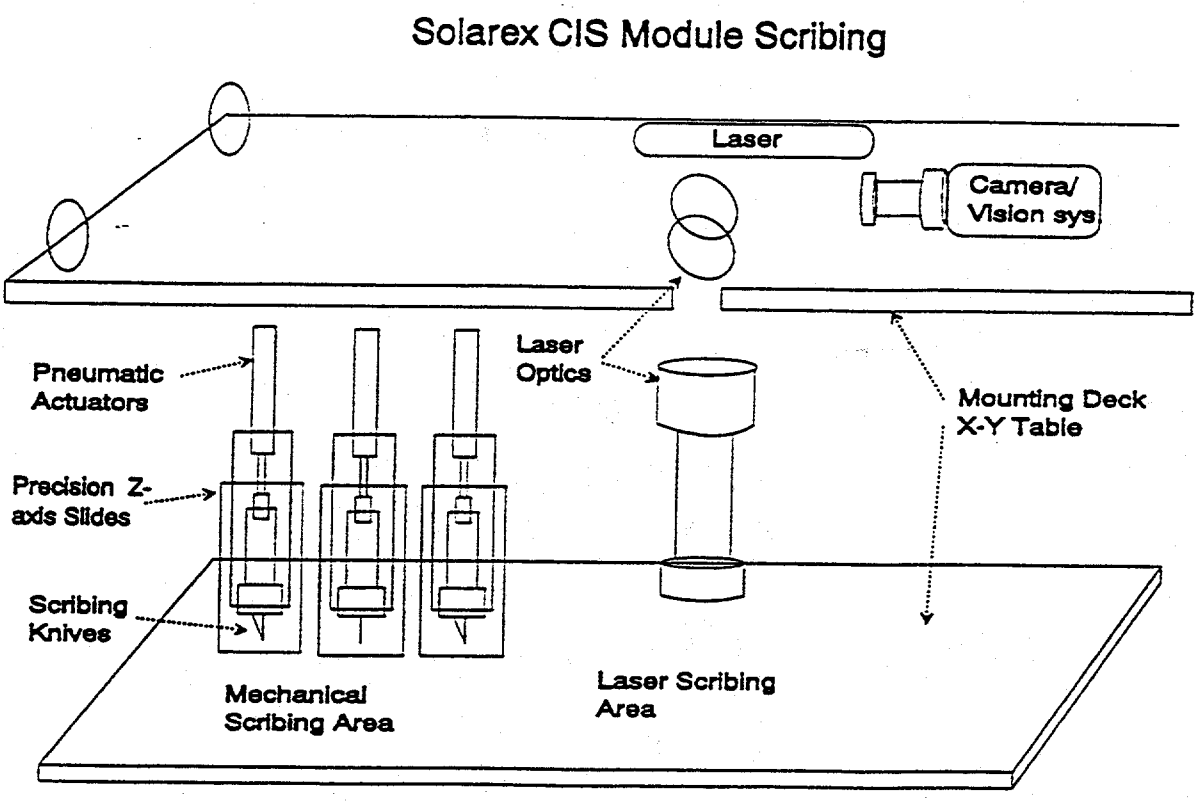

Figure 5-3 Diagram showing schematic placement of components for the Solarex integrated CIS scribing setup.

5.4 CIS Scribing Problems and Improvements

Initial efforts to laser scribe the substrate directly yielded poor results due to the extensive cracking, flaking and burning along the scribe edges. These defects occurred using a substrate of molybdenum on glass and resulted in malformations during later processing suspected of causing shorted or dead areas. This problem has been solved at Solarex by using a substrate consisting of glass/specular CTO/molybdenum. Laser scribing can be accomplished from the glass side of this substrate which yields very clean, uniform scribes. The interaction of the beam with this composite substrate is more favorable in terms of optical, mechanical and thermal aspects resulting in clean ablation without generation of debris or defects. A comparison of laser scribes on these two types of substrates is shown in **Figure 5-4**. All further module results described in this report refer to modules made using the glass/CTO/molybdenum substrate.

A micrograph of all three scribes, substrate, interconnect and top contact (right to left) is shown in **Figure 5-5**. The difference in width and uniformity of the three scribes is apparent, with the top contact scribe being the widest and most irregular. The jagged profile of the top contact scribe reflects the mechanical properties of the ZnO, a brittle material prone to fracture in large chips or platelets as the scribing tool is moved along the scribe. Fortunately, the interconnect and top contact scribes are done after CIS deposition, and have less propensity to cause shorting defects. However, the lost area due to scribe width and required scribe spacing under these conditions is undesirable.

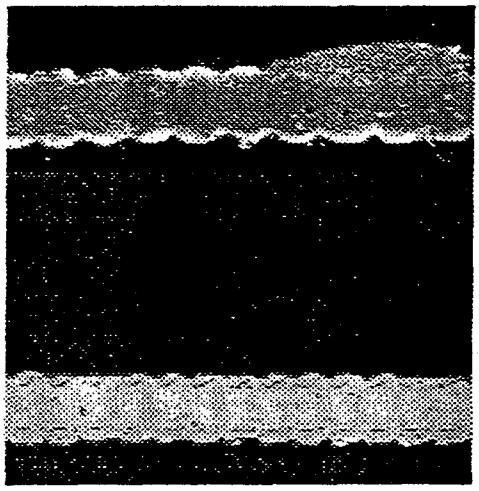

Figure 5-4 Laser scribe of glass/Mo (upper) shows cracking, burning and flaking compared to laser scribe of glass/CTO/Mo (lower).

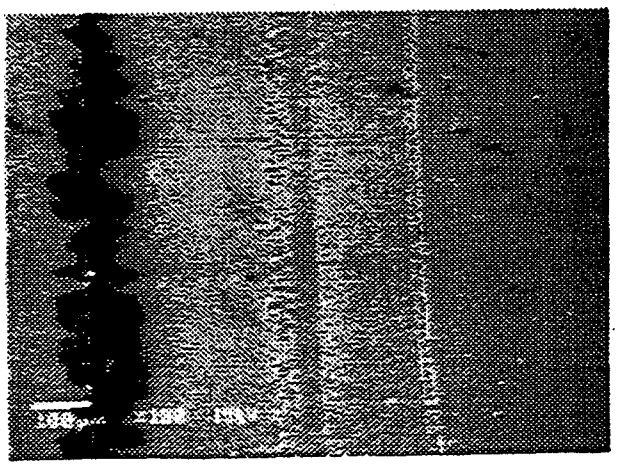

Figure 5-5 Scanning electron micrograph of mechanical ZnO top contact, interconnect, and laser substrate scribe (left to right) on CIS module structure.

One potential solution under current evaluation at Solarex is the use of an all-laser scribed system for CIS. In this case, the laser scribing must be accomplished from the top side of the module for the interconnect and top contact scribe, with the goal of selectively removing the absorber layer for the interconnect, and the ZnO and, optionally, the absorber layer for the top contact scribe. The substrate layers must not be disrupted, nor can conductive debris be generated which may bridge the top and substrate contacts in the area exposed by the scribe. We have had some success in preliminary trials of an all-laser scribed CIS system at Solarex, and we have, in fact, met the criteria above. A comparison of a top contact scribe on an actual CIS module is shown in **Figure 5-6** using first the mechanical system and then the new laser scribe. The improvement in area loss and uniformity is obvious. At present, it appears that the interconnect scribe can be accomplished without problem, however the laser scribing of the top contact is more difficult. The most common difficulty is incomplete separation of the top contact between adjacent segments. Further effort is planned to remedy this problem, since the scribe area loss could be substantially minimized using the smaller, more closely spaced laser scribes rather than the mechanical scribes.

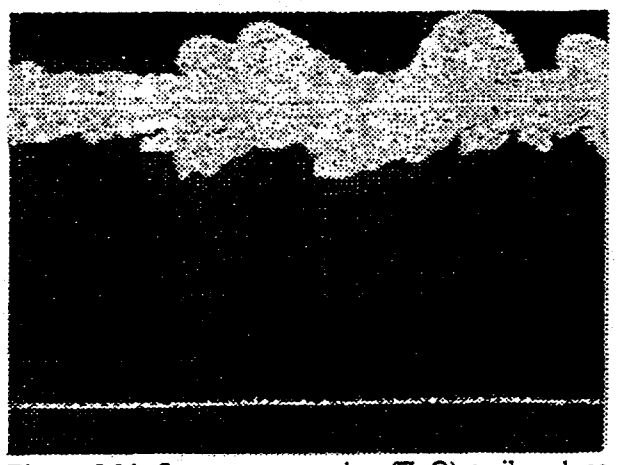

Figure M6 Segment separation (ZnO) scribes done mechanically vs. laser methods. Both scribes done on an actual module structure (glass/Mo/CIS/CdS/ZnO).

Figure 5-6 Segment separation (ZnO) scribes done mechanically vs. laser methods. Both scribes done on an actual module structure (glass/Mo/CIS/CdS/ZnO).

5.5 Module Development

Module development at Solarex has been approached two ways: the scale-up and test of necessary processes from small to large area and the fabrication of complete submodules whose size is determined by the most restrictive processing step. Most of the required process steps have been scaled up to allow CIS module fabrication of about 1000 cm^2 (12"x13") in size, including the elemental precursor deposition, CdS n-layer deposition and all scribing operation. Although ZnO deposition using the preferred LPCVD method is presently limited to 6"x6" area, sputtered ZnO of comparable quality is available for the 1000 cm^2 module process. The greatest size limitation presently exists in the CIS formation step due to spatial non-uniformities in heating and selenization of the 12"x13" substrate. **Figure 5-7** shows a CIS module having functional interconnected segments (25 segments, 6.02 volts Voc) which is 8"x8". Present effort is directed to the design and construction of CIS deposition and formation apparatus that will alleviate the size and uniformity limitations imposed by the existing equipment.

Figure 5-7 Photograph of an 8" x 8" CIS module produced at Solarex using the EDFC CIS deposition method.

Several submodules have been made at Solarex, with the IV characteristics of one of these early modules shown in **Figure 5-8**. Although several process steps are not optimized, the most

serious effect is due to a less than desirable control of CIS quality and uniformity, even for this 3"x3" submodule size. Again, this is one issue where improvement is expected to result from the construction of better CIS deposition and formation equipment, along with process improvements under study. Other submodules have been made using CIS obtained from the Institute of Energy Conversion at the University of Delaware. This CIS was produced by co-evaporation of copper, indium and selenium. All other module processing steps carried out at Solarex, including substrate formation, CdS and ZnO layer deposition and all scribing. A summary of submodules made this way is shown in **Figure 5-9**, with the IV characteristics of the best one shown in **Figure 5-10**. This submodule had an active area efficiency of 7.3%, and we expect improvement in this figure as we develop better controlled, more uniform CIS formation over larger areas. We also expect to derive improvement from development of improved scribing capability, optimization of module design (in terms of scribe and segment widths) and further optimization of CdS and ZnO window layers.

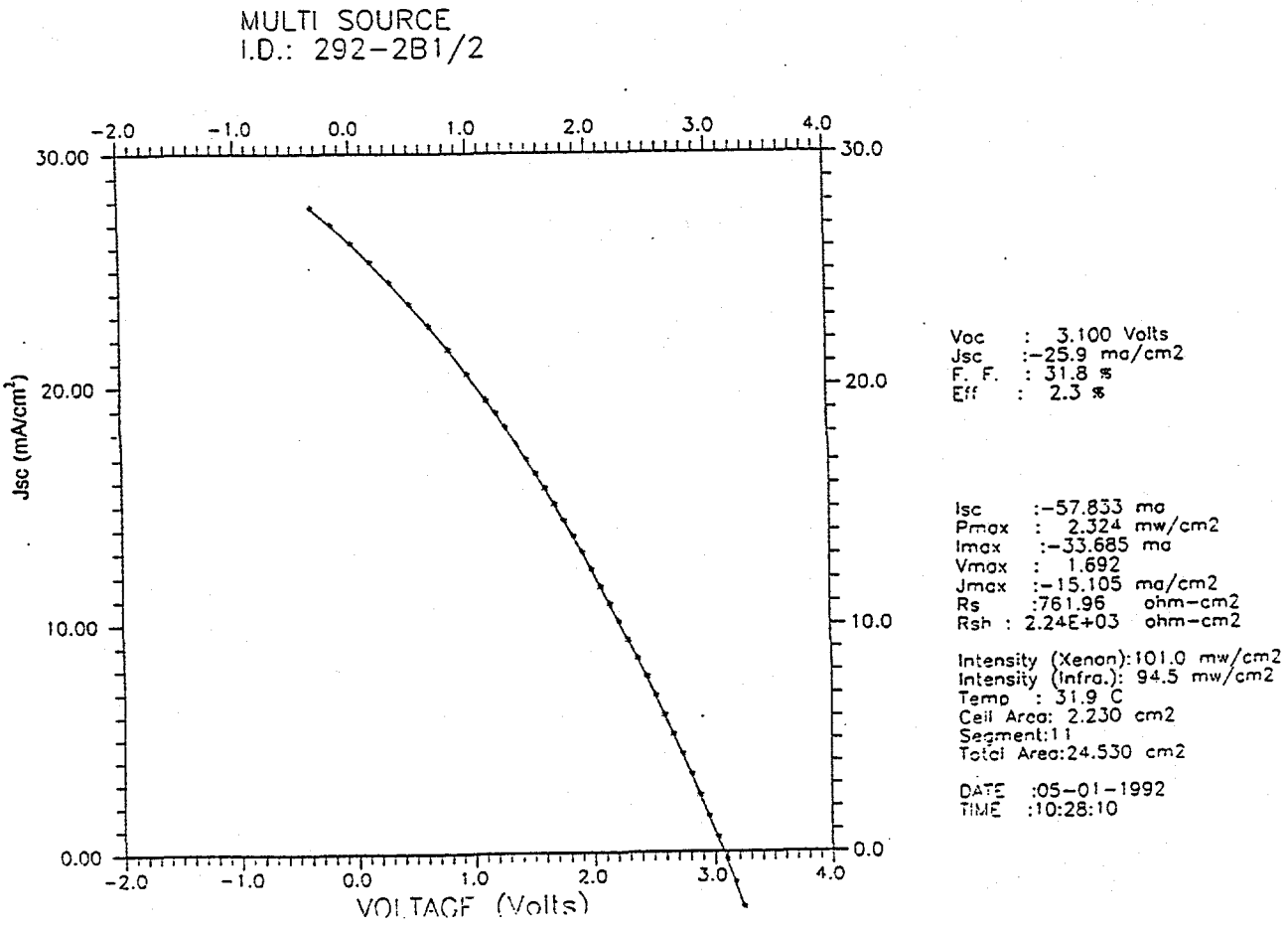

Figure 5-8 Current voltage characteristics of a CIS submodule using CIS made at Solarex using the EDCF process.

Submodules - Solarex CdS, ZnO, Scribing and Processing with EIC CuInSe2 (Area is approximately 25 cm^2)

Module ID	Voc (V)	Voc/seg (V)	Fill Factor (%)	Jsc (aperture) (mA/cm^2)	Jsc **(active)** (mA/cm^2)	Efficiency (aperture) (%)	Efficiency **(active)** (%)
32296	2.849	**0.356**	**38.4**	**30.7**	34.1	4.2	4.7
32297	2.244	**0.374**	**49.2**	**28.8**	32.0	5.3	5.9
32298	2.941	**0.368**	**53.6**	**29.3**	37.2	5.5	7.3
32299	0.345	**0.345**	**45.1**	**30.7**	33.7	4.8	5.3

Figure 5-9 Tabular results for CIS submodules made at Solarex using CIS supplied by the Institute of Energy Conversion

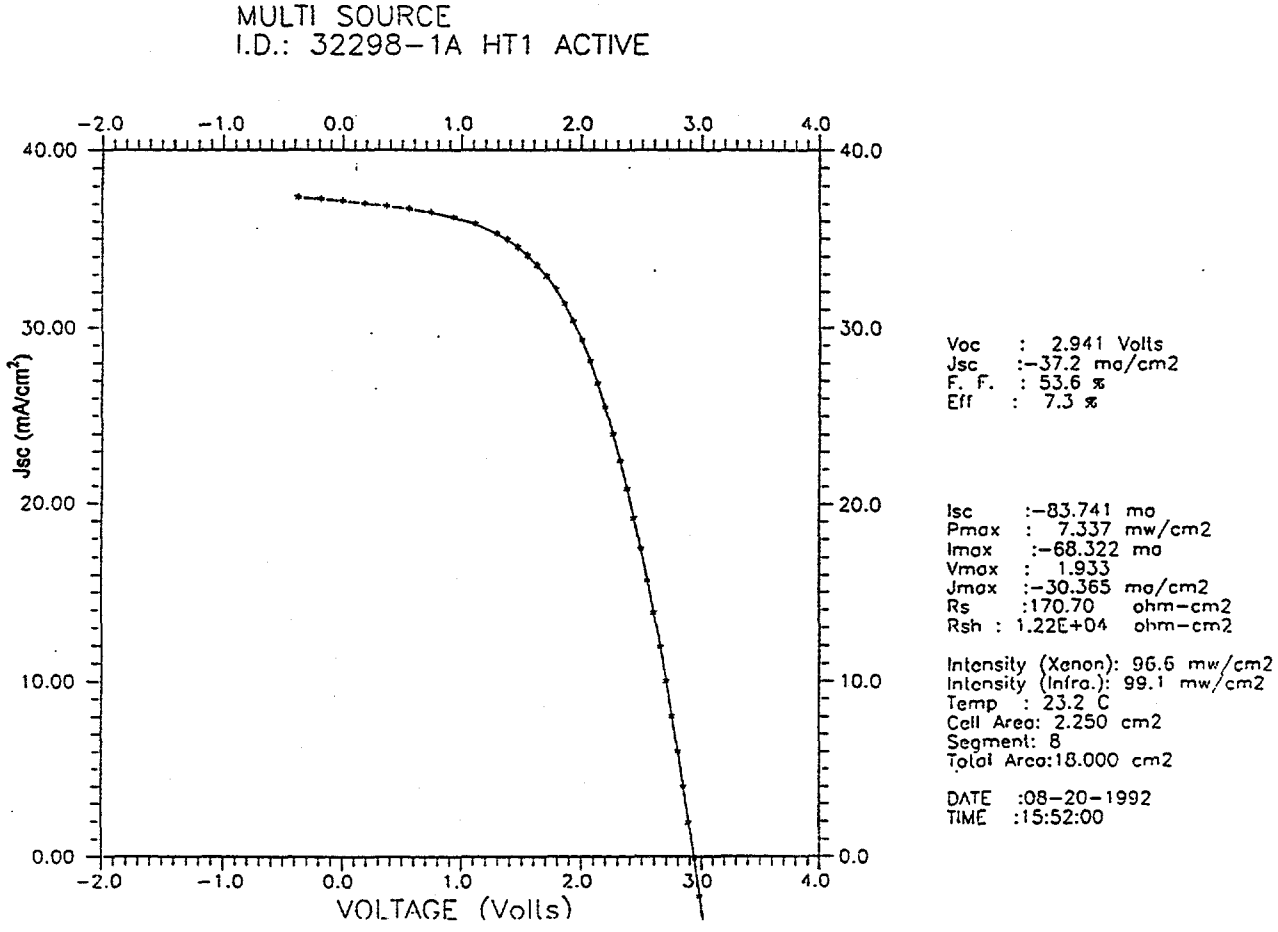

Figure 5-10 I-V characteristics of submodule made at Solarex using evaporated CIS (deposited at the Institute of Energy Conversion).

5.6 Study of Loss Mechanisms

Work in collaboration between Solarex and Dr. Thomas McMahon at NREL has begun to investigate loss mechanisms in CIS based cells using optical beam induced current (OBIC). This work is very preliminary, but does indicate the frequent presence of small areas of low performance on the surface of some CIS solar cells made at Solarex. The feature size of these areas of poor performance ranges about 50 microns. Current speculation as to causes include simple optical shadowing by surface objects, inhomogeneous current collection amplified by the large photon flux densities used in OBIC, inhomogeneous surface chemical composition at the junction or CdS layer, and effects related to poor back contact to the substrate in small areas. The latter effect is presently the focus of some investigation and may relate to sponge-like structures seen in SEM images of the substrate-CIS interface.

5.7 Large Area CIS Machine

We have been able to demonstrate all CIS module processes on 8" X 8" substrates although our present machine are only optimum for 3" X 3" substrates. Moreover, the two step process in CIS formation requires us to first deposit the elemental layers in one machine and then do the heat-treatment in another machine, thereby exposing the elemental stack to air.

In order to fabricate large area (>900cm^2) CIS modules we have designed and are assembling an integrated CIS machine. The schematic diagram of this machine is shown in **Figure 5-11.** The machine consists of a central hexagonal transfer chamber with five arms for different processes. We expect to complete the machine in three phases. In phase one, expected to be completed by June 1993, the Se deposition chamber and the compound formation chamber should be completed. In phase two, expected to be completed by December 1993, the Cu and In deposition chamber and the Mo chamber should be completed. This will then allow us to load glass substrates and complete the entire CIS film without exposing the substrate to air. In phase three, expected to be completed by June 1994, the ZnO deposition chamber and the CdS/ZnSe deposition will be completed.

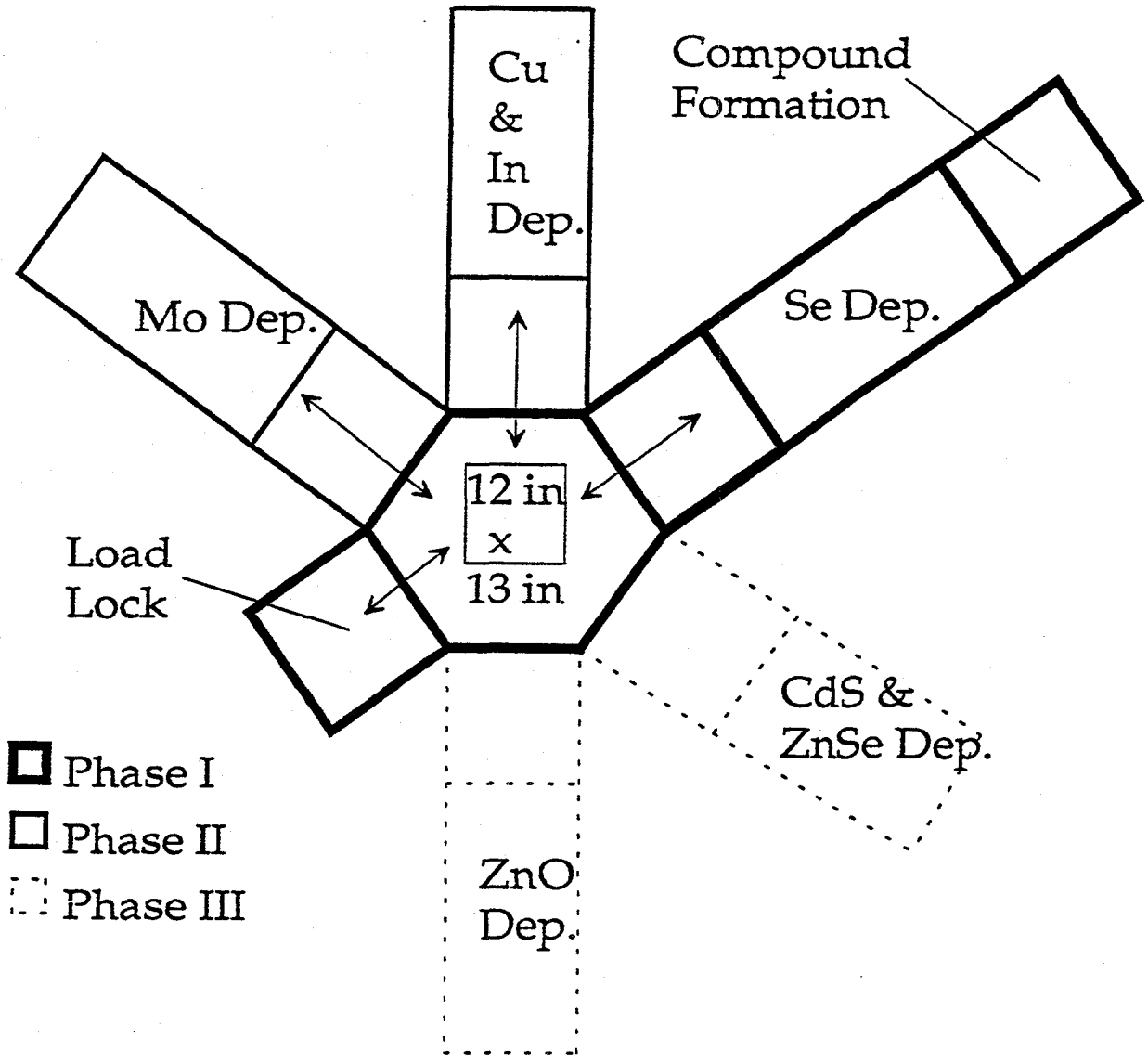

Figure 5-11 Schematic of Star System: Designed for large area deposition.

5.8 Conclusions

We have established all the elements needed for CIS module fabrication. The CIS material prepared by the ECDF has resulted in over 10% efficient small area devices. The module interconnect scheme with laser scribing of Mo substrate and mechanical scribing of CIS+CdS and of ZnO has been demonstrated. A small area submodule fabricated on IEC deposited CIS with all other Solarex processes has resulted in over 7% active area efficiency. The CIS preparation process is still inadequate in terms of reproducibility and scale-up. The large area CIS machine will allow us to address CIS material issues properly.

5.9 Future Work

In phase III we will concentrate our efforts on scaling-up all processes to area > 1000 cm^2. The CdS deposition and the ZnO deposition by LPCVD process will be scaled-up to 12" X 13" substrates. The CIS large area machine will be operational and will facilitate in preparation of CIS material on 12" X 13" substrates. The laser and the mechanical scribing will be integrated into one apparatus and the scribing apparatus automated.

6.0

COMPUTER SIMULATION AND MODELING OF THE GRADED BANDGAP $CuInSe_2$/CdS SOLAR CELL

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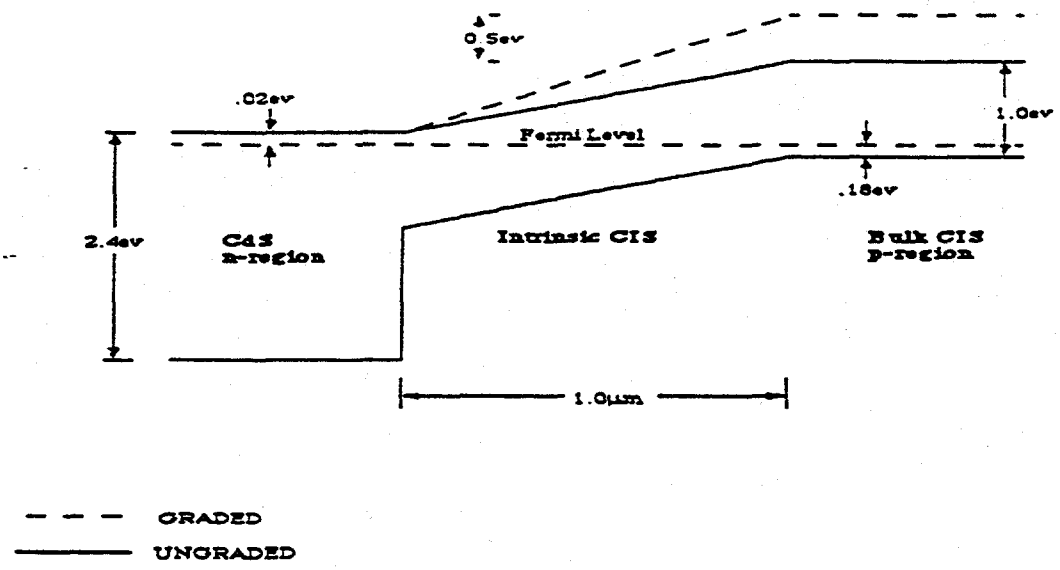
In the present simulation we assume a p-i-n model for the $CuInSe_2$/CdS solar cell, where the intrinsic region is the graded band gap CIS. Reflecting surfaces are provided at the p-i and n-i interface with reflection coefficients of 1.0 and 0.9 respectively. These help trap the light in the narrow intrinsic region for maximum generation of EHPs. Detailed simulation results show that graded bandgap approach can provide higher V_{OC} without sacrificing I_{SC} and FF.

Results are available for an intrinsic region which is graded from 1.0eV to 2.0 eV (in steps of 0.2eV) over a 1μm distance. Nearly 85% of the incident radiation can be absorbed in the intrinsic region (graded from 1.0 to 1.5eV) due to multiple reflections at the boundaries of the intrinsic region, compared to 95% in the case of uniform bandgap.A graded bandgap can be achieved by grading either the conduction or the valence band of the CIS absorber material. For grading in the conduction band only, it is observed that V_{OC} increases with the grading initially and soon saturates at 0.6V. I_{SC} decreases with the grading starting at 36mA/cm^2 and saturating at 28mA/cm^2. However the fill factor and efficiency increase with grading initially to reach a peak value and then decrease as the grading is increased further. The optimal values for V_{OC}, efficiency and fill factor are obtained when the conduction band is graded linearly from 1.0 to 1.4ev. The optimal cell had V_{OC}=0.6V efficiency=13% and FF=0.68 compared to 0.46V, 10.8% and 0.65 respectively for the ungraded cell.The values of current were based upon a thick CdS layer. Higher efficiency results when ZnO/CdS windows are used.

Encouraged by the promising preliminary results we plan to investigate the probable grading profiles in the conduction and the valence band which would not only give us the optimum values for the crucial cell performance factors but also be practically feasible. The simplest practically feasible case is to have a 1.0eV $CuInSe_2$ notch in an otherwise uniform bandgap 1.2eV $CuInS_2$ intrinsic region.Simulation results show that V_{OC} has strong dependence on the width and the position of the low bandgap notch.

The simulations were carried out using analytic forms for the light and dark currents, with the grading simulated by small regions each with a constant bandgap. The finite element approach matched carrier densities and currents at each interface between elements. The 1μm graded region was broken into 60 regions for the calculations. The equations, assumptions and results are given below.

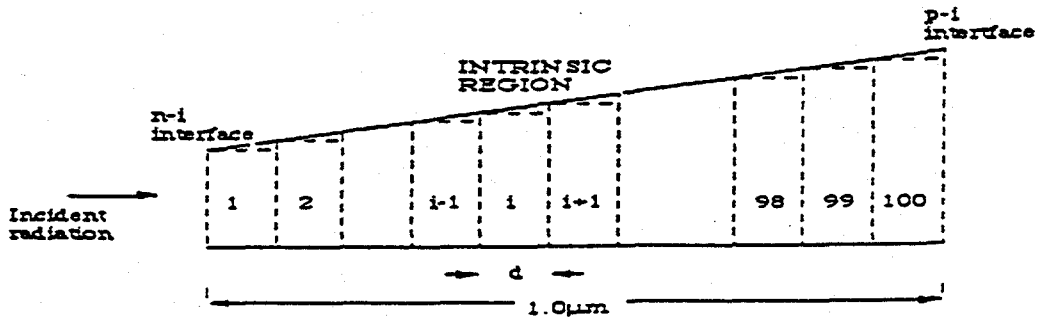
CELL STRUCTURE



p-i-n Solar Cell Structure

* p-i-n Model: n-type CdS,
  p-type CIS,
  i-type graded bandgap CIS
* Reflecting surfaces at p-i and n-i interfaces with reflection coeff. of 1.0 and .9 respectively.

OPTICAL MODEL



UNIFORM BANDGAP FINITE ELEMENT APPROX. FOR GRADED BANDGAP i-REGION

* Incident radiation is assumed to undergo multiple reflections at the p-i and n-i interfaces. This assures complete absorption in CIS.

* Absorption coeff. in the graded region is modeled using the following relation for a direct bandgap semiconductor:

$$\alpha(x)=A_D[h\vartheta - Eg(x)]^{1/2}$$

* Numerical model based on finite element approach is used to determine electron & hole carrier distribution in the graded i-region.

* Graded i-region is broken into infinitesimally small uniform bandgap regions. For each of these we can find carrier density by solving transport equation in conjunction with Poisson and continuity equation.

* Electron & hole carrier density and their derivative are continuous in the i-region. Hence we have a set of following boundary conditions:

$$\Delta n_i(d)=\Delta n_{i+1}(0)$$

$$\Delta p_i(d)=\Delta p_{i+1}(0)$$

.....1

$$\left|\frac{\partial \Delta n_i}{\partial x}\right|_{x_i=d} = \left|\frac{\partial \Delta n_{i+1}}{\partial x}\right|_{x_{i+1}=0}$$

$$\left|\frac{\partial \Delta p_i}{\partial x}\right|_{x_i=d} = \left|\frac{\partial \Delta p_{i+1}}{\partial x}\right|_{x_{i+1}=0}$$

.....2

$\Delta n=\Delta p=0$ @ n-i and p-i interface

.....3

*Boundary conditions 1-3 give a set of simultaneous equations which are solved numerically by Gauss Elimination method to give the carrier distribution in the graded i-region.

DARK MODEL

* The dark current is obtained by integrating the recombination in the intrinsic region over the width of the region, using Shockley-Hall-Read recombination.

$$j_D=q\int_0^W \frac{n(x)p(x) - n_i(x)^2}{\tau(n(x) + p(x) + 2n_i(x))}\,dx$$

* Grading profile Eg(x) for a linearly graded region is given by the following equation, where Eg(0) is the starting bandgap:

$$Eg(x)=Eg(0) + \beta x$$

* Carrier distributions are given by the following equation:

$$n_i(x) = (N_cN_v)^{\frac{1}{2}}\exp[-Eg(x)/2KT]$$
$$n(x) = N_c\exp[(E_{Fn}-E_c(x))/KT]$$
$$p(x) = N_v\exp[(E_v(x)-E_{Fp})/KT]$$

RESULTS

Linearly Graded Intrinsic Region:

* Intrinsic region is graded from 1.0 to 2.0eV (in steps of 0.2eV) over a 1.0μm distance.

* Simulation results show that 85% of the light can be absorbed due to multiple reflections at the p-i & n-i interface in 1.0 to 1.5eV graded case compared to 95% in the 1.0eV ungraded case.

* Following results are for grading present only in the conduction band.

* There is a substantial improvement in the cell performance factors for the graded structure compared to the uniform bandgap structure (Fig.1b).

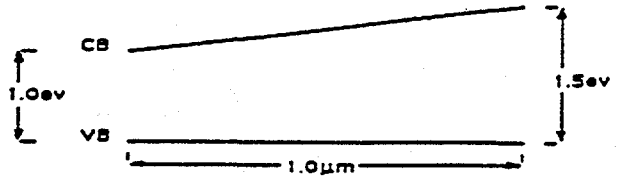


Fig.1(a) Linearly graded intrinsic region.

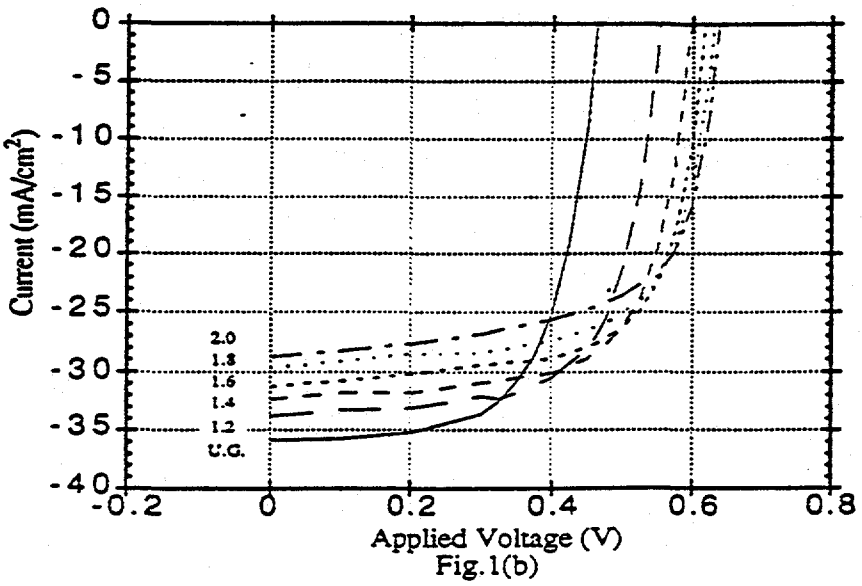


Fig.1(b)

* Fig. 1(c-f) show how the cell performance factors change when grading is increased from ungraded case to 2.0eV in steps of 0.2eV. It can be inferred from the graphs that the V_{oc} and I_{sc} saturate for higher grading profiles. However the efficiency and fill factor show a peak at 1.4eV. Thus the optimal graded cell is obtained with a grading profile of 1.0 to 1.4eV with V_{oc} of 0.6V, Isc of 28mA, efficiency of 13% and fill factor of .68. On the other hand ungraded cell had a V_{oc} of 0.46V, efficiency of 10.8% and fill factor of 0.65.

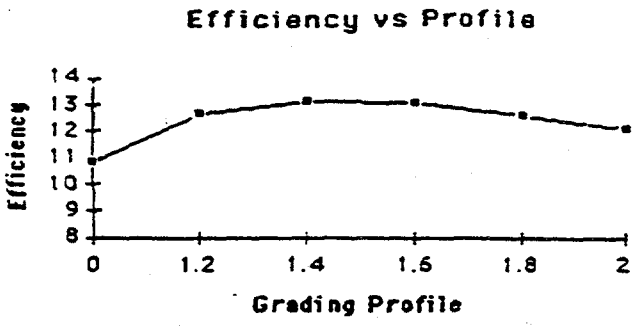


Fig. 1(c)

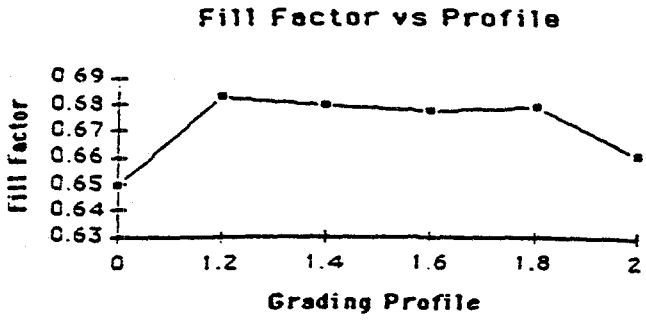


Fig.1(d)

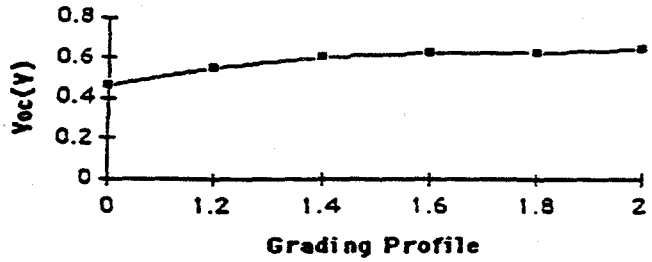


Fig.1(e)

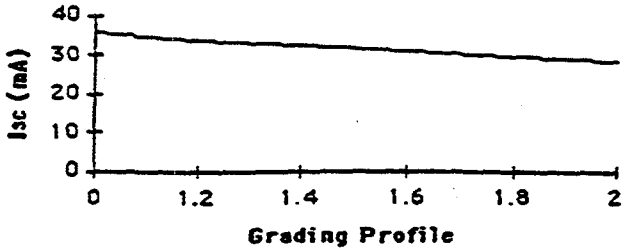


Fig.1(f)

Intrinsic region with a graded notch:

* 1.0eV notch is present in the valence band of a 1.2eV uniform bandgap intrinsic region (Fig.2a).

* Such a structure is practically feasible by depositing a 1.0eV $CuInSe_2$ notch in a 1.2eV $CuInS_2$ intrinsic region.

* V_{OC} for such a structure shows a strong dependence on the position 'd' of the low bandgap notch (Fig.2a).

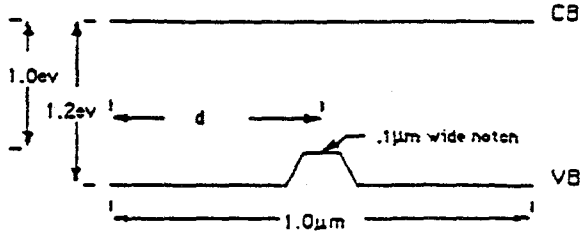


Fig.2(a) Intrinsic region with a graded notch.

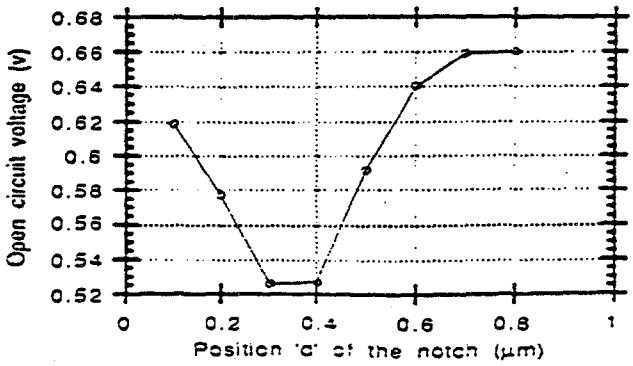


Fig.2(b)

FUTURE WORK

* Different grading profiles will be tried to obtain an optimal cell configuration.

* These grading profiles can be realized practically by replacing In and Se by Ga and S respectively.

* How Ga and S change the conduction and valence bands will be determined by calculating the band structure of the materials, using available models that include the effects of the d-levels in the atoms.

CONCLUSION

The notch approach and the graded bandgap both appear to be capable of yielding higher open circuit voltage and efficiency than the ungraded CIS cell. An optimal structure has not been identified yet.

IEC Interaction and Participation

During this phase we interacted strongly with The Institute of Energy Conversion, Delaware in the following areas:

1. IEC supplied glass/Mo substrates with CIS deposited by thermal evaporation as standard cells which we used for optimization of CdS deposition and optimization of ZnO deposition. This optimization led to demonstration of over 40 mA/cm^2 short-circuit current density.

2. IEC supplied EDX standard for CIS which we used for film composition measurements at Solarex.

3. IEC performed materials characterization, such as, XRD and EDX on Solarex deposited Cu-In films and on CIS material.

4. IEC fabricated and measured several CIS solar cells on Solarex deposited CIS material. This helped us establish our device fabrication processes.

5. IEC deposited CIS films on Solarex's scribed Mo substrates. This helped us establish the scribing and interconnect parameters. It led to the demonstration of 7% active area small CIS submodule.

6. Above all, we had regular technical discussions and consultation on many aspects of CIS solar cell processing with IEC personnel.

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(G)

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14.

15. Supplementary Notes

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16. Abstract (Limit: 200 words)

This report describes a 3-year, cost-shared research program at Solarex to develop all pertinent processes and technologies required to achieve the goal of 12% CIS submodule (with areas > 900 cm^2). The work is focused on four tasks: (1) window layers, contacts, substrate; (2) CIS absorber layer; (3) device structure; and (4) submodule design and encapsulation. Each task addresses (1) basic material improvements, (2) fabrication and characterization of CIS solar cells, and (3) scale up of processes to large-area substrates.

17. Document Analysis

a. Descriptors

thin films ; submodules ; copper indium diselenide ; materials ; photovoltaics ; solar cells

b. Identifiers/Open-Ended Terms

c. UC Categories

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18. Availability Statement

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