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PV Cz Silicon Manufacturing Technology Improvements

Annual Subcontract Report 1 April 1992 – 31 March 1993

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PREFACE

Siemens Solar Industries (SSI) began a three-year, three-phase cost shared contract in March 1992 to demonstrate significant cost reductions and improvements in manufacturing technology. The work has focused on near-term projects for implementation in the SSI Czochralski (Cz) manufacturing facility in Camarillo, California.

The work has been undertaken to increase the commercial viability and volume of photovoltaic manufacturing by evaluating the most significant cost categories and then lowering the cost of each item through experimentation, materials refinement, and better industrial engineering.

The initial phase of the program has concentrated in the areas of crystal growth, wafer technology and environmental, safety and health issues.

Significant contributions have been made by the key personnel involved in the program. They include Jerry Anderson and David Tanner in module and cell evaluations, Kim Mitchell and Karen Pauls in the crystal growth and wafer areas, and Sergio Vasquez in the environmental, safety and health area.

SUMMARY

OBJECTIVES

The objective of the program is to reduce costs in photovoltaic manufacturing by approximately 10% per year. The specific milestones are shown in Table 1. The program consists of three focused tasks relating to cost reduction. The silicon wafer itself contributes about half of the total module cost and has the most potential for cost reduction. The cell processing costs are about a quarter of the module costs, with cell efficiency results being most important. Module assembly and packaging costs are the balance, with the module design, both materials and labor, contributing significantly.

Table 1. Cz manufacturing technology milestones.

	Phase 1	Phase 2	Phase 3
Task 1. Silicon Crystal Growth & Thin Wafer Technology			
A. Increase Cz grower productivity by 25%	10%	15%	25%
B. Demonstrate utility of prototype wire saw Deliver 100 wire sawn wafers	• •		
C. Demonstrate 0.010"-thick wire sawn wafers Deliver 100 0.010" wafers		• •	
D. Reduce wafer cost by 30%		15%	30%
Task 2. Silicon Cell Processing Reduce cell cost by 30% ($/watt)	10%	20%	30%
Task 3. Silicon Module Fabrication & Environmental, Safety & Health Issues			
A. Reduce module fabrication costs by 35% Deliver modules demonstrating reduced $/watt	10%	25% 2 modules (20%)	35% 6 modules (25%)
B. Reduce caustic use and waste	Define process and equipment	25% reduction	
C. Replace CFC's	Evaluate CFC alternatives		90% reduction in CFC usage

Task 1: Silicon Crystal Growth and Thin Wafer Technology. Crystal growing costs are driven by material growing yields and indirect manufacturing costs such as electricity and machine parts used each time a crystal ingot is fabricated. Wafering costs are driven by labor and the number of good slices yielded per length of crystal processed. This first task of reducing the wafer costs has focused on the graphite usage in the crystal growing machines, the polysilicon material used for ingot growth, and the evaluation of wire saw machines to improve the yielded wafers per inch of ingot.

Task 2: Silicon Cell Processing. Cell processing costs are driven by the electrical contacts used, and the labor required for the process steps to clean the wafer, form the semiconductor junction, and the contacts. The second task has been focused on the improvement of the etching bath process for better uniformity, better junction formation, and reduced contact resistance. Studies of process automation for lower labor costs have begun.

Task 3: Silicon Module Fabrication and Environmental, Safety, and Health Issues. Module costs are highly sensitive to labor and materials. The module design tasks are driven by high reliability in the field and lower costs. Included in this task is the environmental work to eliminate chlorofluorocarbon (CFC) usage and significantly reduce the caustic waste volumes.

DISCUSSION AND CONCLUSIONS

During this year, several significant manufacturing technology improvements were achieved.

The crystal growing operation improved significantly with a complete redesign of the graphite hot zone parts. This redesign improved the lifetime of these expensive machine parts by more than a factor of three and has resulted in a savings of over $300,000 annually. This design effort is complete and all the crystal growers at SSI have been retro-fitted to include these parts. Crystal growing improvements were also achieved by an on-going study of the polysilicon materials used versus crystal yield. A three-month study of various polysilicon remelt runs versus runs with virgin polysilicon chips mixed in was conducted. Higher resistivity polysilicon remelt alone shows much higher growing yields, which is believed to be due to the higher state of refinement. This benefit is two-fold, with remelt polysilicon typically much less expensive than the virgin material.

Wafer processing with wire saws progressed rapidly. The wire saws have proven to yield 30% more wafers per inch in production. The capacity of a wire saw is much greater than that of an ID saw, resulting in major labor savings for a given manufacturing throughput. The major trade-off with wire saws is an increase in the cost of the slurry cutting media. The process continues to be optimized through development under this contract.

Cell processing improvements have included the implementation of a new etching process with better uniformity across the wafer surface, and process variations in junction formation and optics versus cell and module performance. A significant result during this study was the quantification of the sensitivity of certain diffusion processes to humidity exposure. This finding led to implementation of an additional etch step for thorough cleaning of the cell surface prior to contact firing. Improved electrical performance of the complete production volume has been achieved under Phase I of this contract.

Module designs for lower material and labor costs have begun with the focus on a new junction box and less costly framing technique. CFC usage has been eliminated in the SSI manufacturing facility under this contract. Studies of methods to reduce caustic and fluoride waste have begun.

SECTION 1.0
CRYSTAL GROWTH AND THIN WAFER TECHNOLOGY

The Crystal Growing Operation in Camarillo increased throughput by 8% over the previous year's value. The increase is attributable to several factors including improved poly quality and cleaning, upgrades to the growing equipment, specifically diameter controls, and upgrades to the hotzone parts which have increased reliability and reduced cycle time. The throughput in Vancouver was unchanged due to an emphasis on developing a recharge process.

1.1 Polysilicon Study:

A wide range of poly silicon starting materials have been evaluated. Crystal Growing yields, cell performance and impurity analysis have been conducted. Overall crystal growing yields improved by 4% as a result of the study.

1000 kg of Semi-Prime virgin poly material was purchased and run through the normal crystal growing process. In Figure 1-1. the yields for the 30 experimental crystal growth runs are compared to the baseline process. Though the Semi-Prime material improved yields, the yield improvement observed was not able to justify the added cost of the Semi-Prime virgin material.

Ethyl poly "beads" were investigated. The cost of Ethyl's standard product is too high to be cost effective for our current process. Though Ethyl sells reject material at a suitable cost, the quantities of this material are limited and cannot be guaranteed.

Remelt from outside sources was investigated. As shown in Figure 1-2., the resistivity of the starting material plays a role in the quality of the grown ingot and has a direct affect on the crystal growing yield. Through this study it was determined that 1-3 Ohm-cm, n-type material consistently produced the lowest crystal growing yields. This material must be heavily counter doped in order to grow 1-2 Ohm p-type material. In comparison, remelt material which is >10 Ohm-cm, n or p-type, repeatedly produces the highest yields for remelt material purchased from outside vendors.

SSI uses inhouse remelt material as feed stock for ingot growth. Inhouse remelt used includes tops, tails, slabs and selected plugs, those which are not suspected of containing quartz chips or other foreign material. Historically, the yields obtained using the slab material were low, believed caused by the heavy oxide buildup on the sides of the ingot. During 1991, use of slab material was stopped until a cost effective method of cleaning the slabs could be found.

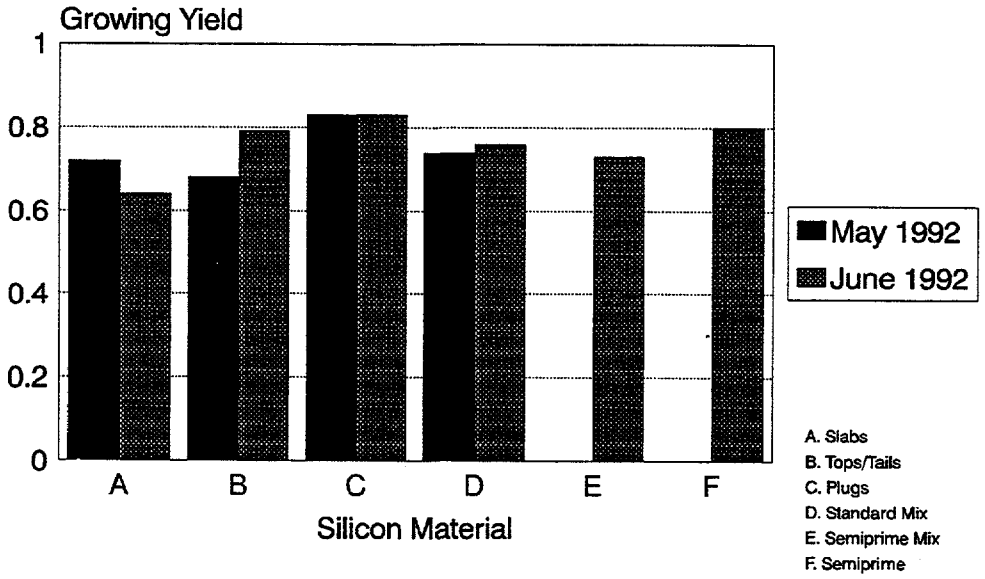


Fig. 1-1. Semi-Prime Poly Silicon Study

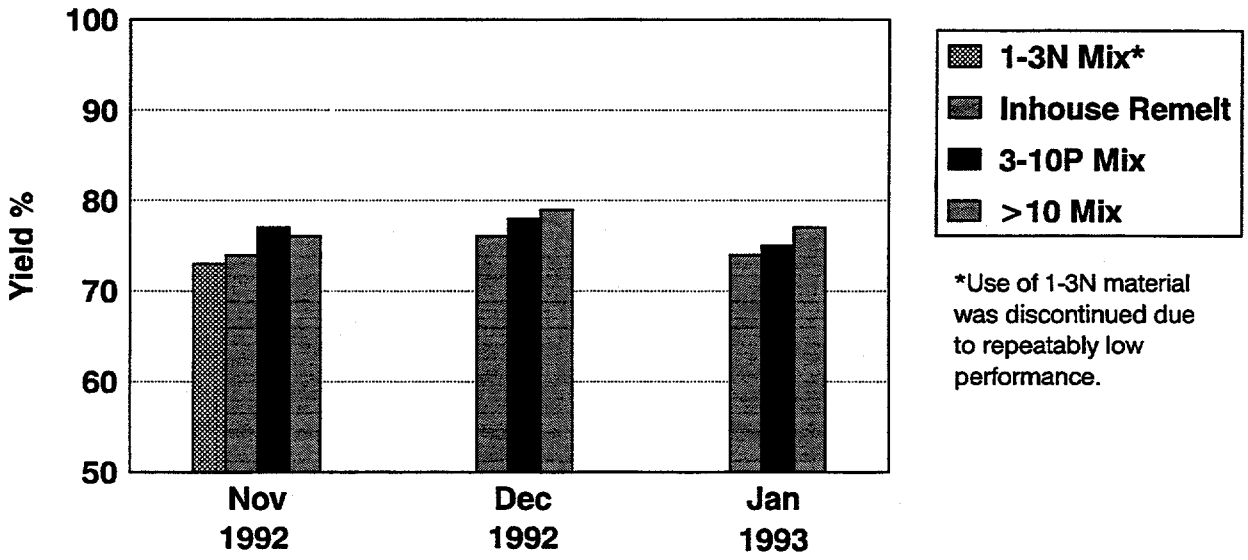
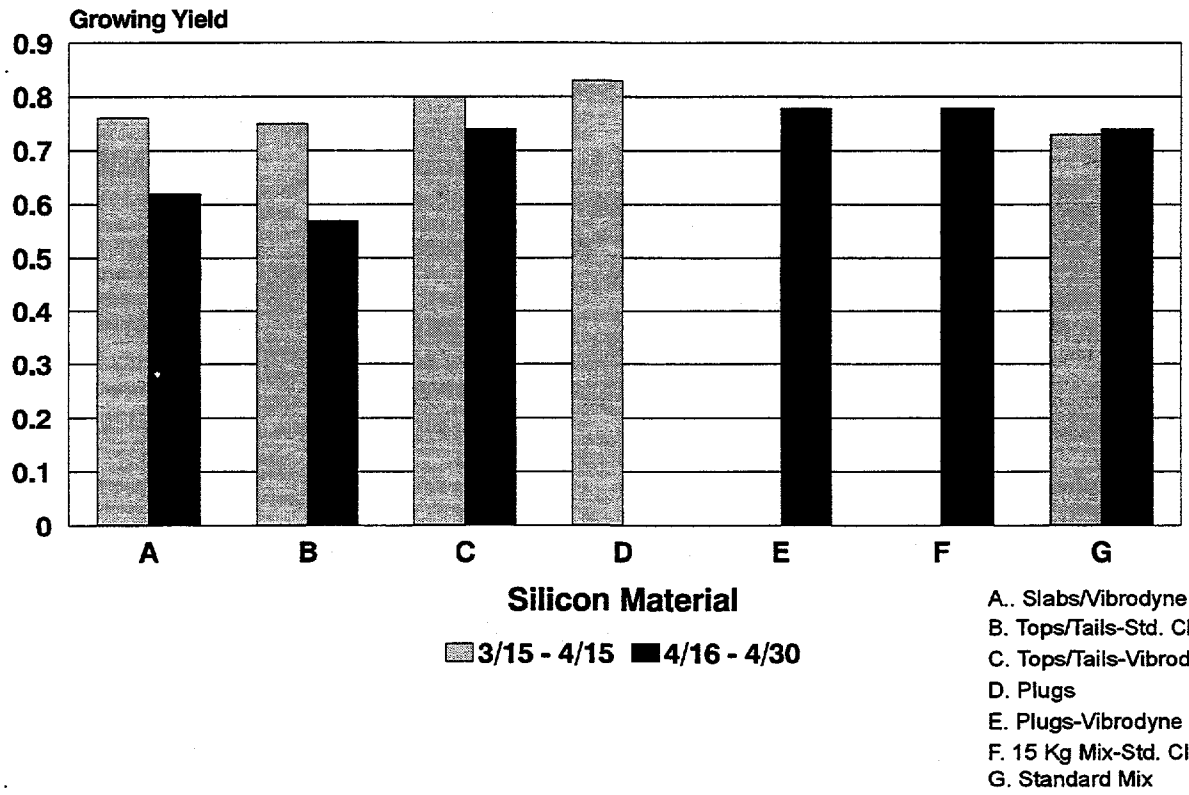


Fig. 1-2 Resistivity Effects of Poly Silicon on Growth Yields

Using an abrasive tumbler we were able to abrade off the outside layer of the slab material, increasing the crystal growing yields. Further studies, summarized in Figure 1-3., were conducted which showed that an overall yield improvement was obtained by placing all remelt material, inhouse and vendor material, through the tumbling process. Yields may still be improved by decreasing the material loss associated with this process.



A.. Slabs/Vibrodyne
B. Tops/Tails-Std. Clean
C. Tops/Tails-Vibrodyne
D. Plugs
E. Plugs-Vibrodyne
F. 15 Kg Mix-Std. Clean
G. Standard Mix

1.2 Crystal Growth

Experimentation with crystal growth techniques began during the second month of the contract.

Experiments initially focused on better techniques for growing ingots from this material. Two types of necking were tested: "step" necking, which produces the fewest dislocations but is slower, and "paintbrush" necking, which is faster and easier from an operations standpoint. The concern during faster pull speed necking is the creation of "slip" dislocations in the crystal structure. The electrical effect of slip dislocation has shown to reduce short circuit current in processed cells. This has been reported by K. Pauls [1]. Cells made from these two different types of ingots do not show a significant difference in electrical performance, thus the faster technique is desirable for production throughput considerations. The results are shown in Figure 1-4.

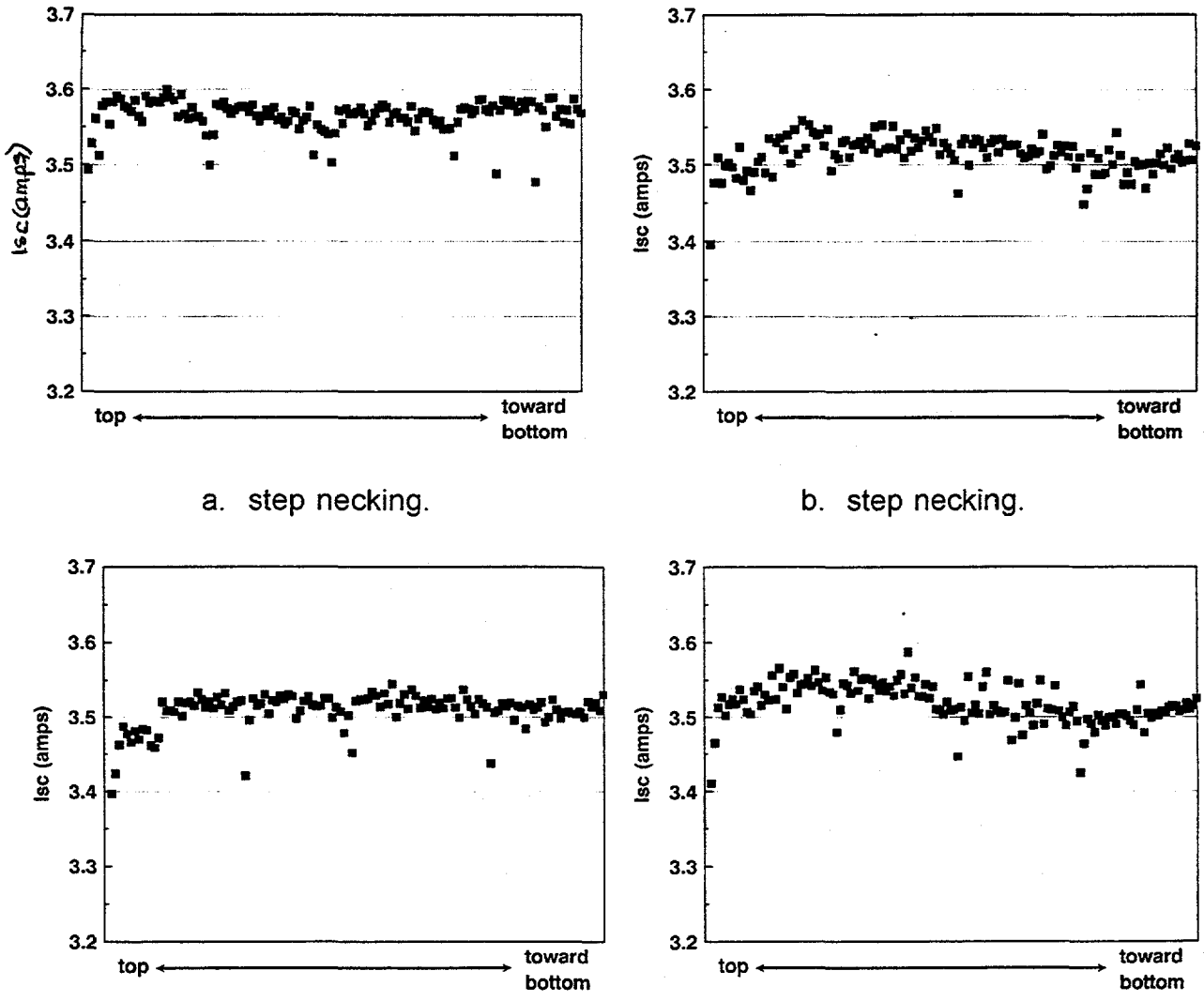


Fig. 1-4. Crystal Growth Technique Study

1.3 Hotzone:

In 1989 SSI installed crystal growers in Vancouver, WA. The hot zone installed in these growers included designs similar to those common throughout the industry. The growers in Camarillo continued to run with an older hotzone design, partially due to the difficulty of adapting the Vancouver design to the shorter tanks found on the older, Camarillo growers. The lifetime of several of the key graphite parts used on the older growers was considerably lower than was possible with a better design.

In the spring of 1992 work began on the design of a new hotzone for the Camarillo crystal growers. The design was tested and eventually implemented on all growers. The results have been remarkable. The most leveraging change was to be able to use the Vancouver style graphite susceptor, which holds the crucible during the run. Several other design changes were required to allow the Vancouver susceptor to be used in Camarillo.

The old graphite susceptor had a top and bottom piece and was used for 4-6 runs before being replaced. The new susceptor design as shown in Figure 4, costs slightly less per unit than the old design, and is used for 18-22 runs. The savings in direct materials cost for the susceptor alone is $224,000. Other savings resulting from design improvements include the heaters and insulating heatpack. The total yearly cost savings for the project is estimated at between $400,000 and $600,000.

Other design improvements which are significant, though the cost savings are indirect, include a spill tray and an upper ring. The upper ring reflects radiation back onto the ingot as it is pulled out of the hotzone in order to minimize the build up of oxide on the ingot walls.

1.4 Recharge:

Most of the effort in Vancouver for 1992 was concentrated on the investigation and development of a recharge process. The process chosen was batch recharge as opposed to semi-continuous recharge. The process was never able to obtain the yields required to compete with the baseline process. Figure 5 shows the yields for the recharge process as compared with the baseline process for the months of March through August. The low yield for the recharge process is a result of the poor quality of recharge poly material. The prohibitive cost of better material far outweighs the cost savings of the crucible usage for recharge. At this time, SSI has decided against further development of a recharge process.

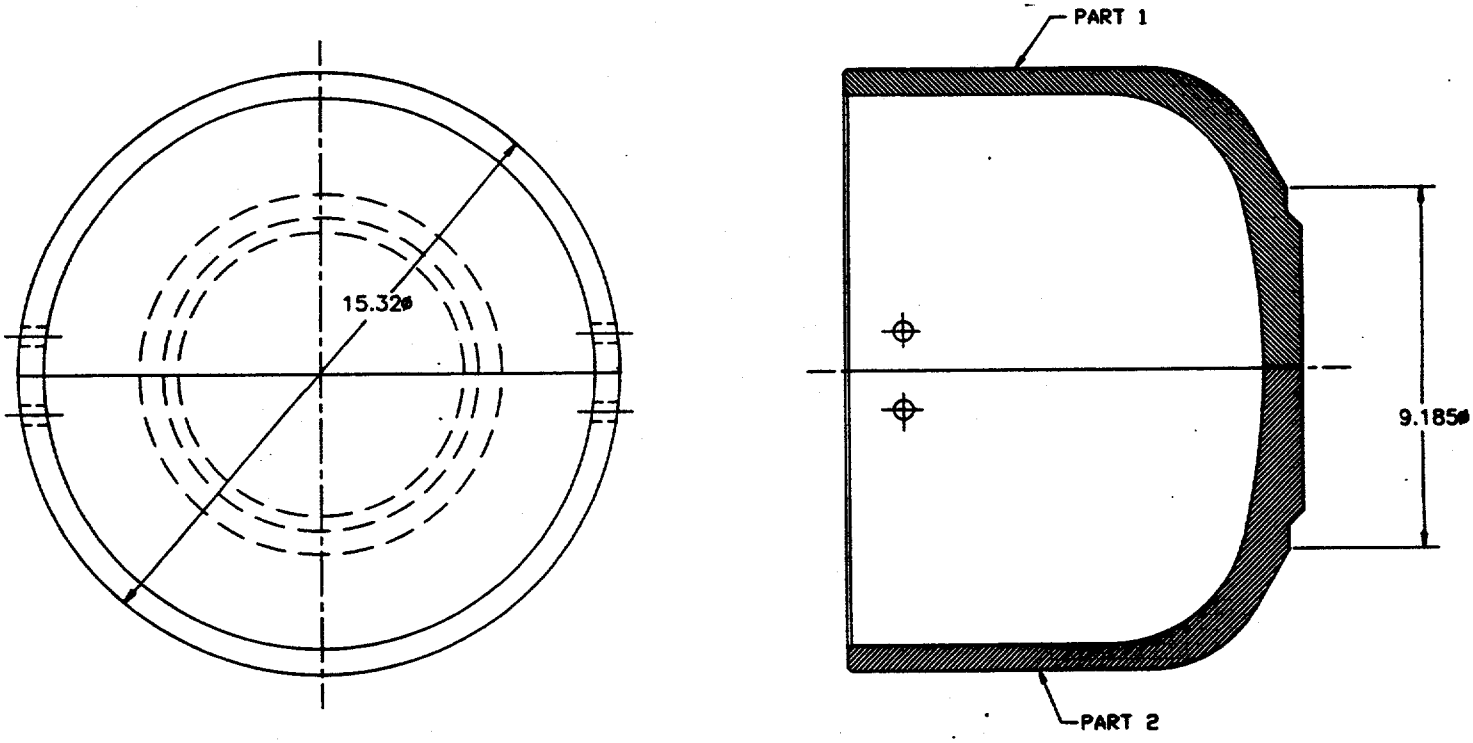


Fig. 1-5. Crystal Growth Graphite Susceptor Design

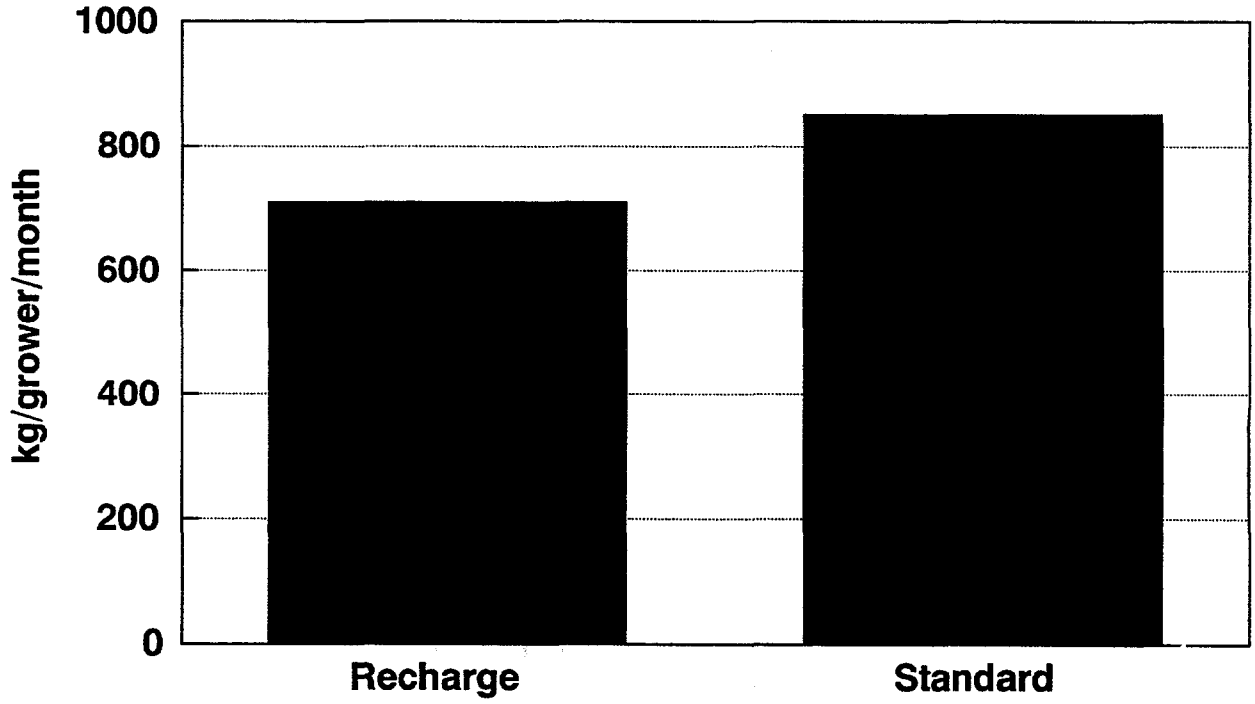


Fig. 1-6 Recharge Process vs. Standard Growth Process

1.5 Crucible Studies:

A two part study of oxygen concentration was begun during this phase. The study includes looking at different types of crucibles and altering growth parameters like pull speed and rotation speed.

The crucible is the major source of the oxygen which is incorporated into a silicon ingot during growth. Crucibles with a denser, bubble free layer on the inside wall have been shown to devitrify less and to contribute less oxygen to the melt. A set of "low bubble" crucibles was compared to standard crucibles and samples of the silicon ingot taken from the top and the bottom of the ingots. Fourier Transform Infrared, FTIR, technique was used to measure the oxygen concentration on each sample. The results, Figure 1-7., show the oxygen concentration for the low bubble crucible to be lower at the bottom of the ingot than for the standard crucible.

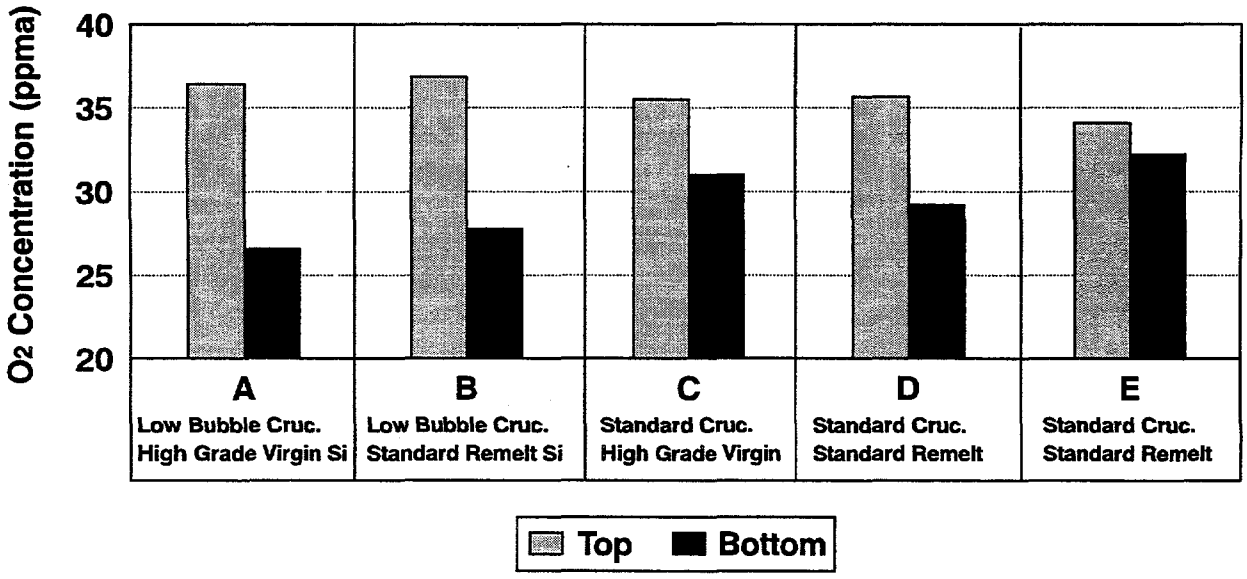


Fig. 1-7 Crucible Study

1.6 Higher pull speed investigation:

An informal review of the methods used to increase pull speed was conducted and initial designs for a radiation shield developed. The shield sits above the melt and the ingot passes through a hole in the center of the shield. Radiation from the melt is redirected down, allowing the ingot to cool more quickly. Several materials of construction are being considered for the shield. Designs for the radiation shield which require no moving parts are highly favored. One problem with a stationary design is that the initial packing of the silicon charge is currently mounded high above the top of the crucible, which restricts the positioning of the shield. A study is underway to address charge packing. Prototype parts have been ordered and are expected in April.

The effect of all of the work conducted in the Crystal Growth program under this contract resulted in over 8% demonstrated improvement in Crystal Growth.

1.7 Wiresaw Evaluation:

A prototype, commercially available wiresaw was tested and a process developed for manufacturing of silicon wafers for photovoltaic use. The development is ongoing with further process and equipment improvements anticipated. At the close of Phase 1, the average number of wafers/inch obtained on the wiresaw is 37 wafers/inch which is a 30% improvement over the results obtained for ID sawn wafers. Figure 1-8. shows the increased wafers per inch.

Wiresaw process improvements completed during this phase include improved slurry mixing, implementation of a spray wash at the conclusion of a wiresaw run, installation of slurry manifolds to uniformly distribute slurry, and implementation of vacuum chuck mounting of the ingots which significantly reduced set-up time.

Several critical issues have been identified for further improvement of the wiresaw process. They include:

- Wire requirements and usage
- Slurry and solvent usage
- Water based slurry development
- Training and procedure completion
- Wafer cleaning after wiresaw
- Ingot mounting

The most significant of these has been the combination of wire usage and slurry usage. The yield trend with number of slurry runs is shown in Figure 1-9. The quality of wafers sliced varies significantly in thickness control and taper (non-parallel sides) if these parameters are not tightly controlled. The goal is to maximize the amount of runs obtained with each wire change and slurry batch used. The amount of these materials consumed per run or per wafer is a very important parameter for cost effectiveness in manufacturing high volumes of wafers. Further studies are planned for Phase II of this contract with emphasis on the optimization of this process in high scale production.

The use of wire saws has been proven to be effective in production under Phase I of this contract.

1.8 Thin wafers:

During Phase I of the project, the wafer thickness was reduced from 450 microns to 350 microns. The thickness reduction was possible because of the reduction in surface damage using the wiresaw, compared with the damage caused by ID saws which then needs to be removed . Experiments on cutting thinner wafers are continuing. The yield and electrical performance data of this change is discussed in the following section. All thin wafer deliverables were met under Phase I of this contract.

All thin wafer deliverables were met under Phase I of this contract.

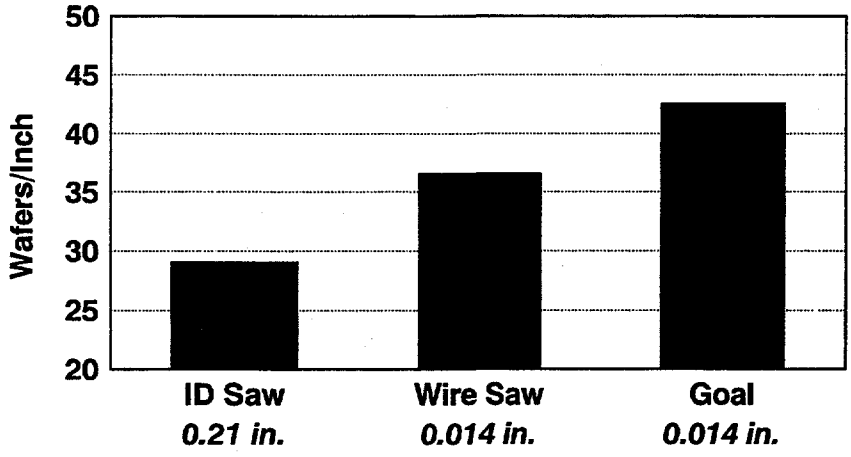


Fig. 1-8 Wire Saw vs. ID Saw Wafers per Inch

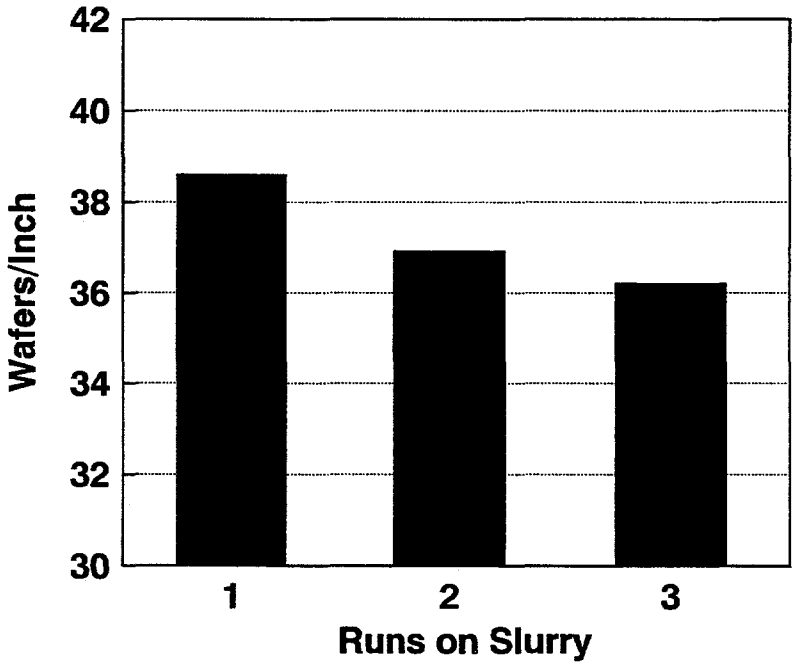


Fig. 1-9. Yield of wafers per inch versus the number of times the slurry is used.

SECTION 2.0
CELL PROCESSING

Cell processing costs are driven by the amount of silicon used per cell (wafer thickness), the electrical performance of the cells, and the labor required for the processing of wafers into active cell devices. The work in this area has been focused on the reduction of labor through automation of various steps, the improvement of the electrical means of the cells processed by improving the contact resistance and diffusion processes. This work has been overlaid onto the results incurred by using thinner wafers. Yields and performance v. cell thickness have been closely monitored, and are described below.

As cell thickness has decreased, the need for automated handling has increased. This coupled with the necessary reduction in labor costs, required a whole new method for anti-reflective coating, printing and firing, and testing cells.

2.1 Thin Cells

A study done to examine the effect of wafer thickness, mechanical yield, and electrical performance was performed during the second quarter of this contract. The experiment used four groups of wafers, two cut by both ID and wire saws. The experimental groups, and the test results are shown below:

Experimental Groups

1. "A" wafers, 17.5 mil cut by ID saws
2. "B" wafers, 17.5 mil cut by wire saws
3. "C" wafers, 21 mil cut by ID saws
4. "D" wafers, 15 mil from the CAM wire saws

- All groups were run through the standard production line with no special handling.
- Groups "A" and "D" were etched to 14 mils at the wetline.
- Groups "B" and "C" were etched to 17 mils at the wetline

Results:

Table 2-1. Cell and Wafer Thickness vs. Performance

Groups-->	A	B	C	D
Total wafers processed	7560	5740	7000	8960
Total cells completed	7054	5573	6787	8217
% loss (Breakage)	6.69	2.91	3.04	8.29
AMP (mean)	3.191	3.235	3.204	3.197
Loss at stringing/Lam (%)	1.74	3.97	1.72	1.5
Average module (Watts)	53.46	53.81	54.13	54.32
Standard Deviation	0.63	0.45	0.67	0.44

The results of the tests can be summarized as follows:

- Breakage was highest with the thin wafers, especially the thin wire saw wafers. This result had been expected. Most of this breakage did occur at print, dry, fire operations because of the multiple handling steps, followed by the diffusion area which also has a boat transfer operation. The thicker ID and wire sawn wafers did not show a significant difference in breakage and the "thin" ID and "thin" wire indicated a comparable breakage.

- The Electrical $mean_{(amps)}$ did not show significant differences with the exception of the final "thin" wire group. No explanation can be given for this deviation.

- Automation or semi-automation of wafer handling between the AR coater, printers, and testing machines needs to be implemented. The flow chart in Figure 2-1. shows the process sequence, with material transfer points labelled.

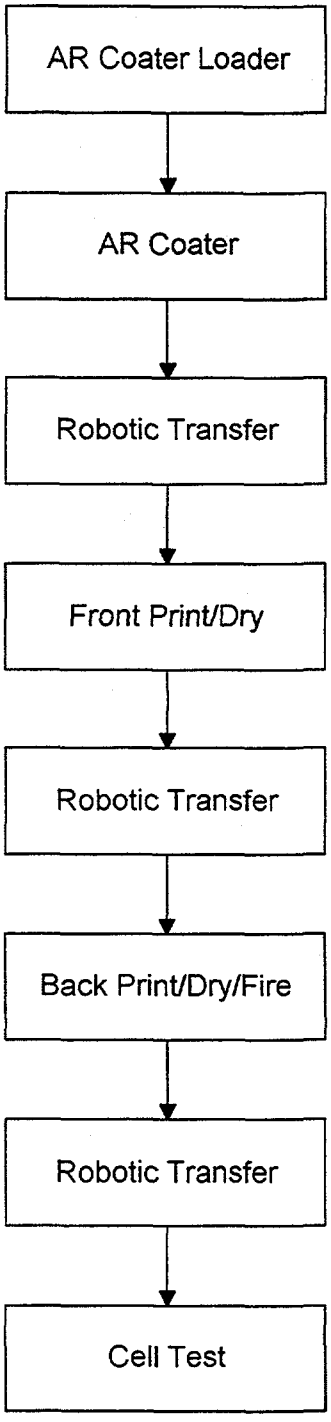


Fig. 2-1 Automated Cell Handling Process Sequence

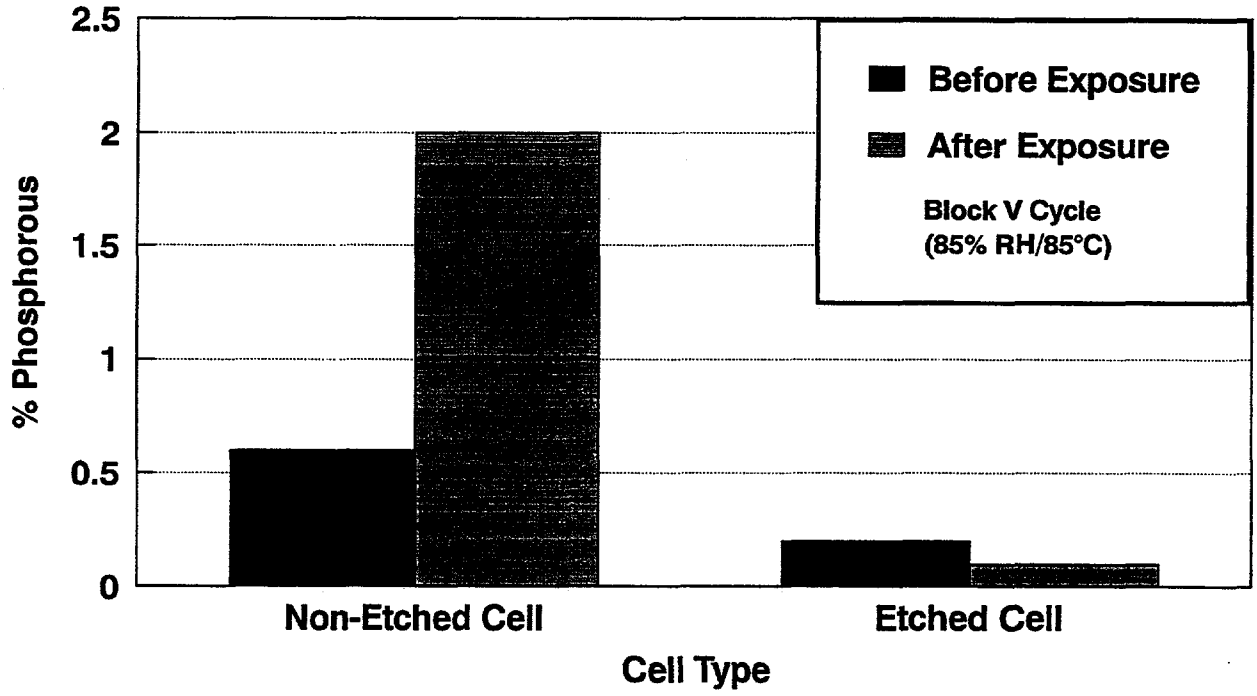


Fig. 2-2. Humidity Sensitivity Study
Eight Days Humidity Freeze Cycle

2.2 Cell Electrical Performance

The cell electrical distribution has improved significantly as a result of improved contact and diffusion processes. In defining and experimentation with process changes, an interesting and significant cell performance sensitivity was discovered. Certain processes showed significant sensitivity to environmental exposure, particularly humidity exposure. Figure 2-2. shows the results of humidity exposure v. process type with a significant change in the amount of Phosphorus present before and after exposure. This larger amount of Phosphorus coincided with visible delaminations in the modules made with these cells.

Through these studies, coupled with contact firing process changes, contact coverage re-design and diffusion changes, a significant shift in the electrical performance was effected. This shift is shown in Figure 2-3. It should be noted that this effort also reduced the amount of Silver paste used for the front contact by over 48%. This savings in materials represents an annual savings of over $100,000 in material usage.

Significant work on front paste formulation changes has yielded no significant electrical improvement. to date. More studies are planned in Phase II of this contract.

Work on improving the etching process by agitation of the baths also yielded no significant improvement electrically, although cosmetic improvements were noted. This process change was implemented in manufacturing as a standard procedure.

The development work done under the Cell Processing Task of this contract has yielded over a 10% improvement in cell costs.

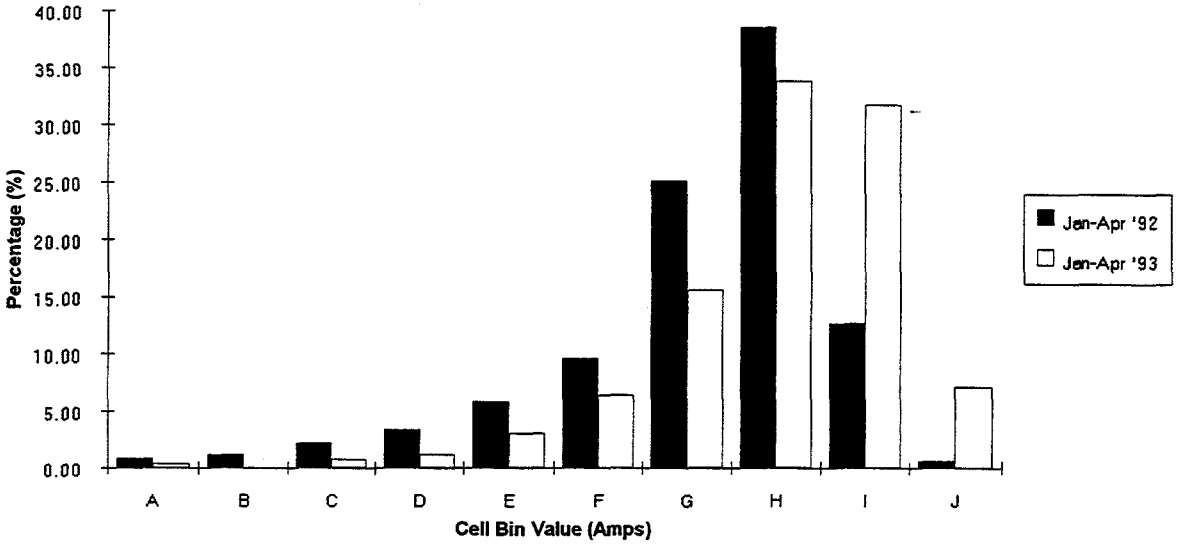


Fig. 2-3. Electrical Distribution Improvement

SECTION 3.0
MODULE FABRICATION AND ENVIRONMENTAL, SAFETY AND HEALTH ISSUES

3.1 Environmental, Safety and Health Issues

In the area of Module Fabrication and Environmental, Safety and Health Issues task, the focus during this reporting period was on the elimination of chlorofluorocarbon (CFC) usage in the manufacturing facility. The project had three phases:

- The reduction of CFC usage in manufacturing
- Evaluation of alternative solder paste materials which do not require CFC cleaning
- The removal of CFCs and the implementation of the alternative solder paste materials

The CFC usage reduction program evaluated both using CFCs more efficiently and alternatives to CFCs for cleaning. Work began on assessing water soluble flux options and various low solids fluxes for soldering. In conjunction, several opportunities for reduction were identified and implemented:

- Additional tank coverage to reduce the amount of evaporation from the ultrasonic baths used for defluxing of solder points.
- Colder chilling water to help condense and trap more liquid for re-use.
- Cleaning of fan blades, screens and heat sinks to help maintain the maximum heat exchange rate for condensation of vapors.
- Re-plumbing of chill water lines for additional cooling capacity.

These modifications to the ultrasonic baths were implemented and produced a reduction in CFC usage of approximately 60%.

The first round of testing for alternative solder paste materials involved water soluble solder flux, which looked promising for replacing the flux currently used in production. Subsequent qualification of the modules in Block V tests failed in less than five humidity-freeze cycles. It appears that the water rinse of the cells retained moisture during the lamination sequence. The modules appeared cloudy and showed a tendency to delaminate the EVA bond after a short humidity-freeze exposure. From

this information, water soluble fluxes were abandoned as an appropriate substitute for CFC defluxing.

The next focus was on low solids fluxes that could be left on the substrate after soldering. An assortment of candidates solders were tested. Modules were made from each solder to first evaluate it compatibility with the in-house soldering equipment (semi-automatic and manual), followed by full environmental testing. The flow chart in Figure 3-1. shows the series of experiments:

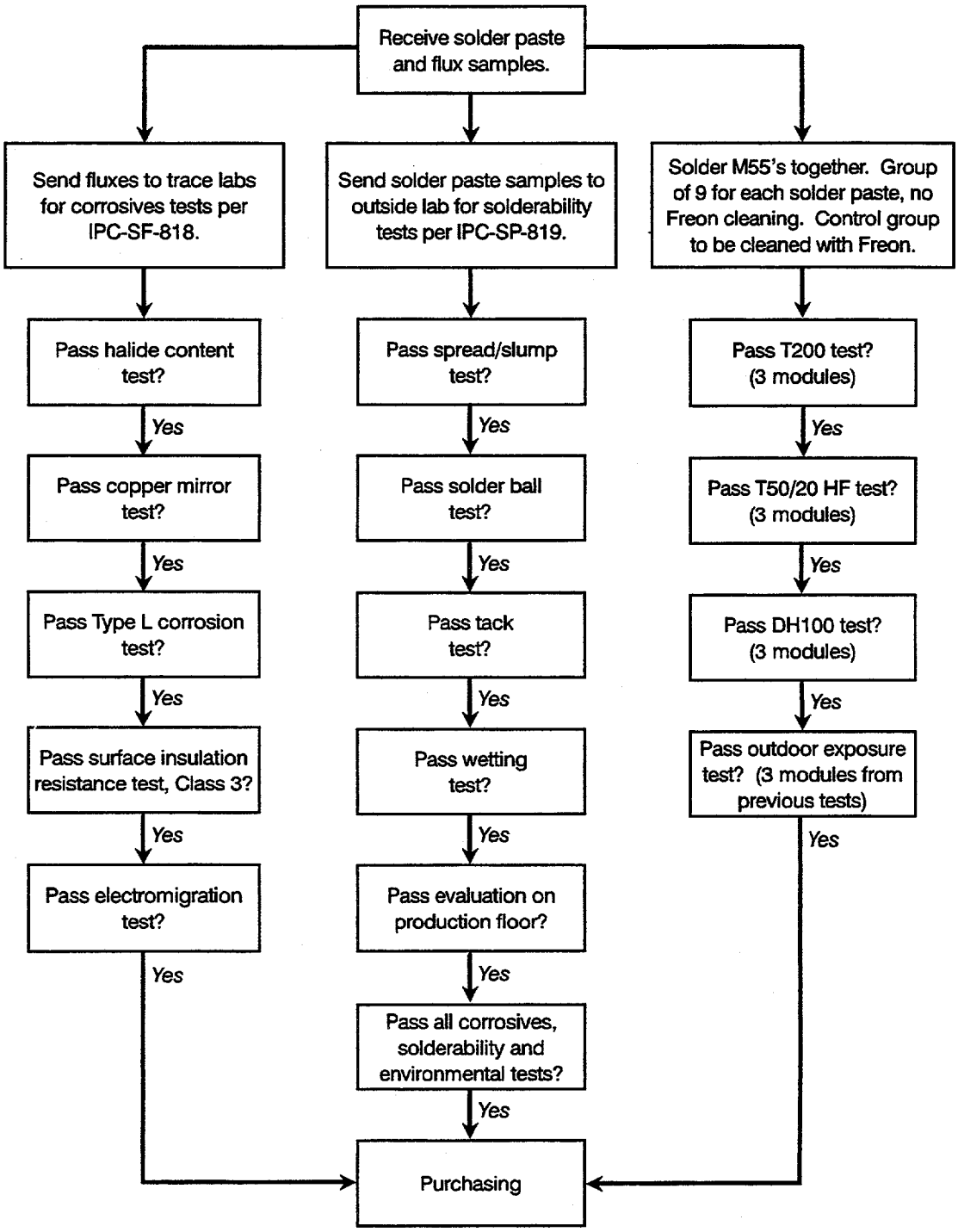


Fig. 3-1. Flowchart showing experiments conducted.

Of solder pastes evaluated, one proved to be acceptable, passing all required characteristics. The following table indicates which pastes were evaluated and their results:

Table 3-1. Solder Paste Evaluation

Manufacturer	Mfg #	Corrosive Level of Flux	Block V Test
Heraeus Cermalloy	SC3610S-1	Pass	Fail
Alpha Metals	LR701	Pass	Fail
Kester	R-244	Pass	Fail
ESP	6-Sn62-500-A	Pass	Pass
Alpha Metals	RMA 341	Fail	Fail
Heraeus Cermalloy	SC3300S	Pass	Fail
AIM	LR5	Fail	Not done
IEM Fusion	NCR-D-7C-3	Fail	Not Done
Dupont	VLR0620	Fail	Not Done
Hereaus Cermalloy	Flux#SF-33-2	Pass	Fail

After selection of the paste, implementation in manufacturing started. This included:

- Modifications to the solder paste application system (hardware and software)
- Modifications to the soldering lamp temperature profile and soldering time
- Installation of the new "no-clean solder paste" with continued CFC cleaning to verify application technique and soldering criteria acceptability/process debug
- Documentation of new solder paste specifications, process procedures, bills of materials, and equipment modifications
- Removal of ultra-sonic CFC defluxing equipment

- Training of manufacturing personnel

- Re-evaluation of random modules produced by manufacturing through Block 5 test

The complete removal of CFCs from manufacturing occurred during May 1993. We continue to evaluation the equipment and solder paste performance. At the present time work also continues on the issue of alternative solder flux cleaning methods, since there is "some" flux remaining on the cell. Additionally, lower viscosity pastes are being evaluated to improve the "dispensibility" of the material.

3.1.2 Caustic Waste and Fluoride Waste Reduction

The second task in the Safety, Health and Environmental area is the significant reduction of the caustic waste volumes and the removal of Fluoride from the waste stream. Several vendors were investigated with two primary vendors proposing methods for production use:

Several proposals have been submitted by both companies and the scope of work proposed includes:

- Collect samples to verify the concentration of waste materials (analyze samples)
- Do engineering study to design system
- Do financial feasibility study
- Run pilot equipment in a manufacturing environmental to test feasibility of design
- Finalize full scale manufacturing system

Figures 3-2. and 3-3. show the proposed methods for caustic waste reduction and fluoride waste reduction respectively. This work will continue under Phase II of this contract. SSI is presently evaluating the proposals from both engineering groups

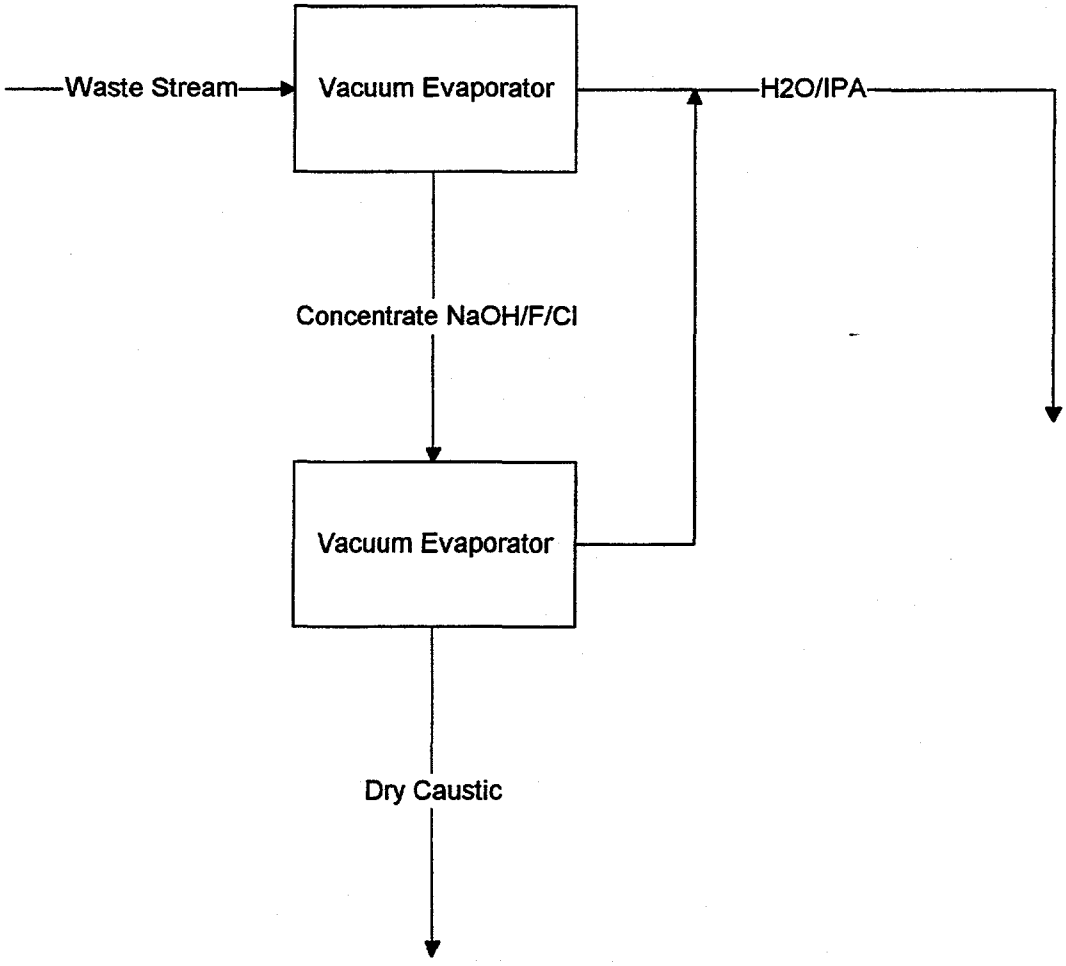
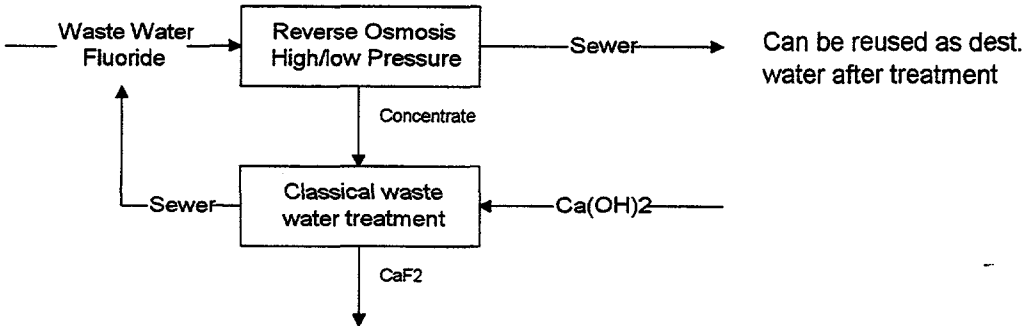
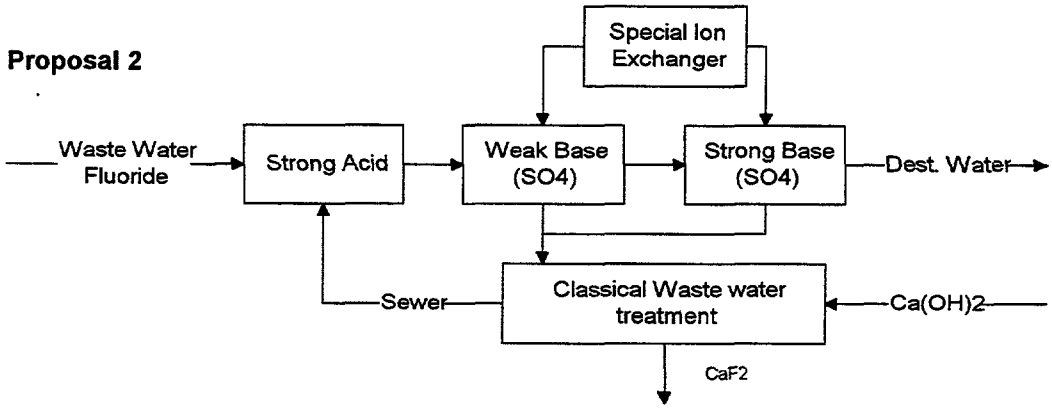


Fig. 3-2. Proposed Caustic Waste Reduction Process

Proposal 1



Proposal 2



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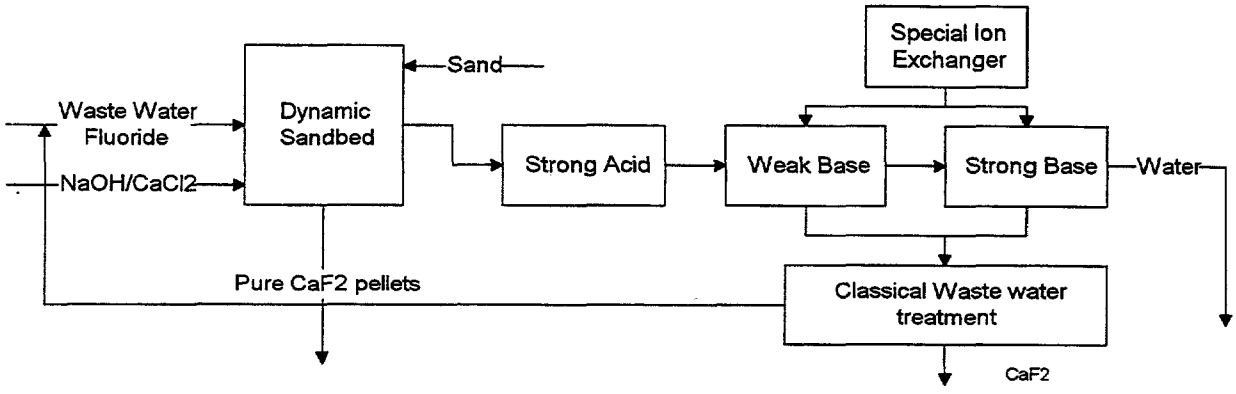

Fig. 3-3. Proposed Fluoride Waste Reduction Processes

3.2 Module Development:

Significant progress in cost reduction in module design has been made during Phase I of this contract. Several items have been identified and implemented in manufacturing to reduce the final cost of modules manufactured. The first of these improvements showed the use of anti-reflective glass etching to decrease the amount of reflected light on a module surface. Greater than a 1 Watt improvement in electrical power was seen on M55 style modules (reference Figures 3-4. and 3-5 respectively). This gain is shown in Figure 3-6. with varying the degree of etch. Although this proved to be a significant electrical performance boost at a low cost, the commercial availability of this glass is quite limited, and use of this material in high volume manufacturing is not feasible.

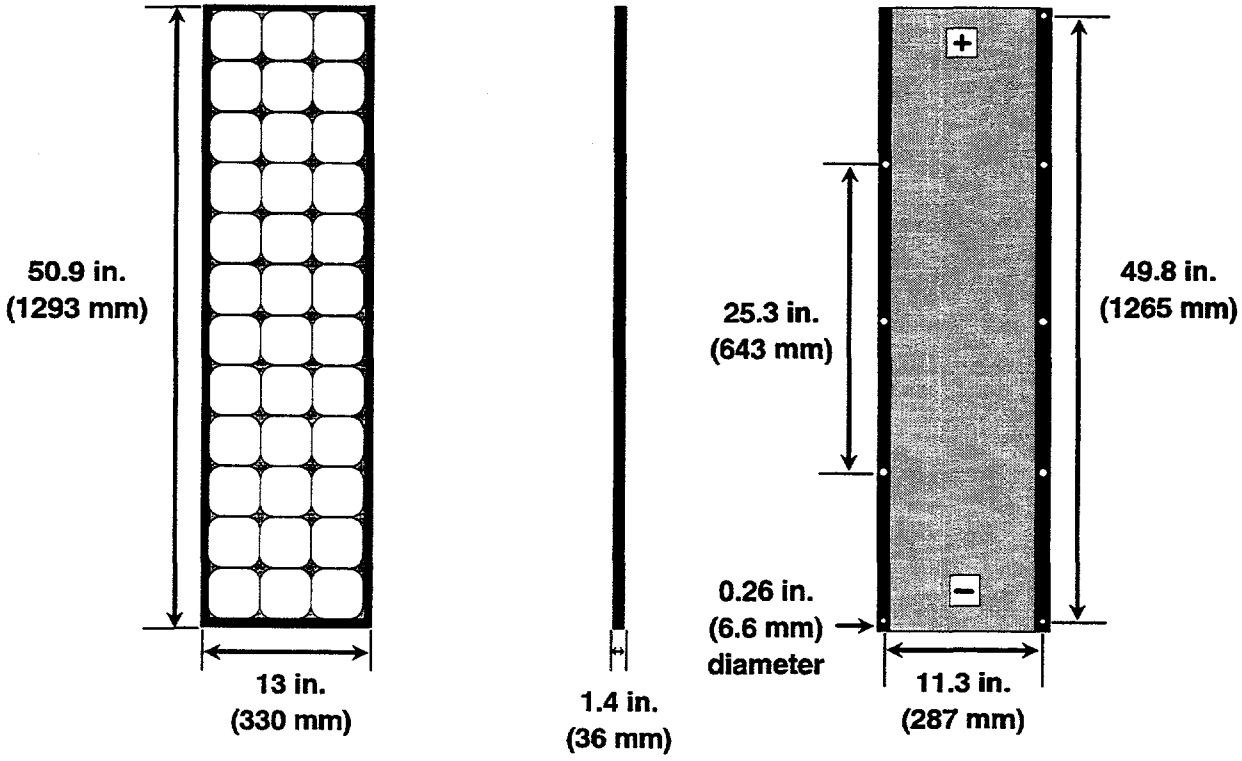

Fig. 3-4. M55 Module Design

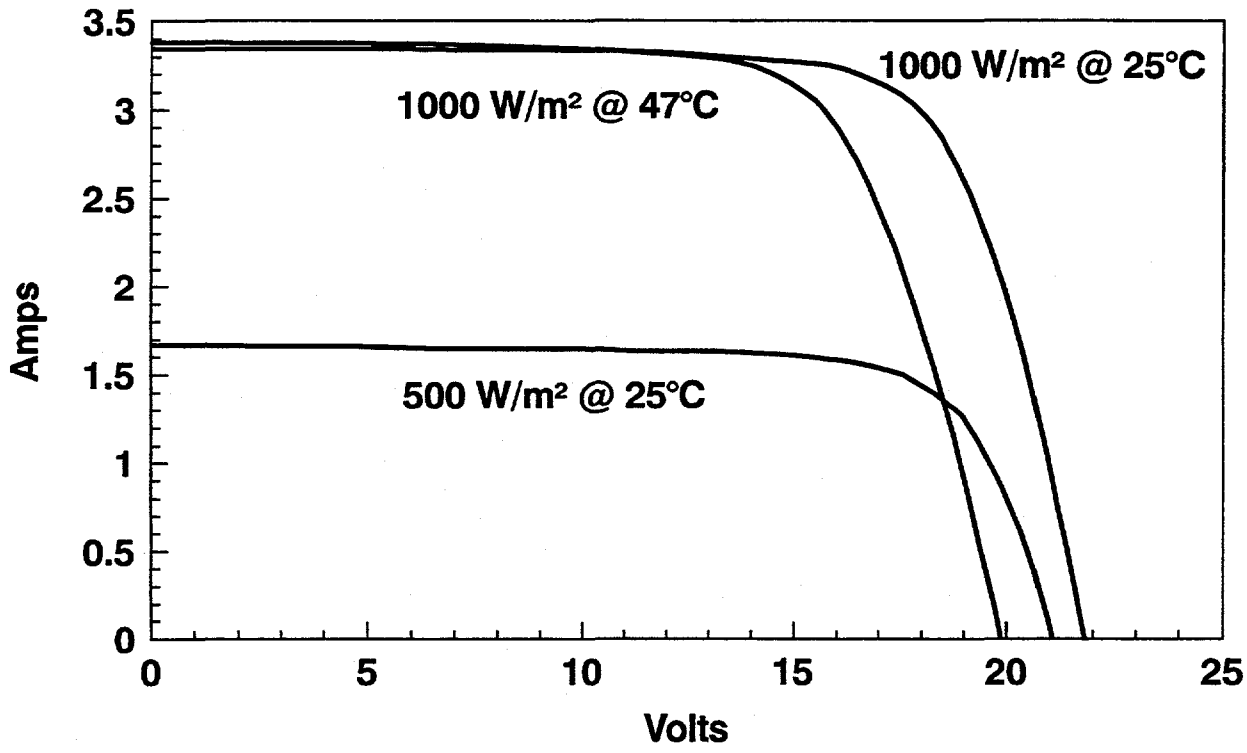

Fig. 3-5. M55 Electrical Characteristics

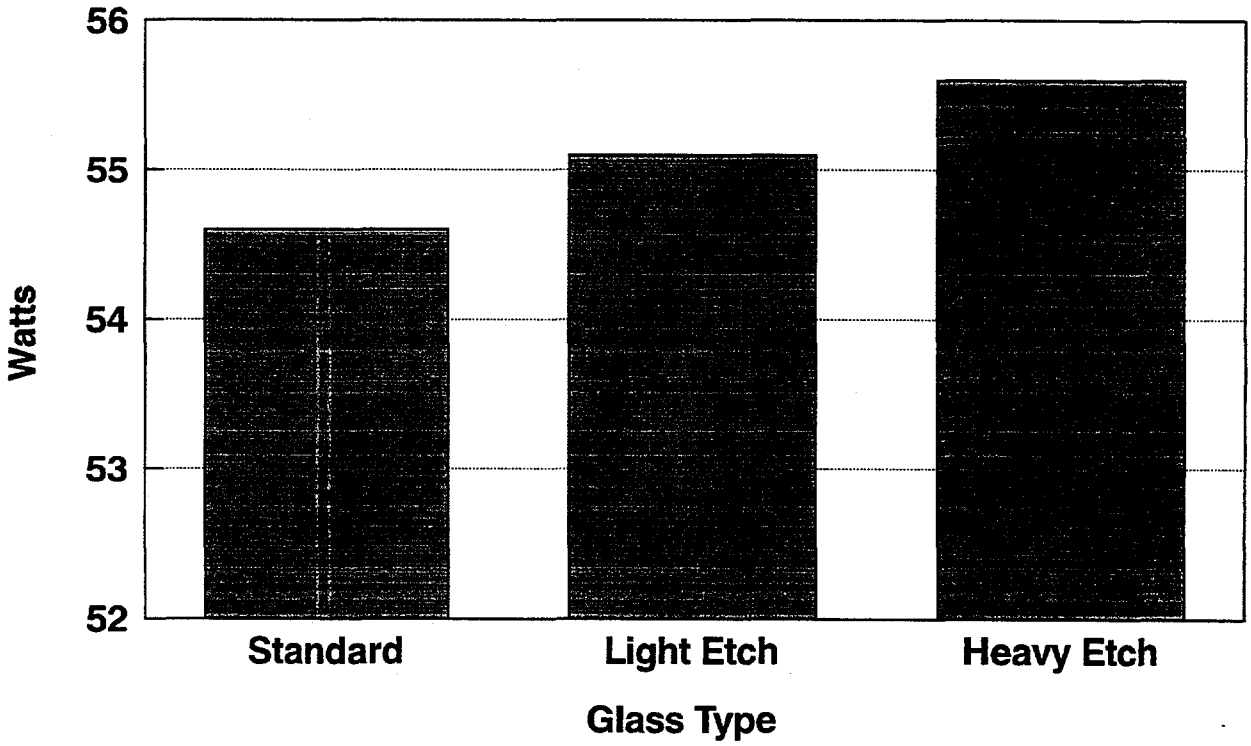

Fig. 3-6. Anti-Reflective Glass Performance Improvement

A second item which showed significant benefit is the use of a "whiter" Tedlar™ backsheet which gave an overall 0.5 Watt gain in electrical performance on an M55 module. The use of "whiter" Tedlar™ has been implemented in full scale production.

The final module improvement has been in the development of a new junction box for modules. This cost improvement in manufacturing is over 1% total, and is currently being investigated for Underwriters Laboratory for approval, prior to production implementation.

All module deliverables, and Safety, Health and Environmental deliverables were met under Phase I of this contract.

4.0 Summary

Table 4.0 shows the categories and total savings for manufacturing cost improvement as completed under Phase I of this contract. As can be seen, the 10% overall goal has been met. In addition, the complete elimination of CFC use has exceeded the contract goals by over two years.

Table 4.0. Phase I Total Cost Improvements

Goal: 10% 1st Year

Category	% Reduction in Cost
1. 35 vs. 29 wafers/inch	6 %
2. 3% power increase due to cell improvements	2.5%
3. Module improvements - Whiter Tedlar - Antireflection glass	1.5%
4. New J-box	1 %
Total	***11%***

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THE EFFECT OF DISLOCATIONS ON THE PERFORMANCE OF SILICON SOLAR CELLS

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Camarillo, California 93010

ABSTRACT

The existence of slip dislocated material in Czochralski silicon ingot and the effects of the dislocations on solar cell performance have previously been identified. In this paper, cell performance as a function of dislocation density and the distribution of dislocations across a wafer has been characterized in order to quantify the performance losses associated with dislocated material. In addition, improvements in wafer and cell processing have decreased the impact that dislocated materials have on solar cell performance.

INTRODUCTION

During Czochralski silicon ingot growth, dislocations can be formed by the stresses induced by the thermal shock of removing the ingot from the melt and by the loss of single crystal structure. Typically, the distance that dislocated material extends up from the tail of the ingot approximately equals the final ingot diameter. Since the ingot cost is a significant fraction of the total solar cell cost for crystalline Si solar cells, maximizing ingot and wafer yields is important. Therefore, a Si solar cell manufacturer must understand the relationships among processes, dislocations and cell performance in order to determine how to minimize performance and yield losses due to dislocations.

This paper presents the results of a study of crystalline Si solar cell performance as a function of dislocation density and distribution. As will be shown, solar cells are tolerant of dislocations densities up to 500/cm^2 to 800/cm^2. Above these dislocation densities, the solar cell performance decreases due to reduced photocarrier collection from the bulk.

Comparative studies of wire saws and inner diameter (ID) saws have demonstrated that wire saws produce significantly less surface damage on the wafers than ID saws [1]. Reducing the amount of surface damage produced during wafer slicing is found to reduce the cell performance losses associated with dislocations.

This work was supported in part by the U.S. Department of Energy's Photovoltaic Manufacturing Technology program under National Renewable Energy Laboratory Subcontract ZM-2-11040-1.

EXPERIMENT

Ingots with three very different tails (bottom of the ingot body) were studied, namely, (1) a preferred case where the ingot maintains single crystal structure and has an adequate tail that tapers gradually to a small diameter, (2) an ingot that lost its single crystal structure during body growth and (3) an ingot that was pulled prematurely from the melt and did not receive an adequate tail. Note that in the present cell design in which the round ingot is slabbed into semi-square cells, dislocations located in the slabbed material are absent from the cells.

The three ingots were cut into wafers and sample wafers taken every inch along the ingot, measured from the point that the tail was cropped from the ingot. The sample wafers were mechanically polished and then chemically etched using a modified Schimmel etch [2], which preferentially etches the dislocations and leaves clearly defined etch pits on the wafer surface. The dislocation densities were quantified using the ASTM standard method [3] for Si wafers, slightly altered to accommodate semi-square rather than round wafers. The arrangement of sampling points is shown in Fig. 1. The first 9 points were used for the ASTM measurement for the whole wafer, and the remainder for a more detailed study of the lateral distribution of dislocations across the wafer.

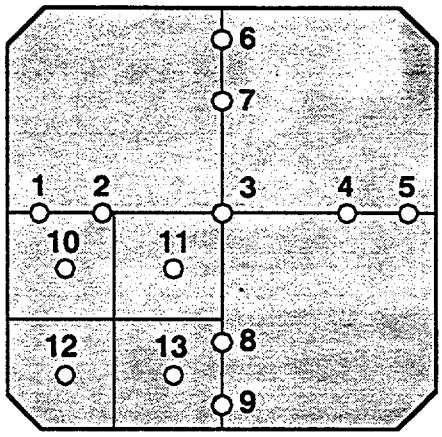

Fig. 1. Sampling positions for measuring dislocation counts on crystalline silicon wafer.

The remaining wafers were fabricated into solar cells using the Siemens Solar Industries' manufacturing process, keeping the cells in order throughout processing. The cells were then

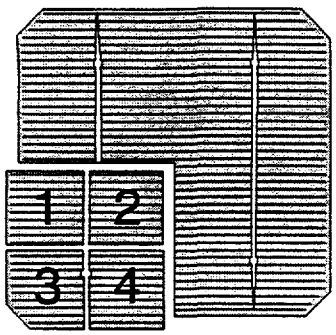

Fig. 2. Crystalline silicon solar cells showing subcells that were diced out of the original cell.

light current-voltage (I-V) tested. Sample cells were taken every inch to coincide with the positions of the sample wafers used for etch pit studies. An optical beam induce current (OBIC) scan was performed on one quadrant of each sample cell. In previous work, OBIC studies of completed cells have provided a simple method for identifying the presence of slip dislocations in the silicon. The same quadrant of the cells was then diced into four subcells (Fig. 2). The light I-V and spectral response were also measured on each of the subcells.

RESULTS

Figure 3 shows plots of short circuit current (I_{sc}) versus wafer position in the ingot, comparing data from the Spring of 1991 [4] with data from the Spring of 1993. In both cases, the wafer location begins with cells made from wafers at the bottom of the ingot body. Two significant differences appear in the data sets. The first is a shift upward of the I_{sc} plateau, which represents improvements achieved in the cell processing technology over the last two years. The second difference is in the ramp up to the I_{sc} plateau, which represents the performance of cells with varying densities of slip dislocations. In the 1993 data, the short circuit current starts at about 3.3 amps, where the 1991 data is as low as 2.8 amps at the start. About 0.1 amps of the difference can be attributed to the overall shift upward in performance as seen with the plateaus. The remaining 0.4 amps difference between the data sets is attributed to changes in the wafer slicing and cell fabrication processes, which reduce the impact of dislocations on the device performance.

Wafers cut using wire saws have been found to have significantly less surface damage than wafers cut using ID saws. In addition, compared to ID sawn cells, the wire sawn cells have less slip dislocation performance losses. Alternatively, cells made from ID sawn wafers which are etched to remove more of the damaged surface layer show increased tolerance to the dislocations. The link between surface layer damage and tolerance to dislocations is significant and warrants further study.

OBIC measurements made on the 1993 cells were less effective in identifying dislocated areas due to reduced dislocation related photocarrier losses. Thus, dislocation etching was used to quantify the dislocation densities. Performances of sample cells taken each inch along the ingot were compared to the measured average dislocation densities for corresponding wafers. Although the general trend is as expected, namely, lower efficiencies for higher dislocation densities, the variability of the data is significant. The dislocation density, and, as a result, the cell performance, can vary significantly across the cell. Figure 4 is a photo of the etch pits at 200x magnification for a center subcell and the corresponding light I-V curve for the subcell. Figure 5 is an etch pit photo and I-V curve for an edge subcell from the same original sample cell. For the two adjacent subcells, the dislocation densities vary from 681/cm^2 to 19/cm^2 and the cell efficiencies vary from 13.6% to 14.9% respectively.

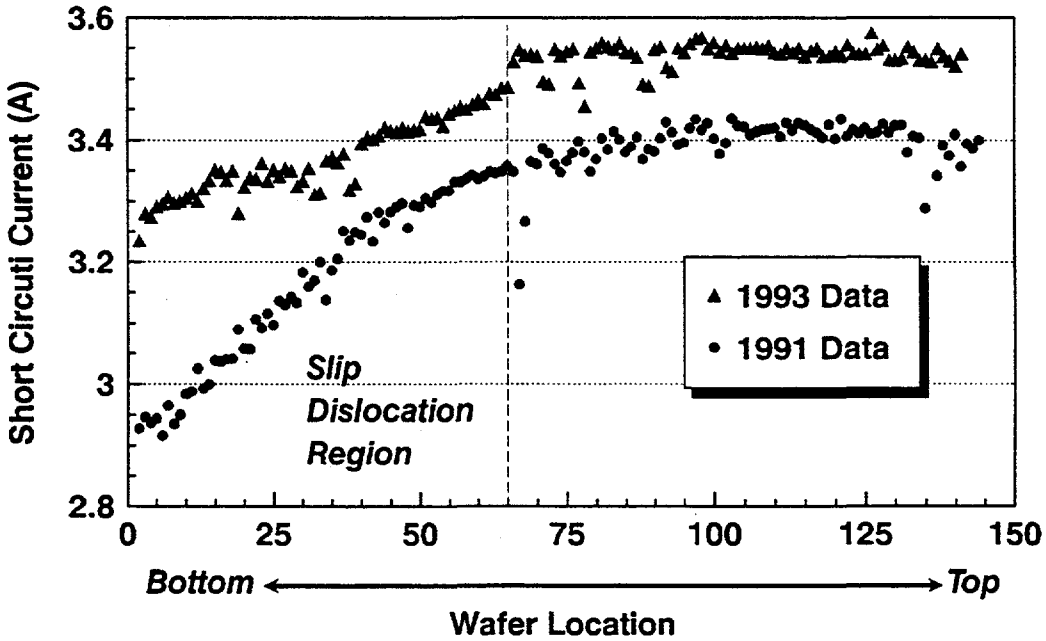

Fig. 3. Comparison of 1991 and 1993 short circuit current versus wafer position in the ingot showing reduced impact of slip dislocations due to changes in wafering and cell processing.

Fig. 4a. Photo of dislocation etch pits for area at the center of the corner subcell.

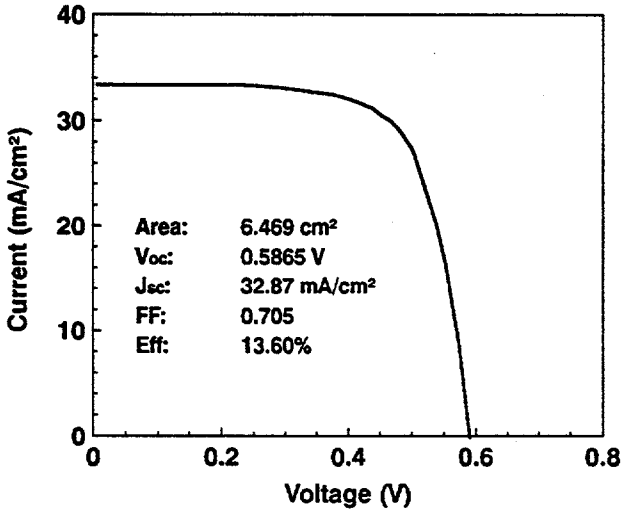

Fig. 4b. Current-voltage curve for corner subcell.

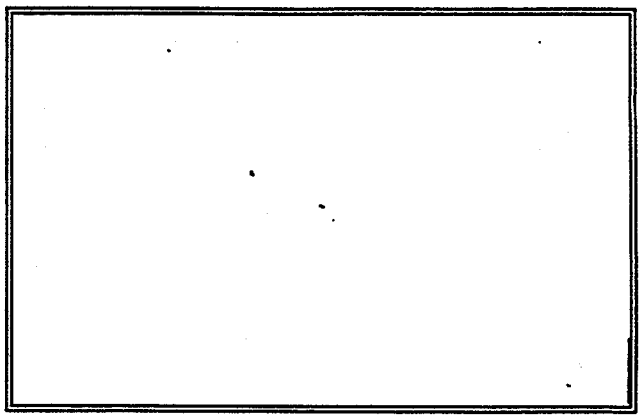

Fig. 5a. Photo of dislocation etch pits for the area at the edge of the subcell.

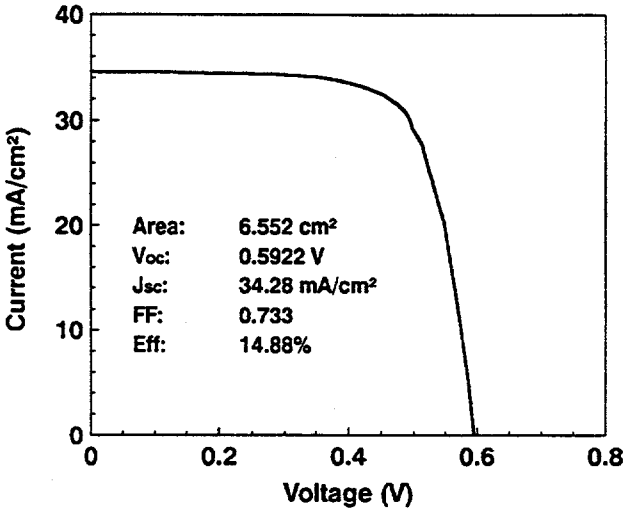

Fig. 5b. Current-voltage curve for edge subcell.

The subcell data can be used to more accurately study the dependence of solar cell performance on the slip dislocations. Figure 6 is a plot of cell efficiency versus dislocation density. (The cell efficiency for the subcell assumes an area that excludes the busbar coverage in the area calculation but includes the grid coverage.) Dislocation densities were taken from the areas at the center of each subcell, points 10-13 as shown on Fig. 1. Efficiencies drop below 14% for dislocation densities exceeding 500/cm^2 to 800/cm^2.

As described in previous work [4], reduced long wavelength quantum efficiency (QE) occurs for cells made from highly dislocated material. Thus, the correlation of long wavelength QE to the dislocation density and cell performance can be evaluated. Figure 7 plots the normalized QE at 900 nm versus the dislocation density for the subcells. (The QE data is normalized to the maximum QE value for each subcell in order to correct for variations in subcell optical reflectances.) Reduced QE at 900 nm correlates with increased dislocation density, providing a simpler criteria compared to dislocation etching for determining the presence of dislocations in solar cells.

Effective minority carrier diffusion lengths were calculated from the quantum efficiency data using standard spectral response equations. Figure 8 is a plot of the effective diffusion length (L) versus the dislocation density. For low dislocation levels, the diffusion length is approximately 250 to 300 μm, which is consistent with values measured on crystalline silicon solar cells in the past [4]. As expected, the diffusion length decreases as the dislocation density increases. Note that further study is necessary to establish if all of the dislocations are electrically active, thus, providing a direct correlation between the dislocation densities determined by etch pit studies and those inferred from minority carrier diffusion length measurements.

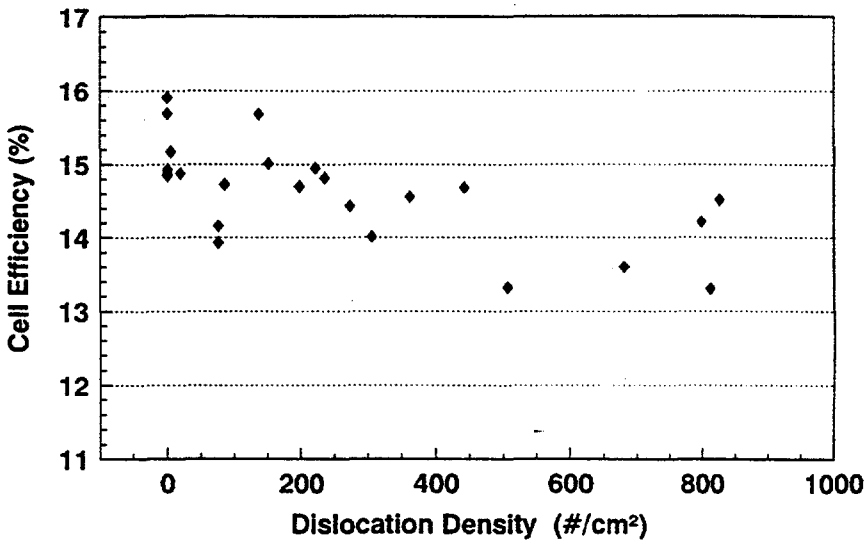

Fig. 6. Plot of cell efficiency as a function of dislocation density for subcells showing only gradual loss in efficiency as dislocation density increases.

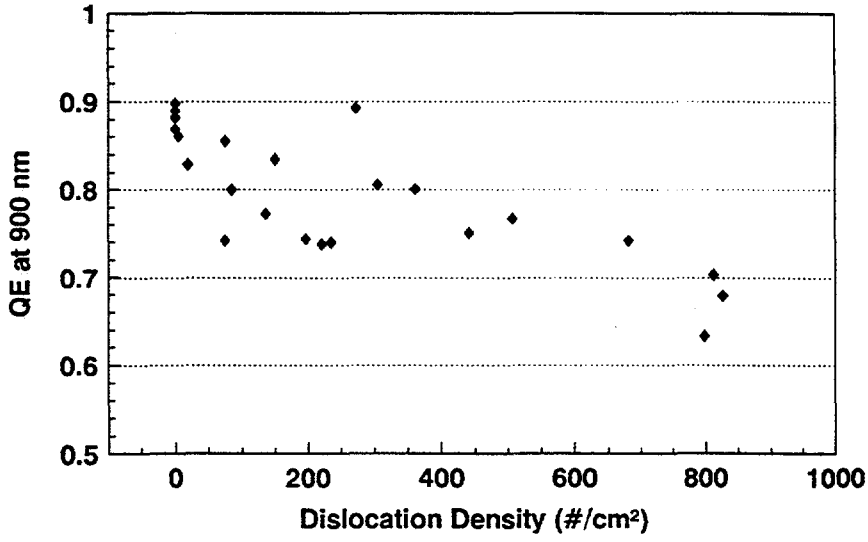

Fig. 7. Plot of normalized quantum efficiency at 900 nm as a function of dislocation density. Loss in response as dislocation density increases is attributed to increased recombination in the bulk.

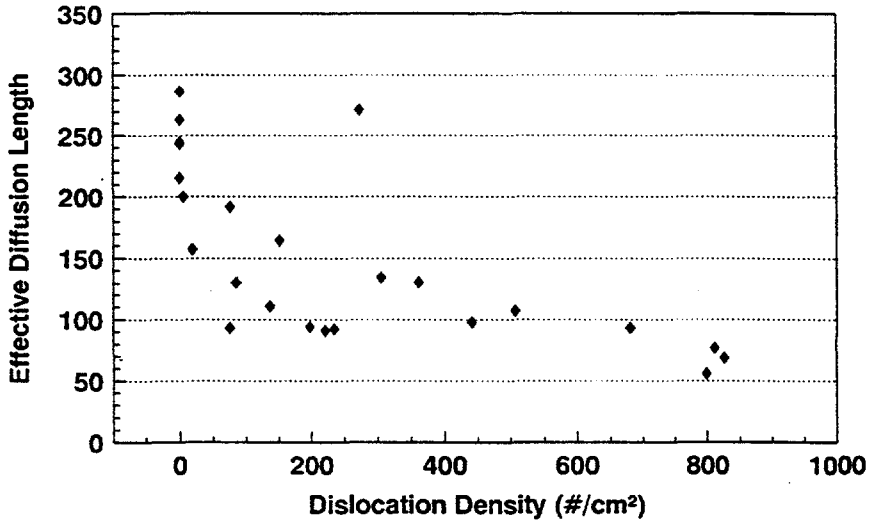

Fig. 8. Plot of effective diffusion length as a function of dislocation density.

CONCLUSIONS

A Si solar cell manufacturer must understand the relationships among processes, dislocations and cell performance in order to determine how to minimize performance and yield losses. A study of dislocation density and distribution as a function of cell performance indicates that solar cells are tolerant of dislocations densities up to the 500/cm^2 to 800/cm^2 range. Above these dislocation densities, the solar cell performance decreases due to reduced photocarrier collection from the bulk. In addition, improvements in wafer and cell processing have decreased the performance losses associated with dislocated material.

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[4] K. W. Mitchell et al., "Characterization of Commercial Single Crystal Si Technology", *10th European PV Solar Energy Conf.*, 1991, pp. 310-312.

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16. Abstract (Limit: 200 words)

This report describes work performed under a 3-year contract to demonstrate significant cost reductions and improvements in manufacturing technology. The work focused on near-term projects for implementation in the Siemens Solar Industries Czochralski (Cz) manufacturing facility in Camarillo, California. The work was undertaken to increase the commercial viability and volume of photovoltaic manufacturing by evaluating the most significant cost categories and then lowering the cost of each item through experimentation, materials refinement, and better industrial engineering. The initial phase of the program concentrated on the areas of crystal growth; wafer technology; and environmental, safety, and health issues.

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