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Silicon-Film™ Photovoltaic Manufacturing Technology

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Executive Summary

Introduction

AstroPower is in the second phase of a three year, phased effort to upgrade its facility to produce 1.22m^2 Silicon-Film™ PV modules with an output of 170 Wp. In this program AstroPower established a baseline capability for growth of Silicon-Film™ wafers by optimizing present equipment. Productivity improvements of the Silicon-Film™ machine have been accomplished during the second phase. Improvements have been made in solar cell performance while decreasing materials consumption, integrating and mechanizing the fabrication process for solar cells, and scaling-up solar cell and module equipment for fabricating larger cells. The key contract milestones during the second year's phase include the demonstration of wafer machine productivity rate of 1.3 MW/year with a material use efficiency of 85%, and demonstration of this capability on 225 cm^2 solar cells, and 675 cm^2 substrates.

Approach

The Silicon-Film™ Process is a method for fabricating solar cells by direct growth of a solar cell quality, polycrystalline silicon layer on a low-cost, supporting substrate. This process is designed to significantly reduce silicon cost while retaining the physical and power output characteristics of single crystal silicon. The focus for the Phase II PVMaT-2A project is improving process capability by increasing wafer machine productivity and developing methods for increasing solar cell performance.

Results

The results from the first phase of the project provided us with the direction for proceeding to the marketplace with a module based on a large 15 cm x 15 cm solar cell earlier than we had planned. This development is favorable to the continued manufacturing technology research of this project. We have continued to explore the boundary capabilities of the wafer machine and the associated solar cell fabrication and module assembly processes in order to capture all of the benefits of larger size solar cell products.

Modifications to a Silicon-Film machine were completed for achieving continuous feed Silicon Film fabrication, higher throughput and an improved thermal profile. Axial and transverse thermal profiles were modified to improve material quality. The new machine and associated fabrication process are being examined according to the following:

- effect of sheet speed on defect density and distribution
- effect of gas ambient on grain size and shape
- analysis of sheet uniformity (thickness, density, morphology)
- characterization of material quality to improve device performance of material.

Based on previous experience, we expect that the material grown in the newly modified SF3-M machine will produce higher quality material at higher production rates (1.6 MW/yr). The improved thermal profile and control is expected to provide optimal conditions for uniform physical (flat, thin, and uniform thickness sheets) and electrical properties (longer diffusion lengths, improved device performance).

Work continues on separating out effects due to impurities and effects due to defects. Analytical tools were developed for measuring area based response based on EBIC and LBIC methods. The Kauffman source for hydrogen ion implantation was used to map out the process space for Silicon-Film solar cell improvement.

Progress was made on improving short circuit current. Areas of focus have included the development of tools to quickly assess material quality, continued development of a hydrogen implantation process, increasing material quality on large area, high throughput of wafers, and study of potential processes for improvement of solar cell power output during solar cell fabrication. A method to improve current collection in a solar cell after contact formation is under development.

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Introduction

Project Overview

The goal of AstroPower's PVMaT-2A project is to develop an advanced, low cost manufacturing process for a new utility scale flat plate module based on thin active layers of polycrystalline silicon on a low cost substrate. This is called the Silicon-Film™ process. This new power module is based on a new large solar cell that is 675 cm^2 in area. Eighteen of these solar cells form a 170 watt module. Twelve of these modules form a 2 KW array. The module, array and solar cells have the features shown in Table 1. As an intermediate step a 225 cm^2 solar cell is being developed which can more rapidly be brought to the marketplace since it will require less fixturing changes in the solar cell fabrication process.

Table 1. Utility Scale Silicon-Film Product Features

Solar Cell Size	675	cm^2
Solar Cell Power	9.45	watts
Module Size	1.23	m^2
Module Power	170	watts
Array Power	2041	watts

The program has three components:

1. Development of a Silicon-Film™ wafer machine that is capable of manufacturing wafers that are 675 cm^2 in size with a total product cost reduction of 70%.

2. Development of an advanced solar cell manufacturing process that is capable of turning the Silicon-Film™ wafer into a 14% efficient solar cell.

3. Development of an advanced module design based on these large area, efficient silicon solar cells with an average power of 170 watts.

The completion of these three tasks will lead to a new power module which will be designed for utility and other power applications with a substantially lower cost. The module assembly labor cost is significantly reduced because only 18 solar cells are required for a 170 watt module in contrast to 36 solar cells for a 53 watt module.

Silicon Film Technology

The Silicon-Film™ Process is a method for fabricating solar cells by direct growth of a solar cell quality polycrystalline silicon layer on a low-cost, electrically conductive, supporting substrate. The Silicon-Film™ Process is designed to significantly reduce the silicon cost while retaining the physical and power output characteristics of single crystal silicon.

A drawing of a Silicon-Film™ solar cell is shown in Figure 1.

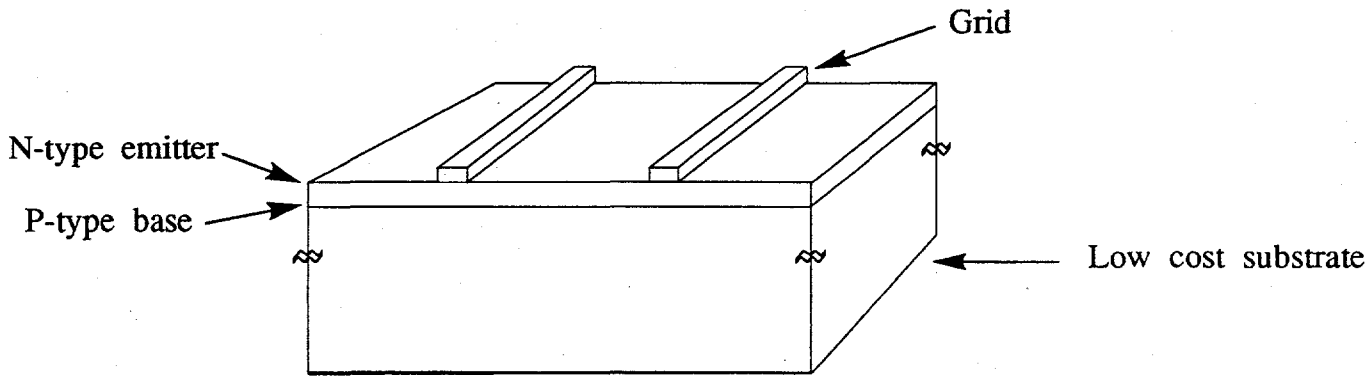


Figure 1. Silicon-Film™ solar cell.

Silicon cost is determined by silicon quality, wafer thickness, kerf loss during sawing and wafer breakage. With the Silicon-Film™ process, a reduction in silicon consumption and processing cost in wafer fabrication is achieved while maintaining the potential for solar energy conversion efficiencies as high as standard crystalline silicon wafers.

In the Silicon-Film™ process, cost reduction begins with designed-in limits on the consumption of costly high quality silicon. Additional reductions come from the elimination of most sawing steps, the use of thinner active silicon layers, a lower cost supporting substrate, and the utilization of high yield continuous manufacturing technology. The continuous manufacturing process produces the volume to reduce the per wafer cost of capital equipment and labor while improving process control.

The photovoltaic effect in Silicon-Film™ grown on a low cost, coated steel substrate was first observed at AstroPower in August 1984 [1]. The energy conversion efficiencies of these micro-sized devices (less than one square millimeter) increased to 9.6%, without an antireflection coating, by October 1985 [2]. Larger area devices were plagued by shunts which were eventually attributed to stress caused by the thermal expansion differences between the steel and the silicon. The impact of this stress was reduced by adding a fairly thick ceramic coating to the steel which led to a 12 square millimeter, 9.6% solar cell as measured by SERI in November 1986 [3]. This thick ceramic coating led to the abandonment of steel in favor of a thermal expansion matched ceramic in January 1987. One square centimeter, 10.2% efficient solar cells were measured by Sandia in June 1987 [4]. Continued development of this approach led to the achievement of a 15.7% Silicon-Film™ solar cell measured by Sandia in December 1988 [5]. All of the above results were achieved with active silicon layers approximately 100 microns thick. Light trapping was not employed for these initial solar cells.

A series of commercial-size, 100 cm^2 solar cells was measured by Sandia in September 1989 with a median efficiency of 10% [6]. These results led to a focus on the development of the Pilot Scale manufacturing machine. This Pilot Scale machine was operated for eight months in a batch mode, while the data was collected and the design rules were developed for the first manufacturing machine. Present material has demonstrated efficiencies in excess of 10%.

Expected efficiency improvements are based on the product development and optimization approach utilized at AstroPower. Following are the key steps:

1. Develop a process that yields an acceptable and reproducible morphology. The key material quality test is minority carrier diffusion length.

2. Demonstrate 25 mA/cm^2 in a 0.1 cm^2 structure with a diffusion length greater than 20 microns.

3. Improve voltage and fill factor through emitter and base doping and contact optimization.

4. Improve current through diffusion length improvement using phosphorus gettering and hydrogen passivation[7].

5. Maximize performance with the addition of surface passivation and grid optimization.

Figure 2 shows the progress that has been made with the development of Silicon-Film technology during the last five years. The key progress step that has been made during the course of this project has been the demonstration of a utility scale product.

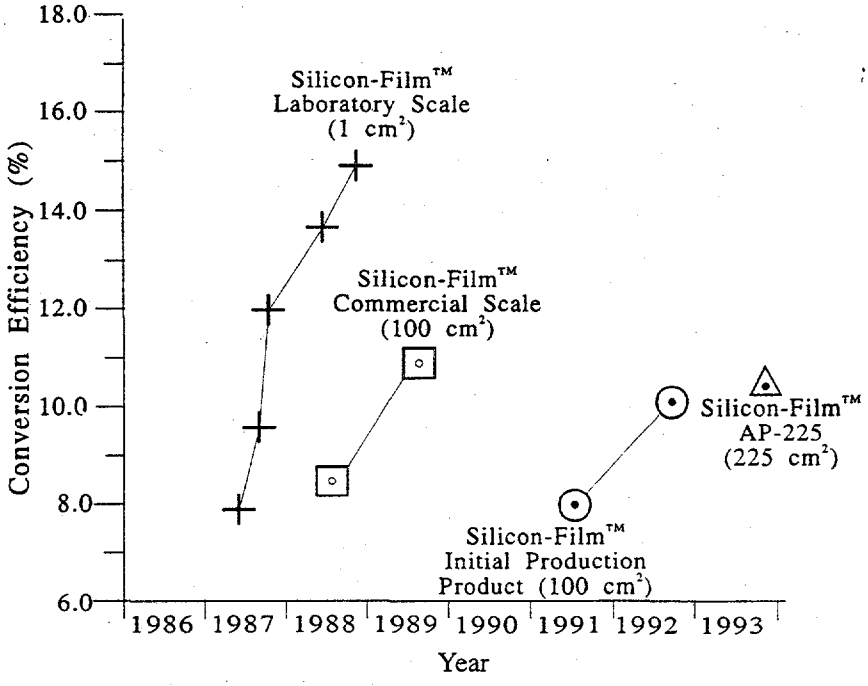


Figure 2. Progress in total area efficiency for Silicon-Film™ solar cells.

PVMaT Project Goals

AstroPower is upgrading its facility to produce 1.22 m^2 Silicon-Film photovoltaic modules with an output of 170 Wp. At a production rate of 19 MW/year a 70% cost benefit would be realized from the current level. AstroPower will work toward these goals by improving its manufacturing line. Table 2 shows the manufacturing technology milestones for the three phases of the project.

Table 2. Silicon-Film™ Manufacturing Technology Milestones*

Milestone	Phase I	Phase II	Phase III
Wafer Machine			
Production Rate	400 kW/yr	1.3 MW/yr	3.0 MW/yr
Material Use Efficiency	75%	85%	90%
Solar Cell Size	a) 10 cm x 10 cm b) 15 cm x 15 cm	b) 15 cm x 15 cm c) 15 cm x 45 cm	b) 15 cm x 15 cm c) 15 cm x 45 cm
Solar Cell Power	a) 1.1 watts	b) 2.5 watts	b) 3.1 watts
Module Power	--------	84 watts	170 watts

* Measured at AstroPower

Areas of focus that will enable meeting these goals include process improvements in wafer formation, solar cell fabrication and module assembly. Specifically, AstroPower will accelerate improvement in production rate and material quality of Silicon-Film fabrication machines; accelerate improvements in solar cell efficiency from 11% to 14%; and utilize large area solar cells and modules to improve parts handling efficiency. These efforts will significantly reduce materials and labor costs. In addition, AstroPower will establish the capability for increased production capacity by increasing wafer machine production rates; automating solar cell processing to accommodate larger wafers; and automating circuit formation to reduce labor costs. AstroPower will also assure that the processes developed for scale-up will minimize the generation of waste streams and minimize environmental impact.

Approach

During the first part of the second phase of the project, AstroPower addressed significant improvements to its wafer production process. Areas of focus included improving the productivity of the Silicon-Film machine. This effort began by modifying the film growth strategy to improve the material throughput and performance. This required a change in the Si-Film machine hardware. In addition, AstroPower worked to decrease module costs through the integration and mechanization of the fabrication process for cells and modules. Plans are being implemented to bring parts on-line for the fabrication of 225 cm^2 solar cells. The production capability of making a 36 solar cell module (as a 6 x 6) based on 225 cm^2 solar cells was brought on-line.

Key Results

This project has accelerated the advance of our technology as follows:

- led directly to the early introduction of 225 cm^2 Silicon-Film™ solar cell product.
- development of a continuous, 1.6 MW/yr wafer machine
- shift in strategy for layer growth
- shift in approach for application of energy for sheet growth process
- development of higher thermal conductivity setter to achieve greater sheet speed
- development of gaseous environment to improve sheet morphology
- improved thermal control of sheet process
- computer control of sheet process
- increase of minority carrier diffusion length from 6 - 10 to 15 -20 micron range
- installation of on-line capability to produce 0.94 m^2 modules

Wafer Machine Performance Benchmarks

Table 3 shows the accomplishments for wafer machine production rate in this project. The material production rate, Mr, is defined in detail and described in a later section. It is a direct measure of the productivity of the wafer machine in useful wafer area. The demonstrated machine rate, DMR, is a measure of the machine productivity in terms of useful silicon generated on a continuous operation basis in MW/year. We have met the project goals for this measure both for 225 cm^2 and for 600 cm^2 size substrates. For 225 cm2 substrates we have demonstrated a 2.3 watt solar cell. The substantial progress made during this phase has opened the way for early introduction of a large area solar cell product.

Table 3. Wafer Machine Production Rate, Progress and Achievements

Parameter	Jan. 1992 Pre-PVMaT	Sept. 1992	Nov. 1992		May 1993
Prod. Rate, m^2/hr	0.14	0.57	0.57	0.64	2.14
Cell area, cm^2	100	100	100	600	225
Power, watt[1]	0.68	0.97	1.10	4.9	2.3
Mach.rate, MW/yr	0.07	0.43	0.48	0.39	1.6

[1] Measured at AstroPower

Another key measure of progress is the Material Use Efficiency, which measures the yield of useful wafer product in terms of input silicon raw material. The goal for Phase II of this project is to demonstrate a material use efficiency of 85%. This goal will be addressed quantitatively during the second half of the Phase II project.

Solar Cell Efficiency Achievements

Figure 3 shows the current-voltage characteristics measured at AstroPower for a 2.3 watt 225 cm^2 Silicon-Film solar cell. The measurements were made at 25°C at an intensity of 100 mW/cm^2 with an AM1.5G spectrum. This solar cell demonstrates substantial progress in meeting our goals for high efficiency Silicon-Film solar cells.

Cell Parameters		
Voc	= 0.566	volts
Isc	= 5.622	amps
Vmp	= 0.454	volts
Imp	= 5.153	amps
Pmax	= 2.337	watts
ff	= 0.734	

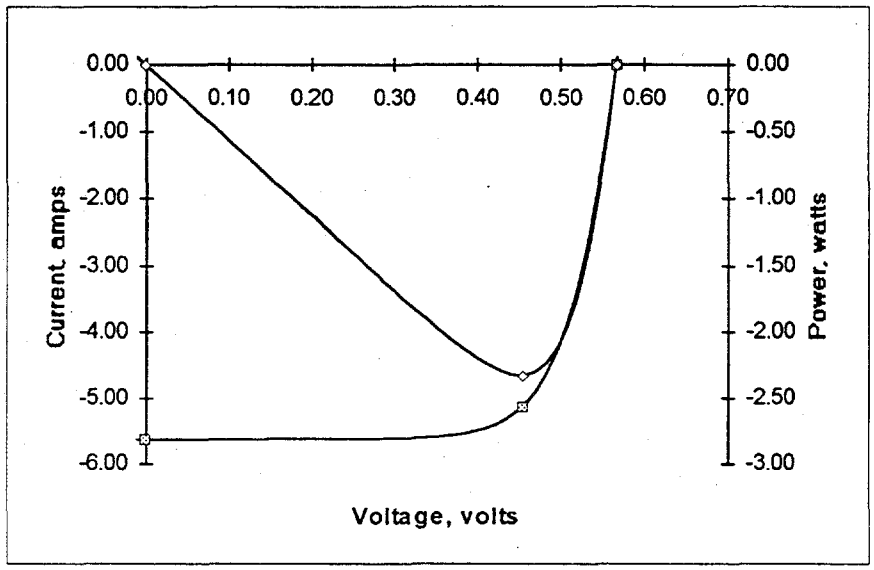


Figure 3. 2.3 watt, 15 cm x 15 cm Silicon-Film™ solar cell

Module Assembly Achievements

An important benchmark for Silicon-Film technology is the demonstration of modules assembled from strings of large area solar cells. During the first half of the Phase II project the capability of fabricating 36 solar cell (as 6 x 6) based on 225 cm^2 wafers has been successfully demonstrated.

Wafer Manufacturing Process Development

Wafer Machine and Process Development

Process Capability

The wafer fabrication process has been modified to improve the rate of material production and improve the material quality. The machine production rate has been increased by increasing the sheet width and the linear sheet speed; the goal is to demonstrate a 1.3 MW/yr production rate. A material generation rate of 2.1 MW/yr has been achieved; the machine is being optimized at 1.6 MW/yr, and the material quality is presently being assessed. The material quality has been improved by modifying sheet growth thermal profiles to reduce stress in the active silicon layer, and by introducing an hydrogen implant process using a Kauffman source.

The size of the present production wafer is a nominal 15 cm x 15 cm. The machine is presently running at a total structure thickness of 700 microns. Modification to the sizing of the starting material is necessary to achieve thinner layers; and experiments are in progress to determine the proper value of this input material attribute.

Wafer flatness, surface morphology, cross sections and mesa current densities are the attributes being employed to assess the material quality. Wafer flatness and acceptable surface morphology have been independently achieved. Simultaneous achievement of these attributes has required modifications to the axial and transverse thermal profiles in the wafer machine. We have achieved current densities equal to those measured when the machine rate was 0.3 - 0.5 MW/yr as reported during Phase 1.

Wafer Formation Process

The process steps employed to fabricate Si-Film Product I wafers are given in Table 4. The as-received materials employed in the substrate are in bulk form. These materials are sized and suitably classified using a milling procedure. The size of the granular material is a critical parameter. The silicon material is doped using a granular doping source.

Table 4. Wafer Formation Process Sequence

	Process Step
1)	Substrate preparation
2)	Active Layer Application
3)	Active Layer Growth
4)	Wafer Separation
5)	Wafer Sizing

A setter is used as a support apparatus for the transportation of the substrate material through the active layer application and growth process. The materials are applied to the setter in granular form. The setters are deployed in a manner that permits the continuous growth of the active layer. The length of the Si-Film sheet is unlimited with the present equipment design.

Wafer Machine Rate Calculation

The machine rate goal for Phase 2 of the project is to demonstrate a production rate of 1.3 MW/year for 675 cm^2 wafers. We have demonstrated this production rate for 225 cm^2 wafers, and have been running at this rate on the current demonstration machine effective 5/1/93. Figure 4 illustrates the geometry for a Silicon-Film sheet on the setter. The demonstration is based on the following assumptions and measurements. The demonstration machine rate is the product of the following set of factors: the areal machine growth rate, Mr, in m^2/hr, the number of operating hours per year, N_o, and the solar cell efficiency, Eff.

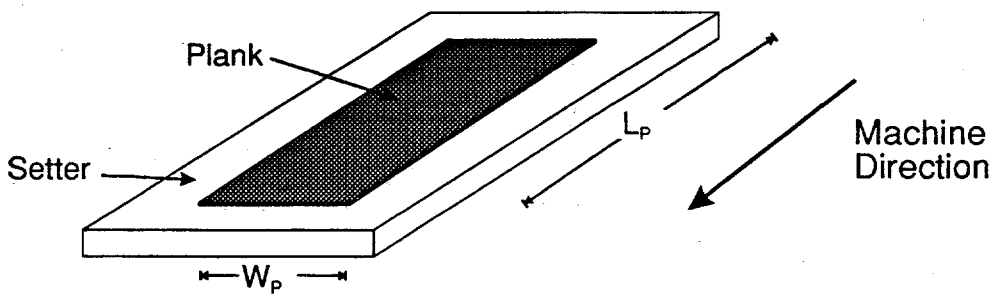


Figure 4. Sheet geometry.

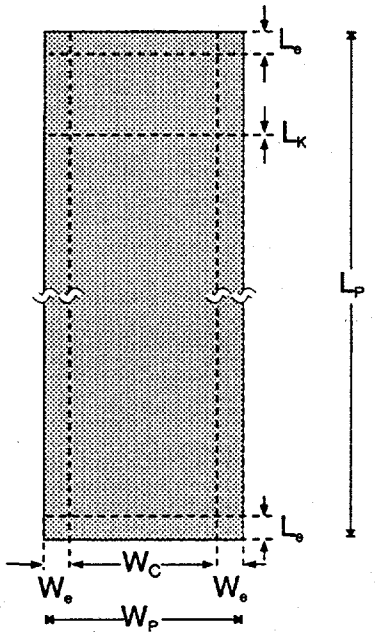
The equation for the definition of the demonstration machine rate is:

$$DMR = Mr * N_0 * Eff * 10^{-5},$$

where

DMR	=	the demonstration machine rate, MW/year
Mr	=	machine rate m^2/hr
N_0	=	number of production hours per year
Eff	=	resultant solar cell efficiency, %.

The present wafer fabrication process is running at an areal generation rate of 2.1 m^2/hour run. A solar cell efficiency of 10% is assumed (solar cell efficiencies in excess of 8% have been achieved with an unoptimized solar cell process at this process rate). The number of hours per year is assumed to be 8000 hrs/yr, based on continuous operation of the machine. Under these assumptions and measured values we obtain a machine rate of 1.6 MW/yr. The areal generation rate is based on finished wafer area generated per hour as shown in Figure 5.



L_n = length of sheet
W_n = width of sheet
N = number of wafers possible from sheet
L_e = edge length
W_e = edge width
L_k = saw kerf
L_c = length of cell
W_c = width of cell

Figure 5. Measurement of machine rate.

Machine Development

An analysis is being carried out to identify the critical parameters required to specify the design for the wafer machine building block. The wafer machine building block is the basic unit of production for the wafer formation process. A goal of the project is to choose the optimal building block size at each stage of process and material development. The analysis will be used to generate a model to guide the design of advanced wafer machines. The model is being tested on the present systems now in operation. These systems employ two different energy application strategies that are accounted for in the modeling. The model will generate the design parameters based on the desired sheet speed, active layer thickness and annealing profile. The model will generate the geometric and power application design parameters based on the desired sheet speed, active layer thickness and annealing profile.

One of the major areas of wafer machine and process progress has been the development of a higher thermal conductivity setter and an improved process gas environment. The higher thermal conductivity setter has been introduced to modify the growth habit of the sheet as a means to increase sheet speed. The change in gas composition has led to an improvement in the electrical properties of the sheet material.

The development of a higher thermal conductivity setter necessitated relatively extensive modifications to the thermal environment in the pre-heat, melt and growth zones of the wafer furnace. A simple heat transfer model has been used to assist in the design of immediate modifications, and will serve, along with the results gleaned from the immediate changes, as the basis for the design and construction of a fully continuous wafer machine during the present contract.

Continuous Feed Design

Previous Silicon-Film machine versions had a chain drive transport which led to speed inconsistencies in material transport, vibration of material during crystal growth, and transport failures leading to extensive repairs and lengthy periods of down-time. As a result, material quality at high speeds was unacceptably low. The modifications completed in May focused on achieving:

- continuous and smooth material feed and transport,
- a low maintenance transport mechanism,
- a longer, more thermally uniform liquid zone, and
- the incorporation of a high thermal conductivity setter

All previous versions were batch feed designs. The SF3-M system has demonstrated the desired transport properties of smooth material feed and transport and is in the process of being qualified for up to 4 hours of continual operation. Hours of operation will be extended once the machine and grown material have been fully optimized and qualified.

Improved Thermal Profile

Improved thermal control leading to optimal physical properties (no warping, minimal stress) and electrical properties at higher material production rates was our motivation. The thermal profile of a Silicon-Film wafer machine must be optimally controlled in the "X" (along length of machine and silicon sheet), "Y" (along width of machine and material) and "Z" (along cross-section of material) directions. These directions are illustrated in Figure 6.

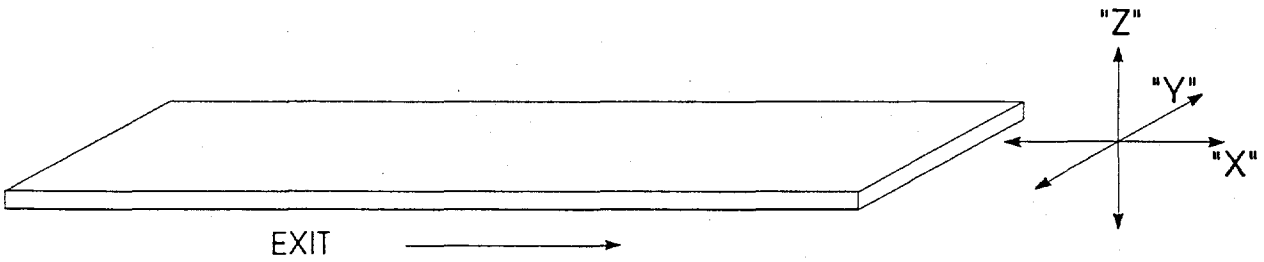


Figure 6. Reference for X, Y, Z Orientations of Silicon-Film Sheet (and Machine).

The new modifications to the Silicon-Film machine have resulted in a new thermal profile along both the "X" and "Z" directions. This profile has an extended liquid zone, thermal control in the "Z" direction, and provides an anneal zone which offers an improved thermal cooling profile from the freeze zone to the sheet exit. Figure 7 is a schematic illustrating the general shape of the "X" thermal profile of the newly modified Silicon-Film machine.

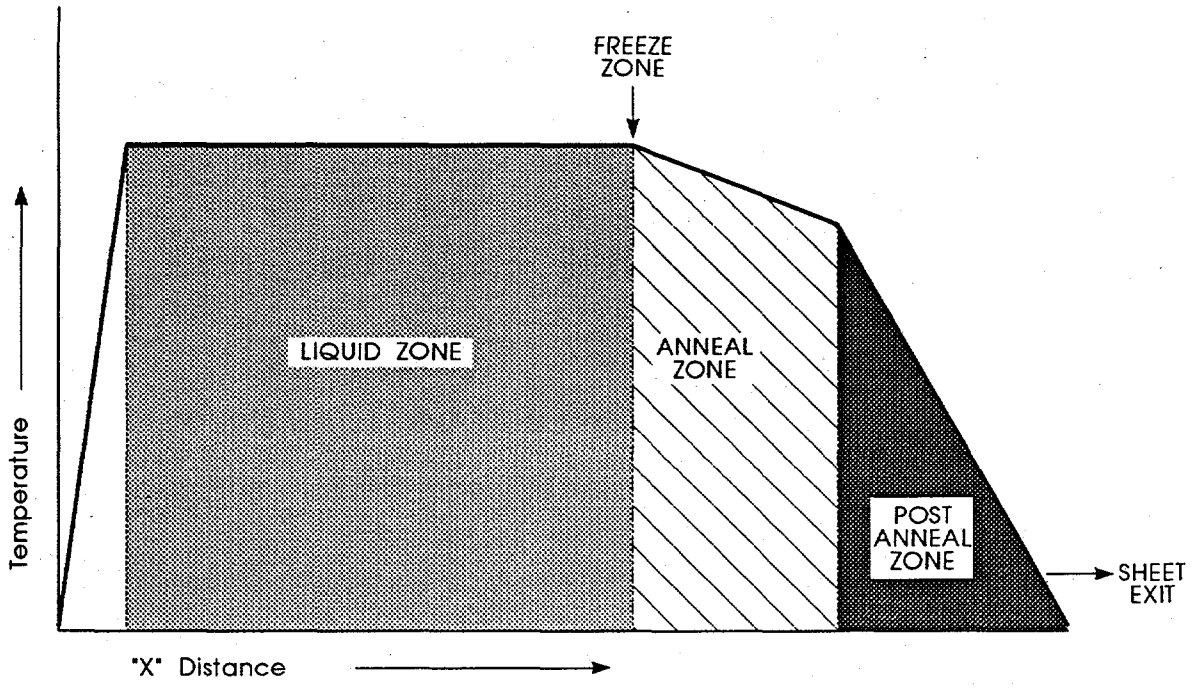


Figure 7. Shape of Thermal Profile Along Length ("X" Direction) of SF3-M Machine.

A primary effort of wafer quality improvement focused on the annealing profile of the grown sheet as a path to achieve improved minority carrier diffusion length of material grown at a 1.6 MW/year throughput rate. Additional focus has been on optimizing growth parameters of gas mixture and flow, the thermal profile in the "Z" direction, and improving instrumentation to enhance monitoring and control of thermal profiles. The gas ambient mixture appears to be a critical parameter in achieving smooth, large grain material.

Process Control

Raw Materials

There are several ways that the presence of chemical impurities can deleteriously affect the quality of the material. The impurity may introduce an energy level in the vicinity of the midgap where it acts as a minority carrier trap, reducing minority carrier diffusion length. Alternatively, the impurity may introduce an energy level in the vicinity close to the conduction-band or the valence-band where it may act as an donor or acceptor, respectively , thereby controlling the conductivity of the material. The nature of the energy level introduced by the impurity is dependent on its location within the lattice (as a substitutional or interstitial). Furthermore, some impurities are subject to removal, or deactivation, as the consequence of subsequent processing, for example by gettering or hydrogen passivation. Impurities may also interact with structural defects, or cause structural defects by precipitation. Recent developments employing hydrogenation of Si-Film material have led to significant improvements in device performance, and will be discussed in a later section.

There are two sources of impurities, and owing to the method of growth, a means for purifying the material during sheet growth. The two sources of impurities in the final sheet material are those introduced with the starting material, and those introduced from the growth system during layer growth.

In collaboration with the Dow Chemical Company, a detailed chemical impurity analysis of the Silicon Film process was performed. The ICP techniques were the method of choice for analysis of incoming Silicon-Film raw materials, however detection limits may not be adequate for resolving electrically active impurities in the grown wafers. To complement the ICP data, wafer samples were sent to an outside vendor for SIMS profiling.

Most of the metallic impurities appear to be coming in with the current supply of silicon (Fe, Ti, W, Cr, Ni). Some impurities are added in the material preparation process (Al, Ba, Ca, Mg, Sr). These impurities correlate well with expected contaminants. However, they are expected to cause minimal photovoltaic degradation, since they are probably tied up as relatively benign alumina inclusions after wafer formation. The material application process steps do not add significant impurities.

The distribution of the impurities in the finished active layer was investigated. Results from SIMS depth profiling of our as-grown Silicon-Film wafers, performed by an outside vendor through the Dow Chemical Company, indicate evidence for concentration of several transition metals to the top surface of the wafer, as expected because of segregation during crystal growth.

Environment

In cooperation with the Dow Chemical Co., an on-line gas chromatograph was installed as an in-situ atmospheric monitor servicing both Silicon-Film machines. The GC is sensitive to N_2, O_2, CO_2, CO, and H_2. Separation is accomplished by a chromatographic retention column. Detection is accomplished by measuring a thermal conductivity difference between the gases sampled from the wafer machine atmosphere and the argon reference gas. This technique is not sensitive to water vapor because water is too strongly absorbed by the column due to its highly polar nature. Moisture content will continue to be monitored with a porous alumina capacitive sensor, a technique which has proven to be sensitive down to at least 10 ppm. Silicon oxides are the only other gaseous species expected to be important in the growth zone. Unfortunately, since GC detection requires cooling of the process gas sample to near room temperature before analysis, gaseous silicon oxides are fully condensed, and hence not detected. These techniques have proven useful for monitoring the process gas environment during operation, and for controlling initiation of product growth.

A change in the process gas used during sheet growth has led to larger grains in the material and the achievement of minority carrier diffusion lengths of 19 microns. Process gases employed during the sheet growth are to inhibit the deleterious effects of oxygen on furnace components and the forming sheet, and to sweep away volatiles generated during the growth process. It has been found that the introduction of more reactive gases changes the growth habit of the sheet material resulting in larger grains.

Thermal Control

A new approach for improving process control by the measurement of temperature using optical pyrometry is now being developed. Optical pyrometry can now be employed with the expectation of reproducible output. Optical pyrometry can be an accurate method for measuring temperature. The accuracy of the method depends on knowledge of the precise values of emissivity of the material being measured. The emissivity of a material is quite sensitive to the presence of surface layers (e.g. oxides), and typically has a spectral dependence as well.

Linear Speed

Linear speeds in the range of 5 to 30 cm/min were explored during the period. No significant correlation between speed and short circuit current density or minority carrier diffusion length was observed.

Wafer Quality Improvement

Impurities

A set of samples comparing our current baseline wafer process to a potentially cleaner, higher performance process was sent to the Dow Chemical Co. for ICP-MS/OES chemical analysis. The sample set compared raw materials, as-grown wafers, and post-diffusion wafers for the production Silicon-Film process and a new higher current density process. The blank levels were improved in comparison to the previous analysis. Unfortunately, the impurity levels in the float zone control wafer were still high.

The ICP-OES analysis of an SEH Float Zone Wafer, ppb above blank, is shown in Table 5.

Table 5. Elemental Analysis of SEH Float Zone Wafer

Element	ppb	Element	ppb
V	81	Cd	63
Mo	0	Co	0
Al	715	Ni	50
Zn	117	Mn	3
Cu	0	Fe	238
Ti	24	Cr	25

Since it is unlikely that the SEH float zone wafer contains these high impurity levels, we suspect some type of systematic contamination is occurring: airborne contamination, contamination from sample containers, or contamination during sample crushing/acid dissolution. Surprisingly, a semiconductor-grade polysilicon sample showed much lower impurity levels that any of the wafer samples, including the SEH FZ wafer.

The Dow Chemical Analytical Group also used neutron activation analysis to test this sample set for Au, Mo, Pd, Pt, Ta, W, In, V. No elements were detected above the detection limits for any of the samples in this set. Detection limits were 0.1 ppb for Au, 10 ppb for W, 5 ppb for V, and 100 ppb for the other elements.

We are continuing to investigate adding a resistivity monitor to control the quality of the incoming active layer silicon materials. We have been able to establish a definite correlation between silicon resistivity and wafer performance. This correlation is used as a pass/fail monitor for wafer quality. At the same time, we are investigating potential impurity sources causing resistivity variability.

Defects

In collaboration with NREL, unpassivated, unhydrogenated Silicon-Film wafers were analyzed by EBIC. The results showed up to 50% degradation of the base-line current at the grain boundaries, but since grain size is relatively large, this alone cannot account for our relatively low average minority carrier diffusion lengths. Inter- and intra-grain response was very uniform. Since dislocation density is known to be highly variable grain to grain, this evidence suggests dislocations are not the primary limitation to diffusion length. Further studies are planned, including EBIC correlation to defect maps, EBIC before and after hydrogenation, and EBIC in cross-section.

We have upgraded our Amray 1200 SEM and purchased a current amplifier to give us in-house EBIC capability. With a combination of high resolution and relatively rapid analysis time, we have found EBIC to be an extremely powerful characterization tool for analysis of defects and spatial uniformity in Silicon-Film wafers. Special thanks to Rick Matson of NREL, who provided us with excellent technical assistance. His advice and input helped us to develop this EBIC system quickly, and at relatively low-cost.

We continued work to automate the defect counting procedure. An adapter was fabricated to connect a video camera to an in-house microscope. Frame grabbing software was used to obtain good, high contrast images of defect etched specimens.

Low short circuit current, Jsc, continues to be the major limitation to Silicon-Film efficiency. EBIC is a characterization tool which can help improve Jsc by determining the relative degradation caused by various recombination centers, such as grain boundaries, thermal-stress induced defects, precipitates, voids, and inclusions. The following is a summary of EBIC characterization work completed to date on several Silicon-Film wafers:

SF2 #1938. Material Source A, Linear speed A. The two micrographs in Figure 8 show the same 0.2 cm^2 mesa (after Kaufman H+) in EBIC and normal SEM modes, respectively. The electrically active grain size can be clearly seen in the EBIC photo. Although the grain size is relatively small, the inter-grain electrical response is surprising uniform, consistent with this mesa's relatively good electrical performance (Voc = 502 mV, Jsc = 15.5 mA/cm^2).

SF3 #494. Material Source B, Linear Speed B. Under normal microscopy this mesa appeared to be large grained and defect free. The left photo, Figure 9A, is a micrograph of an entire mesa in EBIC mode. Numerous large dark spots are seen, indicating areas of very low current response, and consistent with the relatively low Jsc of this mesa (13.5 mA/cm^2). Under high magnification, these areas can be easily identified as dislocation networks. These dislocation networks were previously identified by defect etching (Secco etch), but this is the first, direct confirmation of the detrimental, high electrical activity of these defects.

SF3 #522. Material Source C, Linear Speed C. The EBIC micrograph, Figure 10, shows relatively high current response over most of the mesa consistent with the high Jsc, (16.6 mA/cm^2), but a large void, shown in a higher magnification SEM micrograph, Figure 3B, is probably responsible for shunting and the low Voc, (474 mV).

The Product I solar cell electrical performance has been found to be well correlated with the electrically active defects found by EBIC. Identification of these defects has already led to postulation of their mechanisms of formation, and to proposed process improvements to eliminate them. It takes about 10-15 minutes to prepare a solar cell sample and generate an EBIC micrograph. The combination of high resolution and short analysis time makes EBIC the method of choice for analysis of electrically active defects in Silicon-Film solar cells.

The EBIC technique can also be used to study other important solar cell processes, such as hydrogen passivation of defects, surface and grain boundary recombination velocities, and minority carrier diffusion lengths. EBIC will be a good, complementary match with LBIC analysis.

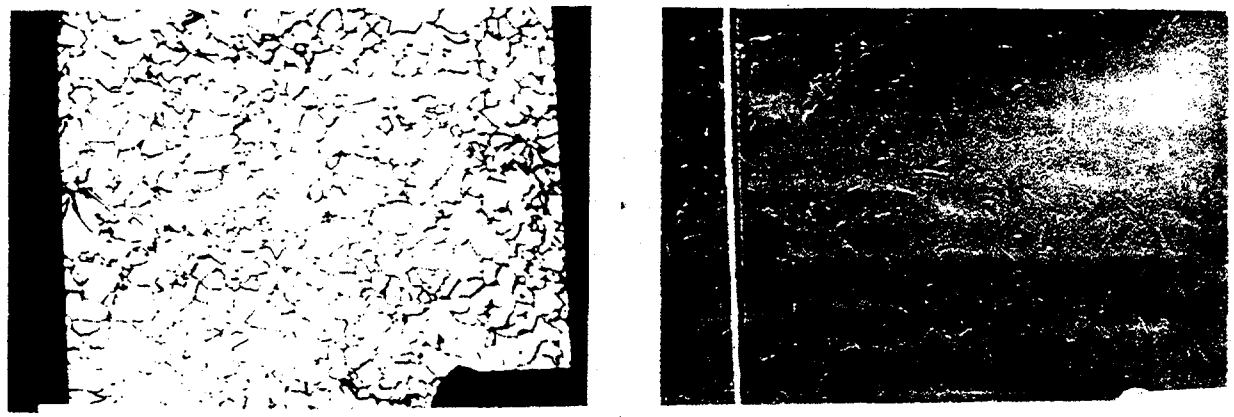


Figure 8. Comparison of EBIC and SEM imaging on Sample SF2 #1938
A. EBIC 20X, B. SEM 20X

Figure 9. Dislocation network shown by EBIC on Sample SF3 #494
A. low magnification, B. High magnification

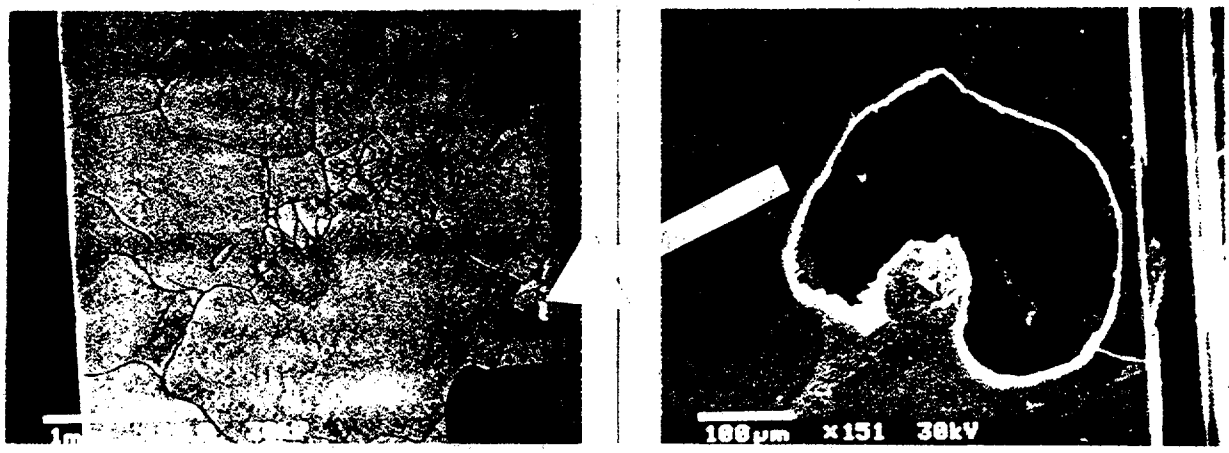


Figure 10. Identification of a void using EBIC method on sample SF3 # 522
A. EBIC 20 X, B. SEM 151 X

Point Defects

After low short circuit current, the next major limitation to the performance of recent high speed Silicon-Film wafers appears to be point shunts.

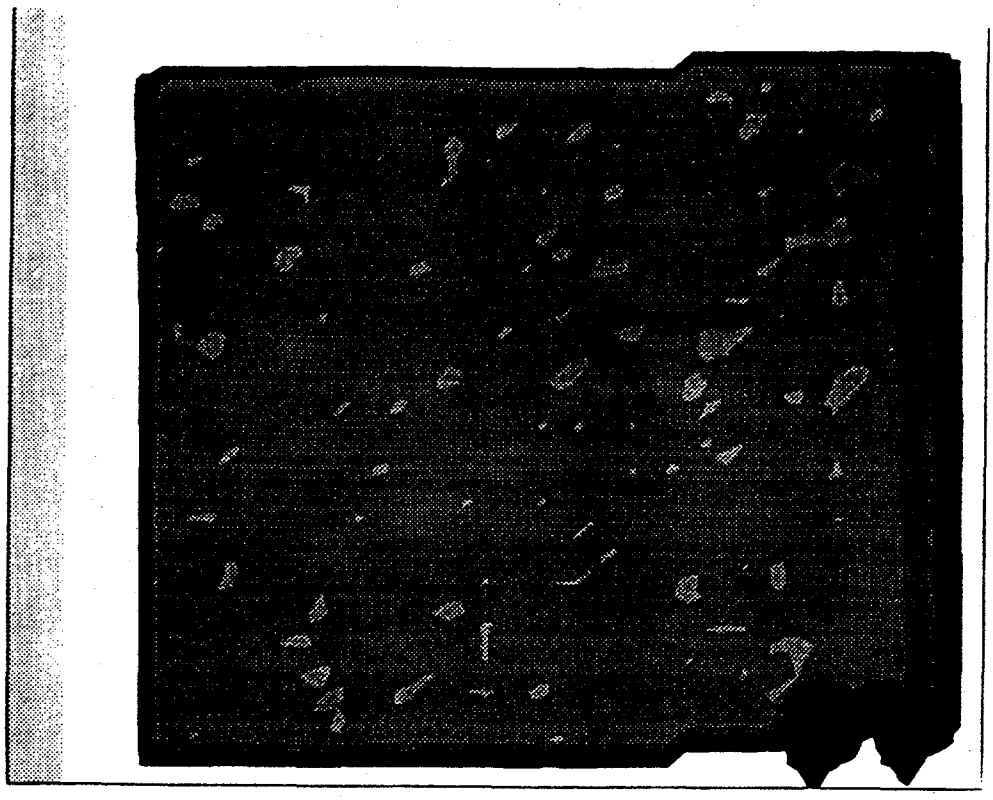
The new LBIC system was employed to conduct a preliminary analysis of these shunts. LBIC maps for two mesas from SF2 Run # 2140 were generated using the 633 nm HeNe laser to raster scan a 50 x 50 array (4 mil step size) over the 0.2 cm^2 sawed mesa devices.

The first mesa scanned was a mesa with high shunt resistance. The resultant map, in Figure 11, shows relatively uniform LBIC response, with current variation only about ± 10%, (±10% is equivalent to one gray-scale color). Lighter areas are regions of highest current response. Probe shading is seen in the lower right hand corner.

The next mesa scanned was a severely shunted device. Near the center of the map, in Figure 12, a small hole can be seen, minus 2 gray-scale colors, ~ 25% LBIC signal reduction. This area is a suspected point shunt.

Next, the shunted mesa was diced into two halves. The top half was LBIC scanned again to verify that the defect was located in this half, which it was. The two half mesas were then tested in the IV light tower. The top half, the half with the defect, showed considerably worse electrical performance than the original whole mesa. The bottom half showed dramatic improvement in Voc, shunt resistance, and Jsc, as shown in the figures.

Examination of the sample under an optical microscope showed a small pit in the vicinity of the mapped shunt. However, numerous pits are also present in adjacent non-shunted mesas. We conclude that pits are not always active electrical shunts.



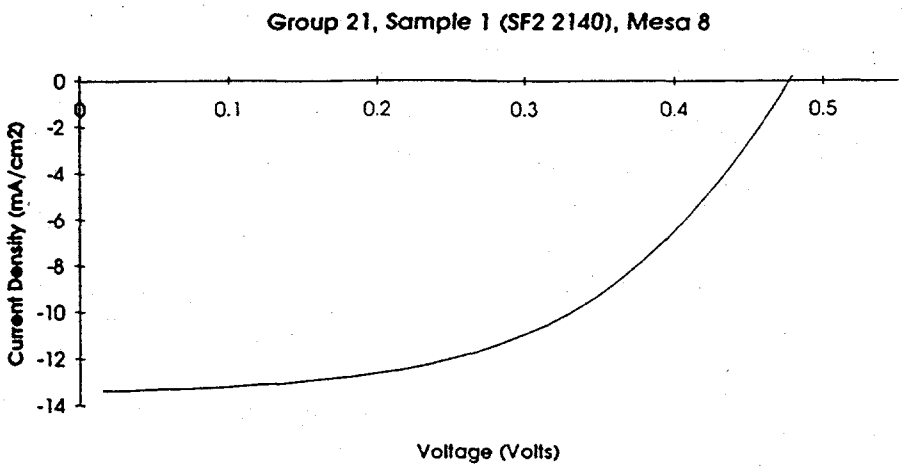
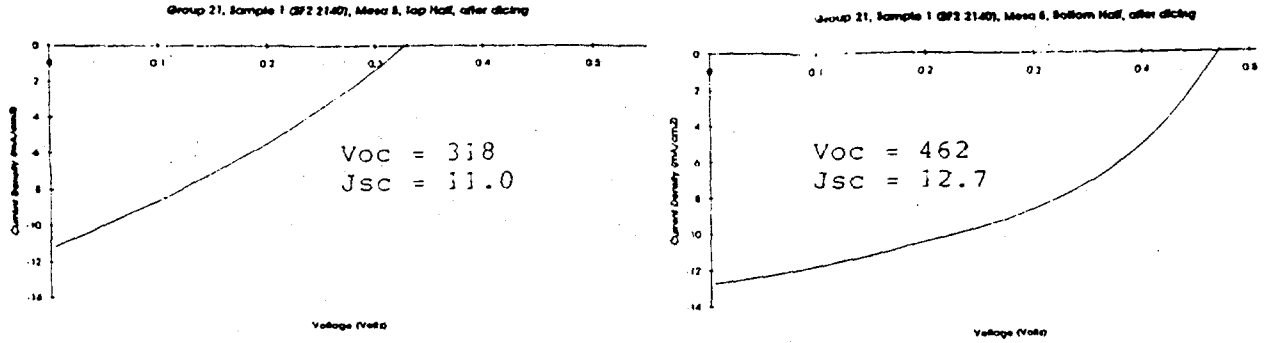
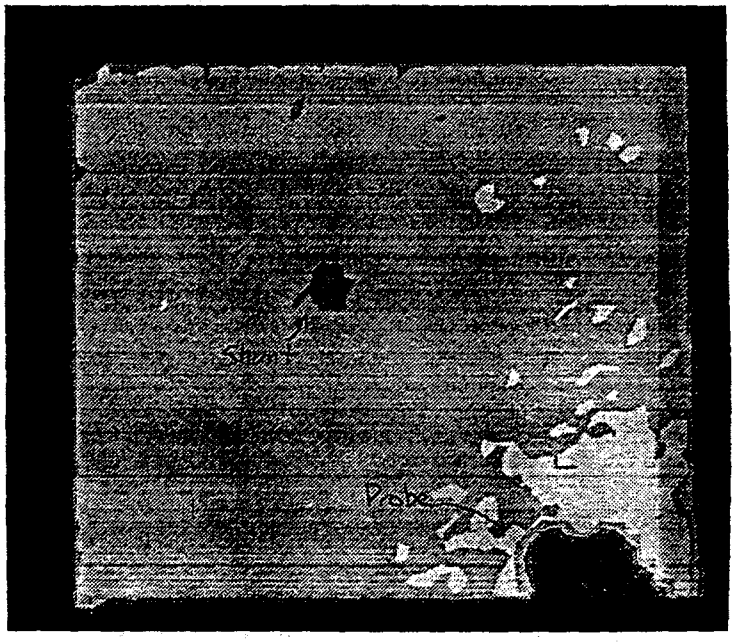


Figure 11. LBIC scan and I-V curve of a uniform Silicon-Film mesa device

(c)



(a)



(b)

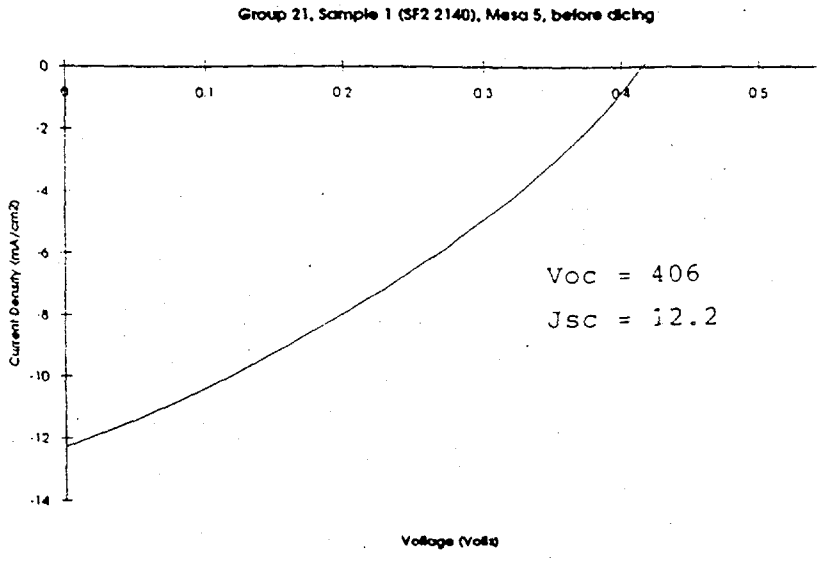


Figure 12. LBIC scan (a) and I-V curve of a Silicon-Film mesa device with shunt, before (b) and after (c) cutting in half

Spatial Uniformity

Initial maps of mesa devices have been generated. Figure 13 shows a sample spatial map and line scan of a Silicon-Film 0.2 cm^2 mesa diode using a 633 nm He-Ne laser light beam source. We observed significant spatial variation in the output signal. Although we are still attempting to correlate spectral response data to regions of high and low LBIC response, we are confident that this spatial variation is a real device effect, and not a testing artifact. In addition to testing more devices and investigating the causes of spatial variation, we are planning to extend this technique to larger area devices. We are also installing longer wavelength laser light sources.

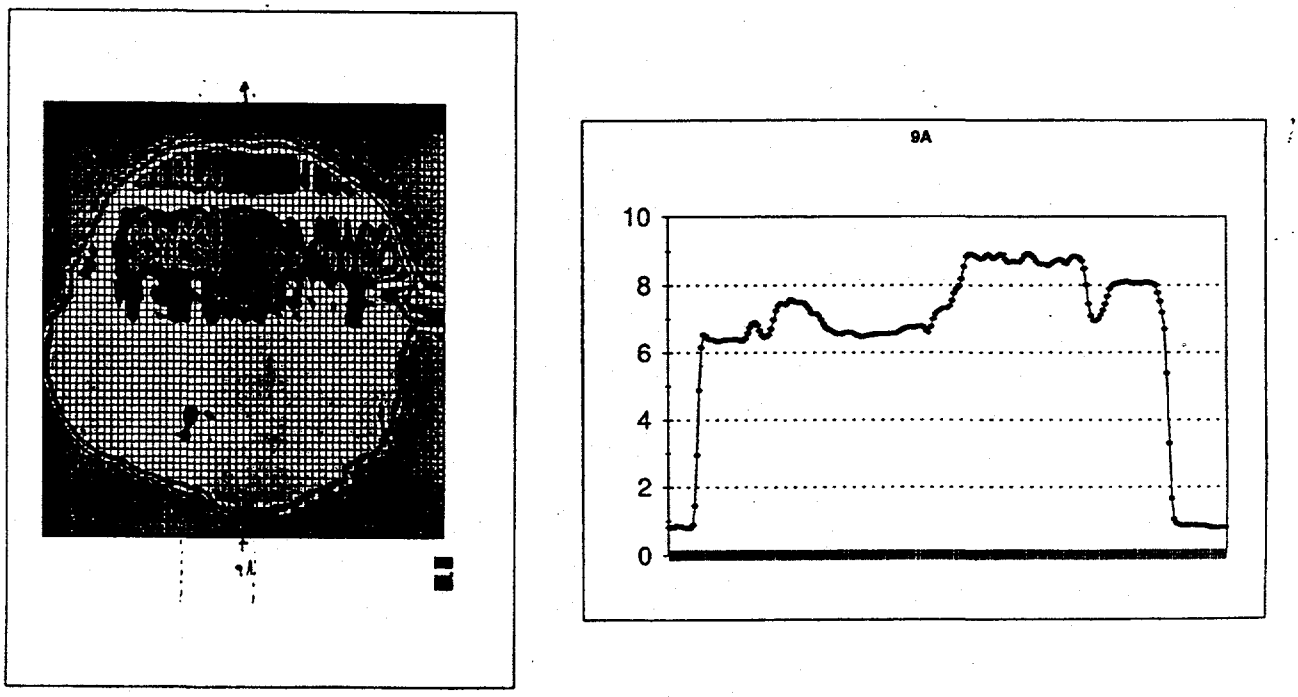


Figure 13. LBIC response for Silicon-Film mesa

Wafer material with an electrically active grain size of 228 microns, (as determined by EBIC - see attached micrograph in Figure 14), was generated in the SF3 wafer machine. This represents an approximate 2X increase in grain size from our baseline process. This material was fabricated into 0.2 cm^2 solar cell mesa devices. Table 6 shows the measured device parameters and sample sizes, (no anti-reflection coating). Diffusion length was obtained from spectral response data.

Table 6. Device Parameters for Mesa Diodes

Sample	n	Mean Jsc (mA/cm^2)	n	Mean Ln (microns)
SF3 Run #537a*	16	17.2	9	19.3
SF3 Run #537b**	7	16.0	4	11.9

Notes:

* Light gettering diffusion (100 ohm/sq), etch-back, second diffusion to 40-50 ohm/sq.

** Sister sample to 573a, single diffusion to 55-65 ohm/sq.

*** Both samples received Kauffman hydrogenation prior to testing

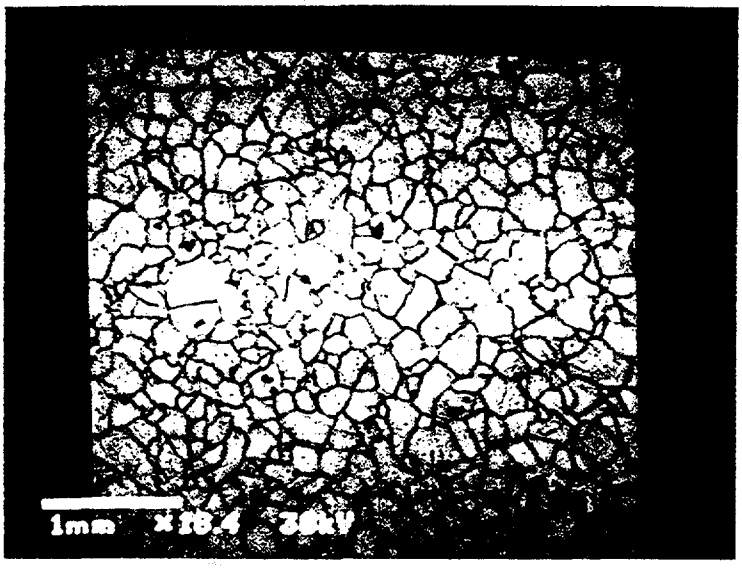
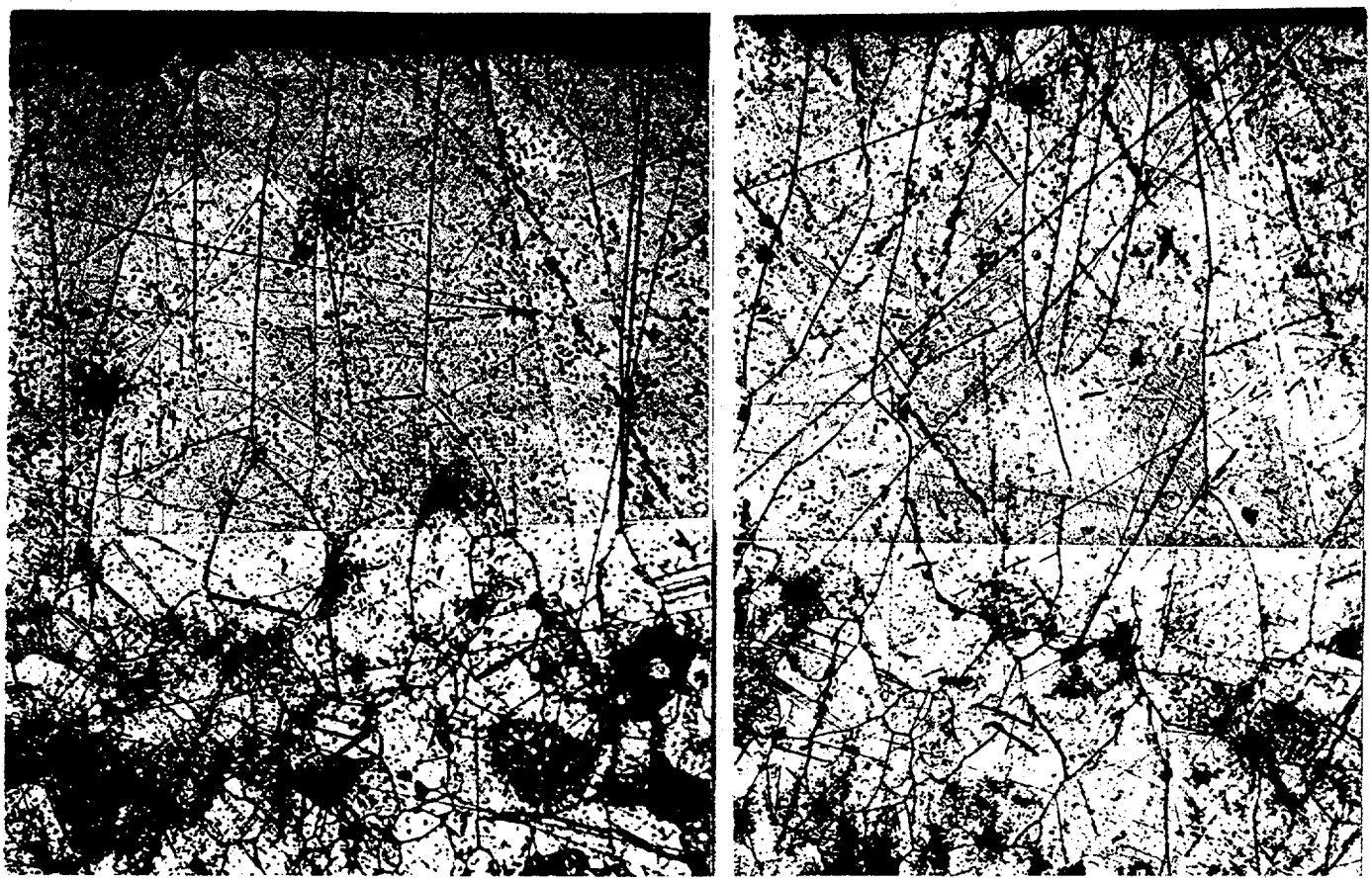


Figure 14. EBIC micrograph of Silicon-Film mesa, showing average grain size of 228 micrometers

Material grown from the newly modified SF3-M machine was analyzed by optical microscopy and defect etching. Figure 15 shows photomicrographs of the XZ plane and YZ plane cross-sections of a Silicon-Film sheet grown at 15 cm/min. The cross-sections were etched for 2 minutes in SECCO etchant to discern defects. We are currently analyzing cross-sections such as these to determine if there is a correlation between sheet speed and defect density and distribution.



(a) Cross-Section in XZ Plane **(b) Cross-Section in YZ Plane**

Figure 15. Photomicrographs of cross-sections of Silicon Film active layers after treatment with a defect etchant.

We expect that the columnar nature of these grains and the new, more optimal thermal profile of the SF3-M machine will lead to longer diffusion length material and higher performance solar cells. Mesa devices will be evaluated during June to determine the effect of the machine modifications on material quality as measured by device performance and diffusion length. EBIC will be used to identify electrically active defects and determine their level of degradation as compared to material grown at slower speeds.

Residual Stress

Development continues on an in-house circular polariscope for residual stress measurement.

Solar Cell Process Development

Baseline Process

Key efforts were completed early in the Phase II program to obtain an updated baseline process. This new baseline process was required to optimize the performance of material being grown. The efforts were to optimize front contact firing conditions and to examine the benefits of the diffusion/gettering process. As part of a program to optimize device performance, an engineering lot of 20 106 cm^2 wafers was sent on for solar cell processing, after the wafer quality had been carefully established using our short mesa loop. The mean power for the lot was 0.963 watts. This was a new record for a Silicon-Film lot of this size.

Front Contact Print/Fire Optimization

Extensive trials were conducted to determine the appropriate firing conditions for different weight ranges of solar cells. Optimal firing conditions were found for the complete range of incoming wafer weights.

Deep Diffusion Gettering

Experiments were conducted to determine the value of the following process steps which had been employed in the previous baseline after surface preparation:

1) deep diffusion to 20 ohm/square
2) etch back of junction
3) standard diffusion to 35 - 40 ohm/square

No significant improvement in solar cell performance was found by employing this sequence versus proceeding directly to the standard shallow diffusion.

Process Development Research

Hydrogen Passivation

We arranged to treat samples of Silicon-Film™ wafers with a Kaufman hydrogen ion source at NREL in November with the collaboration of B. Sopori. Table 7 compares mesa diode, short circuit current results of the two hydrogenation methods to untreated material. It is clear that substantial current gains can be obtain by employment of the Kaufman ion source.

Table 7. Comparison of Hydrogenation Methods on Mesa Samples

Sample	Jsc (ma/cm2)	Improvement (%)
As-Grown	16.51±0.42	-
PECVD H+ Process	17.36±0.67	5.1
Kaufman Ion Process	19.39±0.12	17.4

Based on these results we decided to acquire the capability for conducting process research using a Kaufman ion source. A source was specified which would irradiate an area greater than 15 cm x 15 cm. We visited Commonwealth Scientific and ordered a 16 cm ion source with divergent optics to be mounted on our present vacuum stack. The source was delivered in December and was brought on-line in January.

An initial survey of the process space for Kauffman source process development and equipment upgrade was conducted. Process development is concentrating on high beam energy and short process times. Results to date are summarized in Table 8.

All increases in parameters are based on averages of four to six solar cells. The experiments employed 100 cm^2 Product I solar cells. These are preliminary data. The solar cells used came from a wide range of processing conditions before hydrogenation.

Table 8. Hydrogenation by Kauffman Source

Sample Set	Beam Parameters		Time,	Voc gain,	Isc gain,	FF gain,	Power gain,
	Voltage	Current	min	%	%	%	%
1	1200eV	300mA	2.5	-0.3	5.7	5.7	11.3
2	1200eV	300mA	5.0	5.4	12.3	19.4	37.5
3	1000eV	300mA	2.0	-0.8	2.5	2.1	8.7
4	1000eV	300mA	5.0	6.1	8.5	11.6	24.5
5	800eV	200mA	5.0	0.7	2.9	3.0	6.7
6	800eV	250mA	5.0	1.8	5.5	11.3	19.5

This initial survey shows that longer times, higher acceleration voltages and higher beam currents produce the greatest increases, as expected. These data are being used to formulate the best experimental plan consistent with the constraints of the hardware.

Equipment upgrades were made in order to increase throughput. A load lock was purchased and installed on the system. The load lock design reduces the pumping time per sample from 45 min. to 10 sec. We have been troubled by a rapid buildup of a dielectric film inside the chamber and on the Kaufman source anode; this film prevents the ion source from operating and requires system tear down and cleaning. We suspect that this film is polymerized pump oil from the mechanical backing pumps. Molecular sieve traps have been ordered and will be installed for both mechanical pumps. We expect that this will increase the system up time.

Process work concentrated on the highest energy process achievable to date: 1200 eV, 300 mA. Table 9 indicates data for a well matched group of "A" grade wafers was selected and groups of 10 wafers were hydrogenated for times from 5 to 7 minutes.

Table 9. Percentage Change in Mesa Device Parameters as a Function of Hydrogenation Time

Process time, (min)	5.0	6.0	7.0
Voc	6.9 % ± 0.6 %	6.3 % ± 0.6 %	6.5 % ± 0.6 %
Isc,	11.2 % ± 1.4 %	14.5 % ± 1.4 %	13.4 % ± 1.4 %
ff	- 1.0 % ± 2.0%	4.8 % ± 1.9 %	3.2 % ± 1.9 %
Pmax	18.8 % ± 2.7 %	27.1 % ± 2.6 %	24.9 % ± 2.6 %

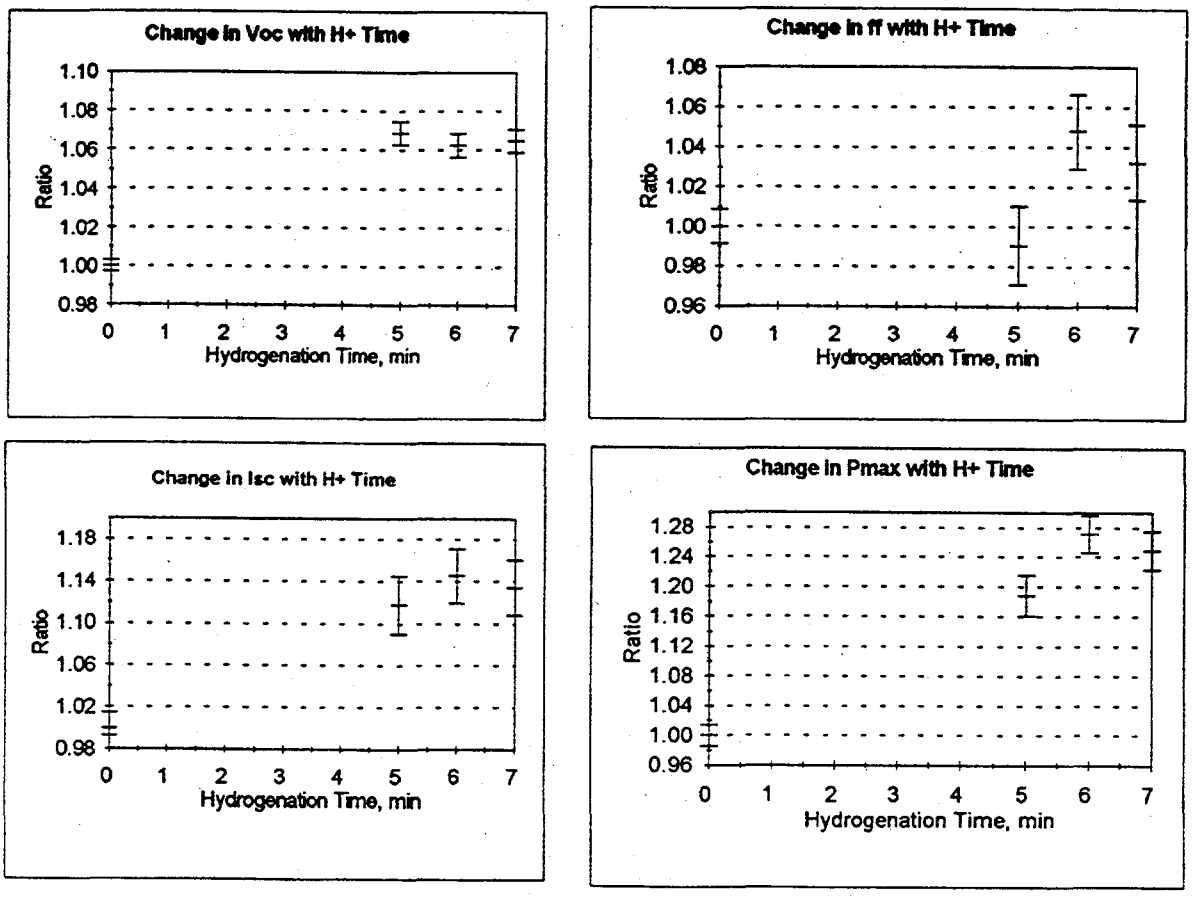
These data are shown with error bars in Figures 16A through 16D. Data from our mesa process, (samples hydrogenated at 1200 eV, 300 mA, 6 min.) indicate that the Isc gains may be limited by surface damage effects. Mesa QE data show increases in diffusion length balanced by a severe drop in blue response. Figure 17 compares the QE of a mesa device before and after hydrogenation.

We can make several conclusions at this point:

a) As previously reported, the RF hydrogenation process primarily improved Voc. The Kaufman hydrogen ion source primarily improves Isc.

b) The Kaufman ion source process appears to be saturated by the time 5-6 minutes of processing time has been carried out. The QE data suggests that there is a balance between continued improvement of bulk performance versus introduction of surface damage.

To recover the blue response, we are looking into the effect of an anneal process. We also will investigate the effect of a combined Kaufman, RF hydrogenation process to capture the benefits of improved voltage and current.



Figures 16. Ratios of changes in solar cell parameters as a function of hydrogenation time

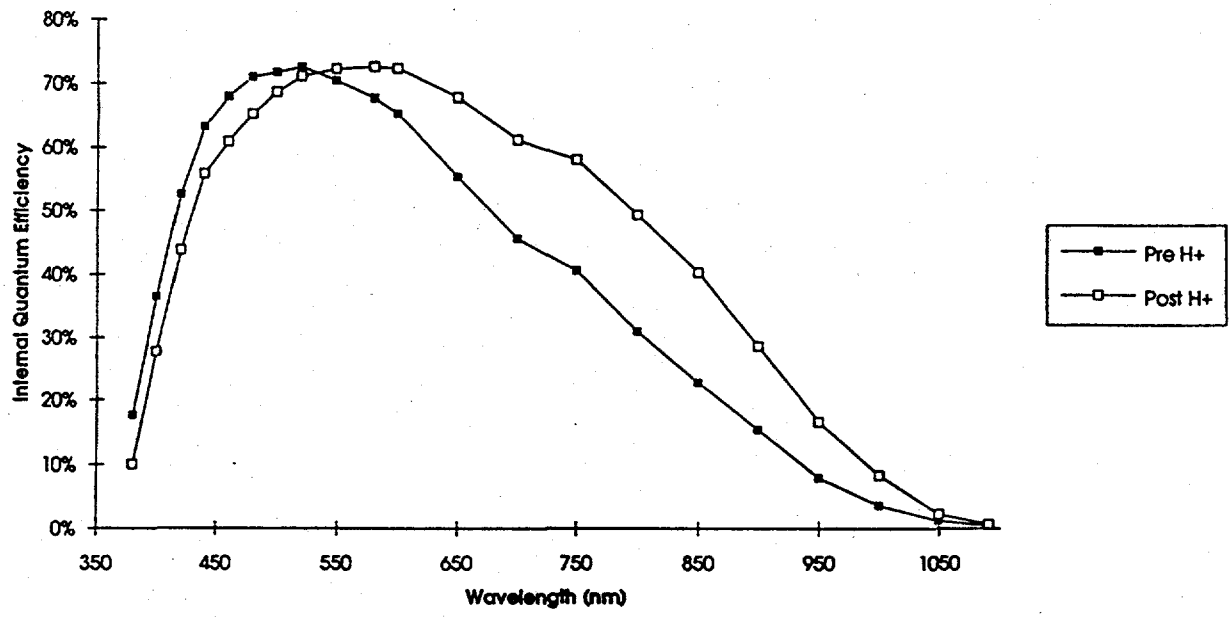


Figure 17 Spectral response of a Si-Film mesa device, before and after hydrogenation

Advanced Processes

During this reporting period work focused on the development of a process for enhancing solar cell performance of the Si-Film Product I material by solar cell processing. The process steps employed were hydrogenation, using RF plasma and a Kauffman source, a junction thinning procedure, a surface passivation process and a PECVD silicon nitride anti-reflective coating.

Tables 10 and 11 shows the improvements measured on a lot of five solar cells subjected to a processing procedure designed to enhance solar cell performance. The lot of solar cells all received an RF and Kaufman source hydrogen treatment prior to a junction thinning step. A striking result of the hydrogenation treatment was an increase in the average device current of 15.7% from 1.35 ± 0.08 to 1.56 ± 0.02 amps. Equally interesting is that the standard deviation of the averages became tighter after the hydrogenation treatments. This result indicates that these treatments upgrade materials with differing initial device behavior to a fairly homogeneous level. This result may indicate the presence of a separate performance limiting defect not treatable by hydrogenation.

Table 10. Solar Cell Performance at Each Process Step

Process Sequence Step	Voc	Isc	FF	Pmax
Initial	0.483 ± 0.013	1.35 ± 0.08	0.613 ± 0.013	0.40 ± 0.06
RF Plasma H+	0.506 ± 0.008	1.47 ± 0.02	0.645 ± 0.008	0.48 ± 0.03
Kaufman H+	0.517 ± 0.007	1.56 ± 0.02	0.657 ± 0.007	0.53 ± 0.04
Junction Thinning	0.515 ± 0.005	1.63 ± 0.03	0.667 ± 0.005	0.56 ± 0.04
Passivation	0.520 ± 0.009	1.65 ± 0.04	0.676 ± 0.009	0.58 ± 0.04
Si_3N_4 AR Coating	0.526 ± 0.007	2.07 ± 0.02	0.689 ± 0.007	0.75 ± 0.03

Table 11. Cumulative Fraction Increase in Solar Cell Parameters

Process Sequence Step	Voc	Isc	FF	Pmax
Initial	1.000	1.00	1.00	1.00
RF Plasma H+	1.05 ± 0.02	1.07 ± 0.01	1.01 ± 0.07	1.14 ± 0.09
Kaufman H+	1.07 ± 0.01	1.14 ± 0.01	1.03 ± 0.08	1.25 ± 0.10
Junction Thinning	1.07 ± 0.01	1.19 ± 0.03	1.05 ± 0.07	1.33 ± 0.10
Passivation	1.08 ± 0.02	1.20 ± 0.02	1.06 ± 0.06	1.38 ± 0.11
Si_3N_4 AR Coating	1.09 ± 0.02	1.51 ± 0.02	1.07 ± 0.03	1.77 ± 0.09

The combination of junction thinning and surface passivation was found to yield an average increase of 9.8% in the power of the lot. The junction thinning step targeted a sheet resistance of 80 to 100 ohms per square. A 10 nm thick, CVD-deposited, SiO_2 passivation layer was employed before the Si_3N_4 AR coating deposition.

The processing sequence outlined below was used to examine the effect of each performance enhancing process averaged over nine Silicon-Film mesa solar cells as shown in Figure 18.

1. surface prep (remove about 12 microns)
2. diffuse (R_{sheet}=30Ω/sq)
3. strip P_2O_5
4. metallize
5. junction thinning (R_{sheet}=60Ω/sq)
6. RF hydrogenation
7. deposition of PECVD SiO_2 passivation layer
8. 400°C, 30 minute forming gas (15% H_2, 85% N_2) anneal

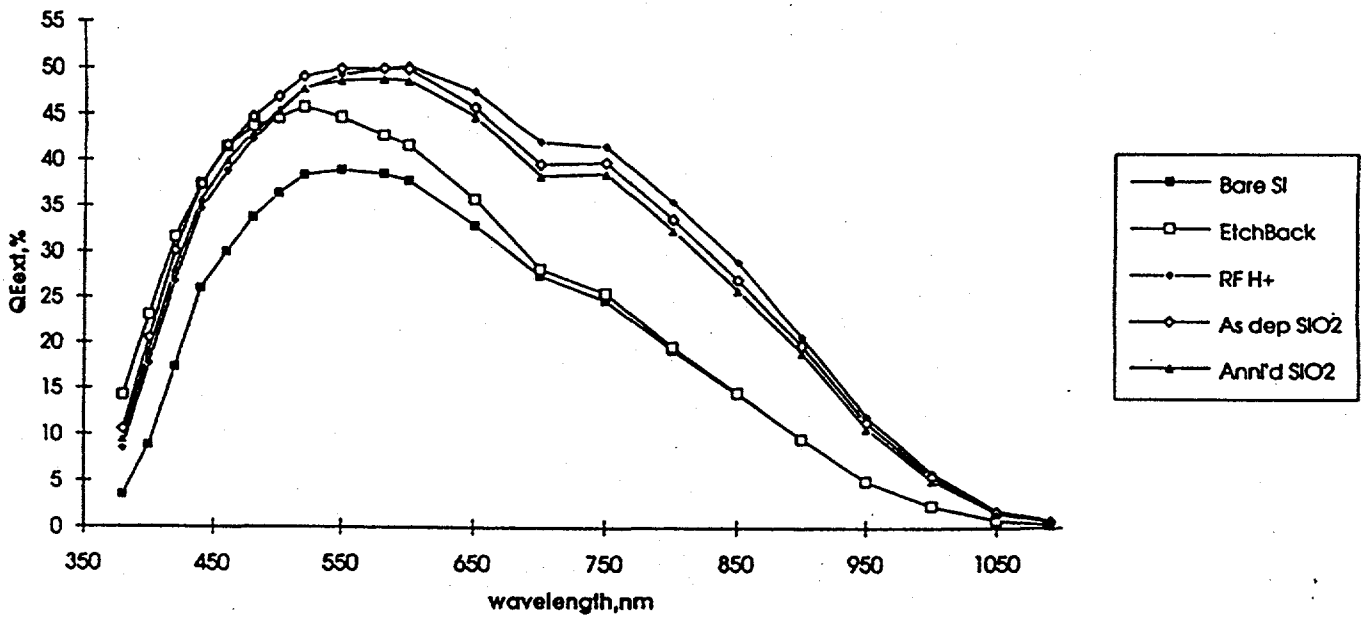


Figure 18. Performance enhancement as measured by quantum efficiency as a function of process step

These data show the performance enhancement resulting from one particular sequence of processes. We are conducting additional studies testing the effect of process sequence (e.g. hydrogenation before metallization) as well as the intensity of each process (e.g. level of junction thinning, ion beam current level in RF hydrogenation). Our objective is to understand the effect of each performance enhancing process alone and in sequence with other processes so that an optimized Silicon-Film solar cell can be reproducibly produced.

Solar Cell Characterization

Solar cell characterization results were reported to us by R. Mitchell from NREL and P. Basore from SNL. The most important conclusion is that the LBIC method for measuring solar cell response has shown that the uniformity of response for Silicon-Film solar cells is quite good. The multi-wavelength LBIC technique has shown that diffusion lengths are in the range of 20 to 70 micron, averaging about 35 micron. The expected or modeled performance of the solar cells based on this measure corresponds well with observed values.

We analyzed and compared the results for measurements of 100 cm^2 solar cells submitted as deliverables during the first phase of the project. Table 12 summarizes the data obtained from AstroPower, NREL and Sandia for the three solar cells. The dates for the reported data are shown in the table notes.

Table 12. Product I Solar Cell Measurements and Intercomparison

Device	Measurement Lab				Ratios	
	API	NREL	SNL		r(NREL/API)	r(SNL/API)
D-2 ID# EL-8/12						
Voc	0.558	0.559	0.555	volts	1.002	0.995
Isc	2.428	2.324	2.205	amps	0.957	0.908
Vmp	0.459	0.437		volts	0.953	
Imp	2.112	2.047		amps	0.969	
Pmax	0.970	0.895	0.883	watts	0.923	0.910
ff	0.715	0.689	0.721		0.964	1.008
Area	106.1	106.1	105.8	cm^2		
D-2 ID# 1192-A5						
Voc	0.561	0.538	0.557	volts	0.959	0.993
Isc	2.586	2.420	2.320	amps	0.936	0.897
Vmp	0.474	0.434		volts	0.915	
Imp	2.236	2.146		amps	0.960	
Pmax	1.103	0.931	0.778	watts	0.844	0.705
ff	0.761	0.714	0.603		0.939	0.793
Area	106.1	106.3	105.8	cm^2		
D-2 ID# 1192-A6						
Voc	0.560	0.543	0.556	volts	0.971	0.994
Isc	2.749	2.600	2.490	amps	0.946	0.906
Vmp	0.445	0.400		volts	0.900	
Imp	2.413	2.264		amps	0.938	
Pmax	1.073	0.905	0.891	watts	0.843	0.830
ff	0.698	0.642	0.645		0.920	0.925
Area	106.1	106.2	105.8	cm^2		

Measurement History	API	NREL	SNL
D-2 ID# EL-8/12	09/01/92	12/04/92	10/26/92
D-2 ID# 1192-A5	11/14/92	11/17/92	12/09/92
D-2 ID# 1192-A6	11/14/92	11/17/92	12/09/92

We have come to the following conclusions at this time:

1) There is good agreement with the Voc and fill factor measurements for sample EL-8/12 for all three labs.
2) We expect that remeasurements of 1192-A5 and 1192-A6 at NREL will bring about agreement with voltage.
3) There appears to be a consistent 5% difference in Isc between AstroPower and NREL.
4) The disagreement between Sandia and the others in Isc appears to be partially (~1.6%) due to light source non-uniformity.

Fabrication of 15 cm x 15 cm Solar Cells

As described in the summary we decided to shift our manufacturing focus completely to large area solar cells and modules. To carry out this aim, we started with the modification, installation and commissioning of an equipment set to manufacture 15 cm x 15 cm solar cells.

We designed and fabricated tooling and materials for production of 225 cm^2 solar cells. This included preparation of the large diffusion furnace and quartz ware, design and ordering of screen print patterns and acquisition of chemical processing cassettes. An initial solar cell fabrication sequence for processing 15 x 15 cm^2 wafers was established for lots of eight.

The two 2/15/93 15 x 15 solar cell deliverables were tested at NREL as a reference point for comparing results between NREL and AstroPower, and for evaluating progress in the development of larger Silicon-Film solar cells. These data are shown in Table 13 and indicate the difficulty in accurately testing these large solar cells. Whereas the individual numbers for the AstroPower results compared to those of NREL are somewhat different, there is a significant difference in the measured short circuit current for sample AP-225-9. There is a need to resolve the source of this particular difference to minimize future discrepancies in measured values of these large solar cells.

Table 13. Summary of AP-225 Silicon-Film Solar Cell Data

AP-225-#8	Voc, volts	Isc, amps	Vmp, volts	Imp, amps	Pmax, watts	FF
AP-CT	0.516	4.74	0.399	4.00	1.59	64.9
NREL	0.534	3.88	0.385	3.13	1.21	58.1

AP-225-#9	Voc, volts	Isc, amps	Vmp, volts	Imp, amps	Pmax, watts	FF
AP-CT	0.518	4.59	0.403	3.79	1.52	64.1
NREL	0.530	4.29	0.387	3.40	1.32	58.0

During May, two 15 cm x 15 cm Silicon-Film solar cells were delivered to NREL. Device performance before and after tabbing is shown in Table 14.

Table 14. Device Performance for 15 cm x 15 cm Solar Cells Before and After Tabbing (Cells delivered in May)

Cell	Voc (mV)		Isc (mA/cm^2)		FF		Power (Watts)	
	before	after	before	after	before	after	before	after
SF2469T1-35	566	568	5.622	5.472	0.73	0.71	2.337	2.193
SF2466B-25	552	550	5.405	5.404	0.73	0.71	2.166	2.119

As shown in Table 14, the short-circuit current of cell SF2469T1-35 dropped significantly after tabbing. This was due to ripping of the bus bar from the top surface of the cell and a resulting collection loss from

here the bus had been ripped. Cell SF2466B-25 exhibited more typical performance levels before and after tabbing.

Advanced Module and Panel Design

A module design was completed employing larger solar cells. The module characteristics are shown in Table 15 for the initial product introduction.

Table 15. 225 cm^2 Solar Cell Module Design

Module Characteristic	Value
Length, cm	96.0
Width, cm	96.0
Area, m^2	0.922
String Configuration	36 series
String Lay-Out	6 x 6
Voc, volts	20.2
Isc, amp	6.2
Pmax. watts	81.0

Modules from 15 cm x 15 cm Silicon-Film Cells

Representative Silicon-Film solar cells, 15 cm x 15 cm, were tested for mechanical stability during standard module fabrication. A two cell by six cell module of 15 cm x 15 cm cells successfully survived lamination with no visual evidence of mechanical failure. The laminator used was one used for our standard 36 Watt module of 10 cm x 10 cm cells (4 cells by 9 cells) which imparts 15 lbs/in^2 across the module area. Further mechanical stability testing was performed on the new laminator capable of laminating module areas up to 0.968 meters by 0.972 meters.

Conclusions

We have demonstrated an improved Silicon-Film wafer machine capable of 1.6 MW/yr volume production; continuous operation has been demonstrated. Solar cell power over 2.3 watts marks an important event for the 15 x 15 cm solar cell. We have demonstrated the capability to fabricate large area solar cells and to incorporate them into modules. Performance improvement of the solar cell process sequence will be obtained by optimizing the uniformity of the diffusion, front contact formation and AR coating processes. The large solar cell results obtained substantiate the assumptions for the cost reduction advantages for large solar cell production.

Key Conclusions

We have accomplished these objectives during this phase::

- 2.3 watt, 225 cm^2 solar cell
- 1.6 MW/yr wafer production rate from single machine
- continuous operation of wafer process

Effect on Product Introduction

The program has accelerated the advance of our technology:

- led directly to the early introduction of 225 cm^2 Silicon-Film™ solar cell product.
- development of a continuous, 1.6 MW/yr wafer machine
- shift in strategy for layer growth
- shift in approach for application of energy for sheet growth process
- development of higher thermal conductivity setter to achieve greater sheet speed
- development of gaseous environment to improve sheet morphology
- improved thermal control of sheet process
- computer control of sheet process
- increase of minority carrier diffusion length from 6 - 10 to 15 -20 micron range
- installation of on-line capability to produce 0.94 m^2 modules

Plans for Remainder of Phase II

- Determine material utilization of high throughput wafer machine
- Explore wafer process boundary conditions
- Improve solar cell performance
- Integrate solar cell and module line processes

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16. Abstract (Limit: 200 words)

AstroPower is in the second phase of a 3-year, phased effort to upgrade its facility to produce 1.22-m^2 Silicon-Film™ PV modules with an output of 170 W_p. Productivity improvements of the Silicon-Film™ machine were accomplished during the second phase. Improvements were made in solar cell performance while decreasing materials consumption, integrating and mechanizing the fabrication process for solar cells, and scaling-up solar cell and module equipment for fabricating larger cells. AstroPower is continuing work on separating out effects due to impurities and effects due to defects. Analytical tools were developed for measuring area-based response based on EBIC and LBIC methods. The Kauffman source for hydrogen ion implantation was used to map out the process space for Silicon-Film™ solar cell improvement. Progress was made on improving short-circuit current. Areas of focus include developing tools to quickly assess material quality; developing a hydrogen implantation process; increasing material quality on large-area, high-throughput wafers; and studying potential processes for improving solar cell power output during cell fabrication. A method to improve current collection in a solar cell after contact formation is under development.

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