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Silicon-Film™ Photovoltaic Manufacturing Technology

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S. R. Collins, R. B. Hall
AstroPower, Inc.
Newark, Delaware

NREL technical monitor: H. Thomas

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Introduction

Project Overview

The goal of AstroPower's PVMaT-2A project is to develop an advanced, low-cost manufacturing process for a new utility-scale, flat-plate module. This process starts with the production of continuous sheets of thin-film, polycrystalline silicon using the Silicon-Film™ process. Sheets are cut into wafers that are nominally 15 cm x 15 cm. 56 of these wafers are then fabricated into solar cells which are strung together in a 170 watt module. Twelve of these modules form a 2 kW array. The module, array, and solar cells have features described in Table 1.

Table 1. Silicon-Film™ Large Area PVMaT Products

Solar Cell Size	225	cm^2
Solar Cell Power	3.15	watts
Module Size	1.4	m^2
Module Power	170	watts
Array Power	2041	watts

The program has three main components:

1. Development of a Silicon-Film™ wafer machine that is capable of manufacturing wafers that are 225 cm^2 in size with a total product cost reduction of 70%.
2. Development of an advanced solar cell manufacturing process that is capable of turning the Silicon-Film™ wafer into a 14% efficient solar cell.
3. Development of an advanced module design based on these large area, efficient silicon solar cells with an average power of 170 watts for 56 solar cells and 113 watts for 36 solar cells.

Silicon-Film™ Technology

The Silicon-Film™ Process is a method for fabricating silicon wafers by the production of continuous sheets of thin film silicon on a low-cost substrate which are then cut to size. Because these sheets are produced at the desired thickness, ingot sawing and wafer polishing steps are eliminated resulting in a significant reduction in cost. For the Silicon-Film™ Process, silicon cost is determined by the material quality, silicon thickness, wafer breakage, and kerf loss during sheet sawing. In developing a low-cost process, the focus is on limiting the consumption of higher cost high quality silicon, eliminating ingot sawing steps, and utilizing a high yield continuous manufacturing technology. The continuous manufacturing process produces the volume to reduce the per wafer cost of capital equipment and labor while improving process control.

The photovoltaic effect in Silicon-Film™ grown on a low-cost, coated steel substrate was first observed at AstroPower in August 1984 [1]. By October of 1985, the energy conversion efficiencies of these micro-sized devices (less than one square millimeter) increased to 9.6 %,

without an antireflection coating [2]. Larger area devices were plagued by shunts which were eventually attributed to stress caused by thermal expansion differences between the steel and the silicon. The impact of this stress was reduced by adding a fairly thick ceramic coating to the steel which led to a 12 square millimeter, 9.6% solar cell as measured by SERI in November 1986 [3]. This thick ceramic coating led to the abandonment of steel in favor of a thermal expansion matched ceramic in January of 1987. One square centimeter, 9.7% efficient solar cells were measured by Sandia in June 1987 [4]. Continued development of this approach led to the achievement of a 14.9% Silicon-Film™ solar cell measured by Sandia in December of 1988 [5]. All of the above results were achieved with active silicon layers approximately 100 um thick. Light trapping was not employed for these initial solar cells. A series of commercial-size, 100 cm^2 solar cells was measured by Sandia in September 1989 with a median efficiency of 10% [6].

A Pilot Scale machine was operated in a batch mode, while the data were collected and the design rules were developed for the first manufacturing machine. Until May of 1993, semi-continuous mode machines were used leading to demonstrated efficiencies in excess of 10%. Modifications were then made to convert a semi-continuous mode machine to a truly continuous manufacturing mode machine which is the current Phase A production machine.

Figure 1 shows the progress that has been made with the development of Silicon-Film™ technology during the last six years. The key progress step was the demonstration of the 10.3% efficient 15 cm x 15 cm product.

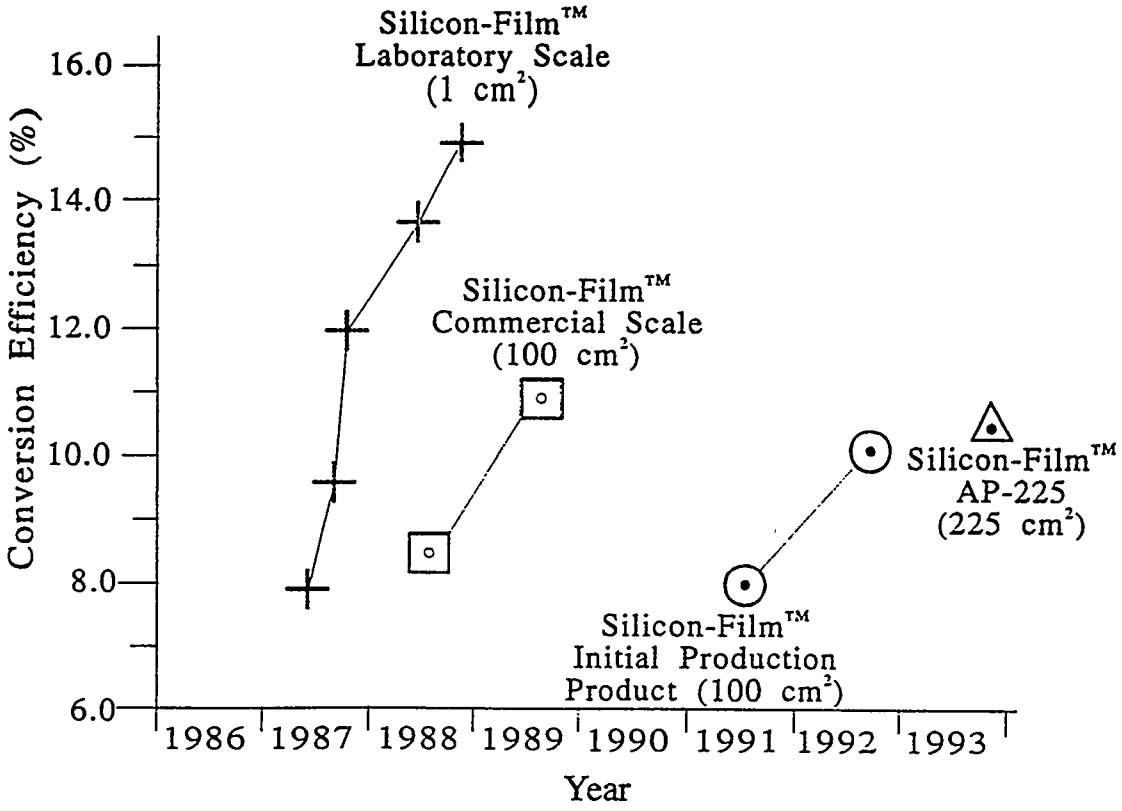


Figure 1. Progress in total area efficiency for Silicon-Film™ solar cells

PVMaT Goals

Development of a Silicon-Film™ manufacturing technology requires the successful achievement of the following three objectives leading to the milestones listed in Table 2:

- design, construction, and demonstration of a production machine that generates sheets of Silicon-Film™ at a wafer production rate capable of 3.0 MW/yr.
- development of a low-cost fabrication process that fabricates 3.15 watt solar cells that are 15 cm by 15 cm.
- development of a large area module production line that produces both 113 Wp, 0.9 m^2 modules and 170 Wp, 1.4 m^2 modules.

Table 2. Specific PVMaT Goals for Phase I through Phase III

	Phase I	Phase II	Phase III
Wafer Machine Production Rate Material Use Efficiency	 400 kW/yr 75%	 1.3 MW/yr 85%	 3.0 MW/yr 90%
Solar Cell Size*	a) 10 cm x 10 cm b) 15 cm x 15 cm	b) 15 cm x 15 cm c) 15 cm x 45 cm	b) 15 cm x 15 cm c) 15 cm x 45 cm
Solar Cell Power	a) 1.1 watts	b) 2.25 watts 2.5 watts	b) 2.8 watts 3.15 watts
Module Power	--------	b) 72 watts 84 watts	b) 98 watts 170 watts

* a) AP-100, b) AP-225, c) AP-675

The two solar cell and module powers shown in Table 2 for Phase II and Phase III indicate improvements in performance targeted for those phases. For example, a 2.8 watt cell is the target for the first six months of Phase III, whereas a 3.15 watt cell is the target for the last six months of Phase III.

Key Results

During Phase II, AstroPower made significant advances in improving Silicon-Film™ material quality and device performance. Advances were made in developing the prototype machines and processes toward reliable manufacturing counterparts. Our key achievements in Phase II are detailed in the sections that follow. They are:

- demonstration of a truly continuous production mode Silicon-Film™ machine.
- demonstration of a 2.5 watt, 15 cm by 15 cm Silicon-Film™ solar cell.

- demonstration of a 78 watt module fabricated from 36, 15 cm by 15 cm Silicon-Film™ solar cells.

Wafer Machine Performance Benchmarks

A three phase (A through C) development plan with full specifications for the Silicon-Film™ manufacturing machine has been completed. The Phase A machine exceeded its targeted material generation rate by 31% during the seventh month of Phase II. The Phase B machine design parameters and conceptual drawings are nearly complete; construction of the Phase B machine is scheduled for completion in 1994. This new machine is designed to operate at a machine generation rate that exceeds Phase III goals.

Solar Cell Efficiency Achievements

Figure 2 shows the current-voltage characteristic for a 2.5 watt, 240.2 cm^2 Silicon-Film™ solar cell as tested at NREL. This solar cell demonstrates significant progress in Silicon-Film™ process development. It is the biggest and best solar cell AstroPower has ever made.

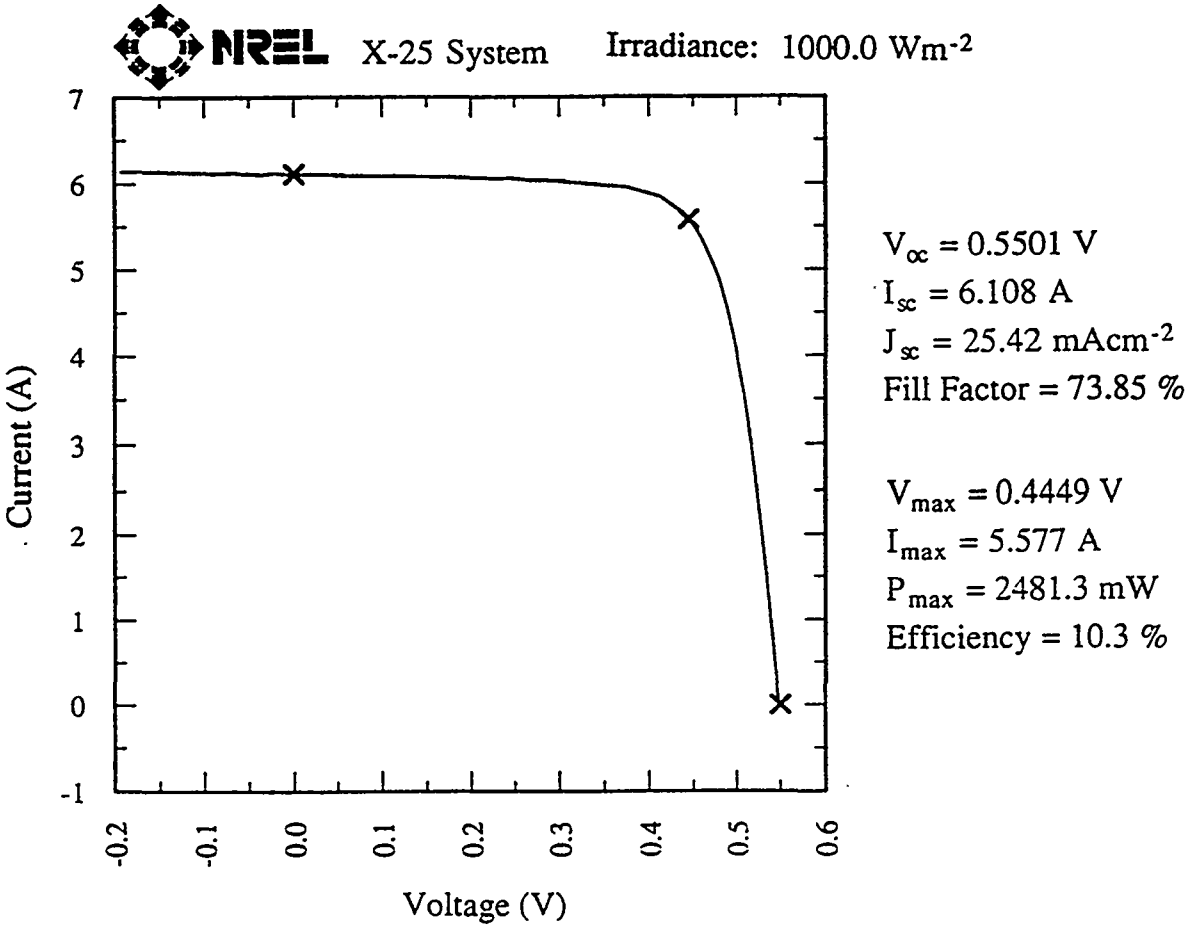


Figure 2. NREL I-V characteristic of a Phase II 240.2 cm^2 solar cell delivering 2.5 watts

Module Assembly Achievements

An important benchmark for Silicon-Film™ technology was the fabrication and delivery of two large area modules (0.95 m^2) during Phase II. Both modules were fabricated from 36, 15 cm x 15 cm solar cells. Table 3 provides the performance parameters for the two modules as tested outdoors by NREL. These modules represent the largest and highest power modules AstroPower has ever made.

Table 3. NREL Outdoor Test Data for 36 Cell Silicon-Film™ Modules

ID#	Area (cm^2)	Temp (°C)	Voc (V)	Isc (A)	FF (%)	Vmax (V)	Imax (A)	Pmax (W)	Aper. η (%)
D-12	9082	21.9	18.7	5.5	69.9	14.5	4.9	71.3	7.6
D-18	9082	17.3	19.7	5.6	70.6	15.8	4.9	78.0	8.4

The estimated U95 uncertainty of the NREL outdoor measurements is ±5%. Temperature was measured at the back of the module during testing; no correction for temperature was made. The square aperture area was 95.3 cm x 95.3 cm. Total irradiance was 1036 W/m^2. Spectral mismatch error was measured at 2% and second order irradiance error was less than 4%; the provided data was not corrected for these errors.

Silicon-Film™ Process

Process Capability

The capability of the Silicon-Film™ Process is described in this section. The wafer formation process is briefly presented followed by calculations describing the areal generation rate and material use efficiency planned and achieved during Phase II. Finally, a discussion of the details of yield and machine operation are presented.

Wafer Formation Process

A setter transports the raw materials through the active layer growth process. The setters are transported in a manner that permits the continuous application of the raw materials and the continuous growth of the active layer; there is only one beginning and one end of the sheet as established by the beginning and the end of the production run. The sheet is cut to the desired length as it exits the machine.

The growth of the active layer is accomplished in a system purged with an inert gas to reduce the effects of oxidation. The linear sheet speed, gaseous ambient, and the axial and transverse thermal profiles of the machine are fundamental parameters that are critical to achieving the desired sheet properties.

There are two key performance benchmarks for this task: wafer machine rate and material use efficiency. The Phase II goal for these benchmarks was to demonstrate a wafer machine operating rate capable of producing 1.3 MW per year and to demonstrate a material use efficiency of 85%. In the following paragraphs, we describe how these benchmarks are measured and how the targeted goals were met.

Wafer Machine Rate Calculation

The machine rate goal for Phase II was to demonstrate a areal generation rate capable of producing 1.3 MW/year. We have exceeded the targeted production rate by 31%. Figure 3 illustrates the geometry for a Silicon-Film™ sheet on the setter. Production rate is the product of the following set of factors: the areal machine growth rate, Mr, in m^2/hr, the number of operating hours per year, N_O, and the solar cell efficiency, Eff.

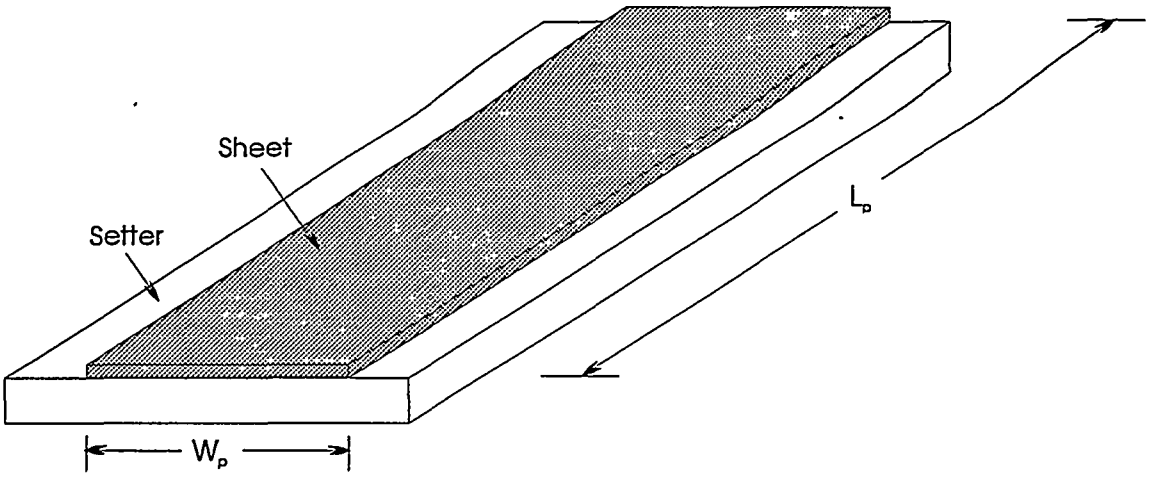


Figure 3. Silicon-Film™ sheet geometry

The equation for the definition of the production rate is:

$$PR = Mr * N_o * Eff * 10^{-5},$$

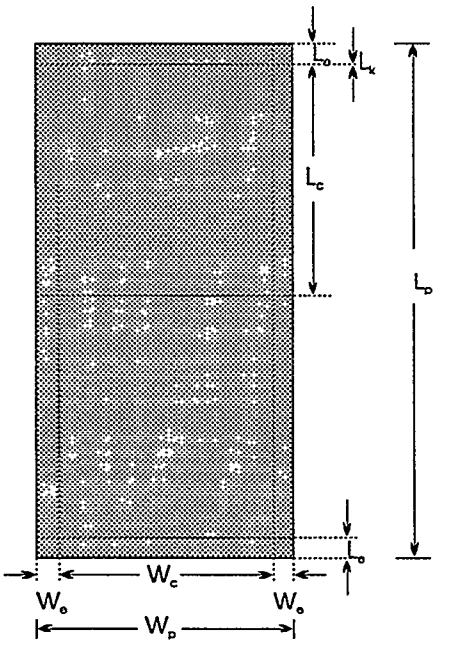
where

PR	=	production rate, MW/year
Mr	=	machine rate m^2/hr
N_o	=	number of production hours per year
Eff	=	resultant solar cell efficiency, %.

The solar cell efficiency was based on the highest efficiency measured by NREL on a solar cell fabricated from representative material. The number of hours per year is assumed to be 8000 hrs/yr, based on continuous operation of the machine. Under these assumptions and measured values we obtain an optimal Phase II machine rate of 1.8 MW/yr. The areal generation rate is based on finished wafer area generated per hour as shown in Figure 4.

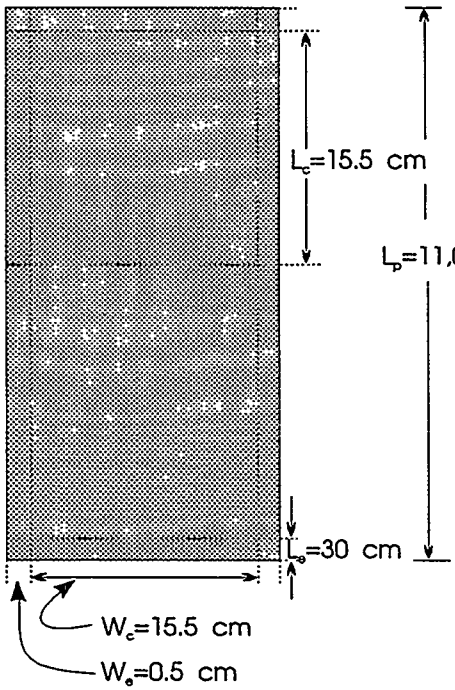
Material Use Efficiency Calculation

The material use efficiency measures the amount of silicon which ends up in the finished wafer compared to the amount of silicon introduced at the beginning of the wafer formation process. Figure 5 shows the relevant geometric considerations for the calculation of the material use efficiency.



L_p = length of sheet
W_p = width of sheet
N = number of wafers possible from sheet
L_e = edge length
W_e = edge width
L_k = saw kerf
L_c = length of cell
W_c = width of cell

Figure 4. Definition of dimensions for calculating finished wafer area



L_c = 15.5 cm
W_c = 15.5 cm
N = 703
L_p = 11,040 cm
W_p = 16.5 cm
L_e = 30.0 cm
W_e = 0.5 cm
L_k = 0.2 cm
Y_g = $\frac{703*15.5*15.5}{11,040*16.5} = \frac{170,097}{182,160} = 0.93$

Figure 5. Measurement of plank geometric yield for a typical 8 hour production run

This efficiency depends on the details of the wafer formation process and can be resolved into the product of three factors: the applicator yield, Y_a, the edge trimming and kerf yield, Y_g, and the wafer visual and mechanical yield, Y_{VM}:

The equation which defines the material use efficiency is

$$MUE = Y_a * Y_g * Y_{VM},$$

where

MUE	=	material use efficiency
Y_a,	=	application yield
Y_g,	=	geometric yield
Y_{VM},	=	visual and mechanical yield.

The applicator yield measures the amount of silicon material applied against the amount that is moved into the growth zone. The applicator yield throughout Phase II averaged 99%. The geometric yield is based on the number of wafers that could be obtained from the as-grown planks compared to the amount of material applied. Throughout Phase II, a 16.5 cm wide plank was produced which was cut into 15 cm x 15 cm cells. Based on a typical 8 hour production run and 30 cm of lost material at the beginning and end of the sheet, the ideal yield calculated from geometric considerations is 93%. The visual and mechanical yield accounts for the losses of wafers due to a variety of defects as well as to mechanical breakage. The visual and mechanical yield during our best production run was 93% leading to a cumulative material use efficiency of 86%.

Wafer Process Improvement (Task 8)

Central to the achievement of the Silicon-Film™ solar cell is the development of the wafer machine and the related wafer production process. The development of a wafer process capable of manufacturing depends on establishing control of the key process variables. During Phase II, the wafer production process went through significant transformations leading to a new machine design and improvements in parameter control. The following sections describe those transformations and their significance.

Environmental Control

The only recognized environmental variable is the gas that is present during sheet formation. The sources of the gas components are those that are intentionally introduced, and those that are generated during processing. We have experimented with two different intentionally introduced gases. Mixtures of these two gases have also been investigated. Under the present operating conditions, only one of these pure gases promotes consistently smooth surface morphology.

Thermal Control

Thermal control of the process is necessary to achieve the temperature ramp-up of materials prior to growth, to control the active layer growth, and minimize defects that can occur during the temperature ramp-down of the grown layer. These three zones and their relative size is shown in Figure 6.

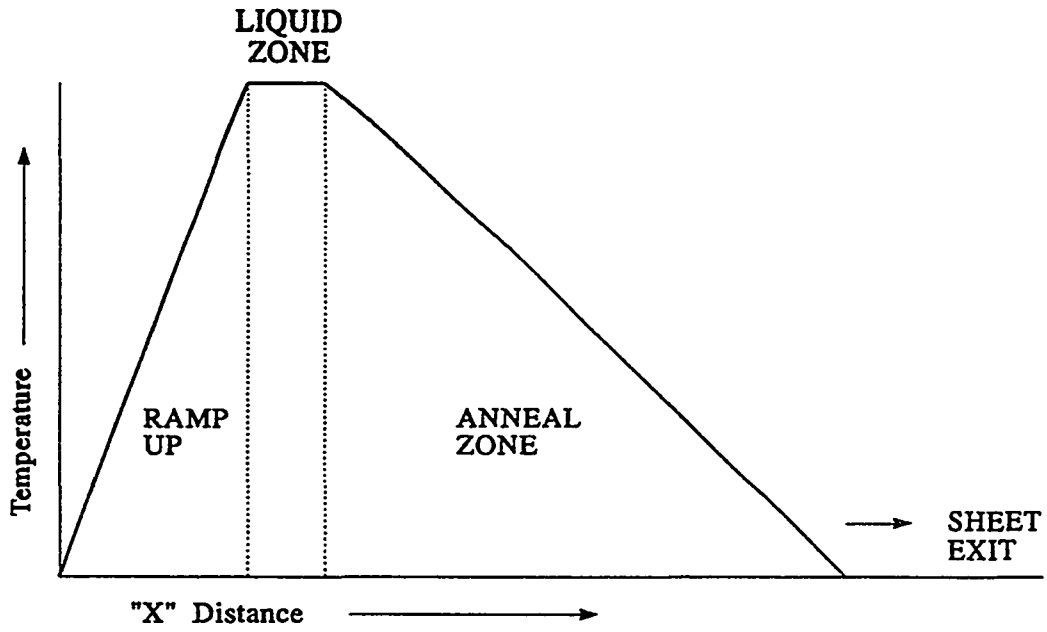


Figure 6. Shape and relative size of thermal zones along the length of the Silicon-Film™ machine

During Phase II, fundamental changes in thermal control were undertaken. These changes were the direct result of crystal growth modeling which prescribed the thermal environment required to support desired crystal growth mechanisms. The prescribed thermal environment was then transcribed into conceptual machine and component designs, computer-aided design drawings, and finally machine modifications. This design process led to the present Phase A machine and the Phase B machine design.

In the present Phase A machine, monitoring of system temperature is accomplished by thermocouples and optical pyrometry. Thermocouples have been the core monitoring device due to their low maintenance, high reliability, and durability. Contact and close proximity thermocouples are both employed depending on the feasibility of contacting the heated surface. Point viewport optical pyrometry is also used, however, stable emissivity of the heated surface is a prerequisite and viewport windows require regular cleaning and maintenance. A linescan optical pyrometer is under consideration to supplement thermocouple monitoring, since it offers thermal image profiles of the sheet surface instead of an instantaneous temperature at a given point.

Closed Loop Control System

All closed loop control and data logging features are controlled by a personal computer. Closed loop control is used to control the sheet speed and the temperatures of heat sources. Data logging of raw material temperature, sheet temperature as it travels along the length of the furnace, and active cooling media temperature and flow is continual at time increments down to 1 second. One minute intervals are presently being employed.

Wafer Process Boundary Conditions (Task 9)

The productivity of the Silicon-Film™ wafer process is determined by the square meters produced per hour (throughput) that meet the product performance specification. The critical element in determining the productivity of the present wafer manufacturing line is the active layer formation step, specifically the linear process speed and the width of the generated sheet and associated boundary conditions. The following sections describe the present productivity status of the Silicon-Film™ wafer machine including the issue of material use efficiency.

Linear Process Rate

The Phase II sheet fabrication machine was designed to run at a production rate capable of 1.3 MW/year. It was empirically determined that the optimal speed with the current design was capable of 1.8 MW/yr production rate. "Optimal" here relates to the machine reliability rather than dependence of material performance on sheet speed. To determine the correlation between linear process speed and device efficiency, small area (0.2 cm^2) mesa diodes were fabricated using identical processing on material grown at varying linear sheet speeds. No direct correlation was established.

To date, it has been found that linear sheet speed is machine design dependent. We have not yet approached an upper limit.

Process Length and Width

An important step in improving process yield was made by transforming the Silicon-Film™ sheet process into a truly continuous process. This was achieved by eliminating the chain drive transport system which led to speed inconsistencies in material transport, vibration of material during crystal growth, and transport failures leading to extensive repairs and lengthy periods of down-time. The new system is based on continuous feed operation. Process width remained 16.5 cm throughout Phase II.

To date, it has been found the width of the sheet is machine design dependent. We have not yet examined the possibility of an upper limit. We intend to continue to produce sheets between 15.5 and 16.5 cm wide throughout the PVMaT program due to our targeted 15 cm wide product.

Large Area Wafers

Throughout Phase II, standard solar cell areas of 15 cm x 15 cm were handled. Larger solar cell areas of 15 cm x 45 cm were also fabricated to show future capabilities of the process. Full tooling to support manufacture of the 45 cm long cells is considered a premature investment for the technology and was therefore not a focal point of the Phase II effort.

Material Usage Efficiency

Conversion to a continuous process led to a significant improvement in material usage efficiency. Prior to this development, the areal yield of product was strongly influenced by the growth commencement and termination zones of each sheet. These zones comprised a significant portion of the sheet length. Now that the sheet is continuous, commencement and termination zones occur only once a day and are not a significant percentage of the generated area of sheet. Improvement of Material Use Efficiency to 90% will be investigated during Phase III by reducing the sheet width to 16.1 cm and improving the sheet quality yield to 96% by implementing improved process controls.

Wafer Machine Building Block Design (Task 10)

A three phase (A through C) development plan for the Silicon-Film™ manufacturing machine was completed during Phase II. Specifications categories for each phase are listed in Table 4. Most of these categories were fully specified in a written planning document for each of the three phases. Phase II of the PVMaT program was conducted using a Phase A machine which exceeded its targeted material generation rate by 31% during the seventh month. The Phase B machine is designed to operate at a machine generation rate that exceeds Phase III PVMaT goals and will be brought on-line during 1994. Consultants from The Dow Chemical Company have provided guidance on tactical approach, project planning, technical assistance and operations management. Their vast experience in converting prototype designs and processes to successful manufacturing counterparts will ensure that our Phase III achievements occur on schedule.

Table 4. Specification Categories of Three Phase Machine Development Plan

1. Basic Functions	10. Process Controls
2. Safety	11. Operator Inputs
3. Environmental Concerns	12. Equipment Adaptability
4. Industrial Hygiene Concerns	13. Equipment Accessibility
5. Product Specifications	14. Non-product Quantities and Specs
6. Production Quantity	15. Utility Requirements
7. Production Yield	16. Quality Control
8. On-line Operating Time	17. Reliability
9. Raw Materials Specifications	18. Operating Lifetime

Material Quality Requirements

The most important electrical parameter determining the level of quality of the Silicon-Film™ active layer is minority carrier diffusion length. Both the magnitude of the minority carrier diffusion length and its spatial uniformity are important in establishing the utility of any photovoltaic material. This section describes the level of solar cell performance achieved and planned with present Silicon-Film™ material, indicates the known causes that limit performance in this material, and demonstrates the high degree of spatial uniformity achieved in the material and device parameters.

Expected Performance

The best measure of potential solar cell performance is minority carrier diffusion length. Figure 7 summarizes the predicted power from the 15 cm x 15 cm Silicon-Film™ solar cell as a function of diffusion length and solar cell design. The present solar cell design refers to the processing used for the deliverables at the end of the Phase II program leading to the 2.5 watt 15 cm x 15 cm solar cells. The advanced design incorporates a grid shading of 3.2%, improved blue response including surface passivation and improved emitter design corresponding to a 12% increase in current, an increase in voltage to 600 mV, and a fill factor increase to 0.74 leading to a 3.15 watt 15 cm x 15 cm solar cell.

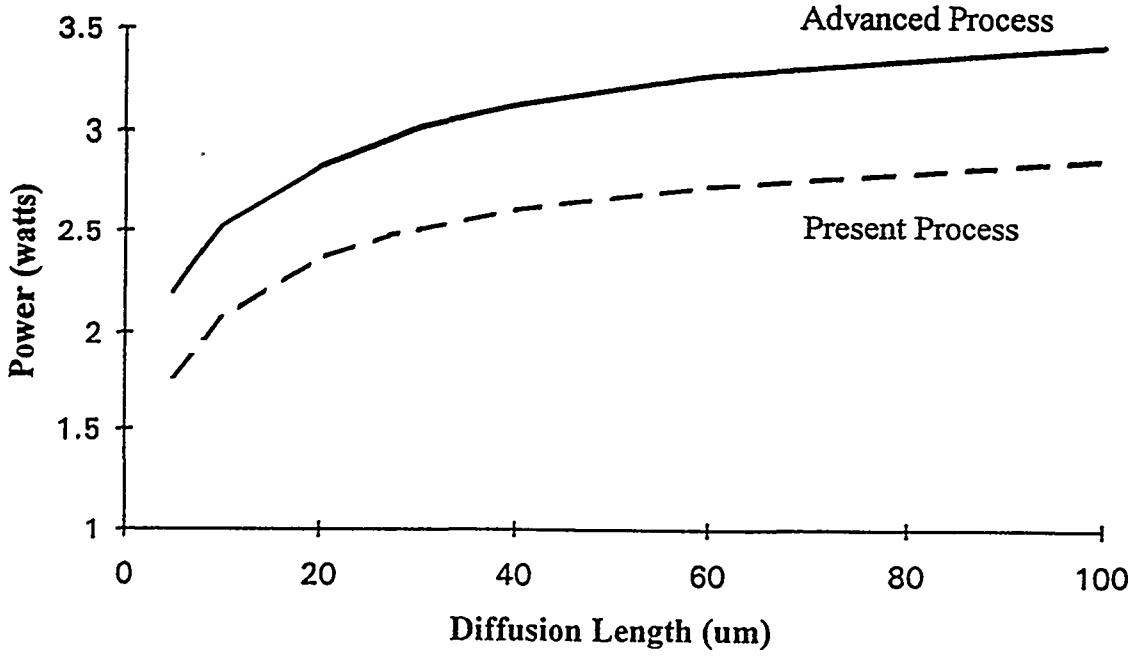


Figure 7. Predicted power as a function of Ln

Characterization

The main characterization tool used during the Phase II program was the small area mesa test device. These devices are processed using the same baseline fabrication sequence used in making large area cells. The processing sequence is provided in Table 5.

Table 5. Processing Sequence Used for Fabrication of Mesa Test Devices

Surface prep - *sandblast* - *NaOH etch* - *HCl:H_2O etch* - *HF:H_2O etch*
Diffusion - *$POCl_3$ source*
HF: H_2O etch
Aluminum paste back contact
Isolate devices by dicing
Test

The dicing step isolates devices from edge to edge across the sheet in areas of 0.2 cm^2. Testing includes Jsc, Voc, and Ln measurements (from quantum efficiency measurements). Additional characterization includes quantum efficiency spectra, EBIC imaging, LBIC imaging, dark I-V measurements, and capacitance-voltage measurements for estimations of base carrier concentration.

Causes Limiting Performance

Determining the causes that limit the minority carrier diffusion length has been the focus of an ongoing program to improve the Silicon-Film™ material. There are two main areas that are being examined: impurities and defects. The following sections will discuss each of these areas, and indicate the extent to which they may be limiting minority carrier diffusion in the present material.

Impurities

There are several ways that the presence of chemical impurities can deleteriously affect the quality of the material. The impurity may introduce an energy level in the vicinity of the midgap where it acts as a minority carrier trap, reducing minority carrier diffusion length. Alternatively, the impurity may introduce an energy level in the vicinity close to the conduction-band or the valence-band where it may act as an acceptor or donor, respectively, thereby controlling the conductivity of the material. The nature of the energy level introduced by the impurity is dependent on its location within the lattice (as a substitutional or interstitial). Furthermore, some impurities are subject to removal, or deactivation, as the consequence of subsequent processing, for example by

gettering or hydrogen passivation. Impurities may also interact with structural defects, or cause structural defects by precipitation.

There are two sources of impurities in the final Silicon-Film™ sheet material: (i) those introduced with the starting material, and (ii) those introduced from the growth system during layer growth. In Phase I, it was found that impurities were found in both the starting material and the finished sheet, however, it was concluded that these impurities had little effect on the photovoltaic properties of the material or were segregated to the top of the sheet and are removed by chemical processing during solar cell fabrication.

In Phase II, contaminants introduced by the feedstock material were an intermittent problem. In most cases, contaminated lots were identified and eliminated before they entered the wafer production machine. However, improvements to our feedstock preparation process for elimination of low level impurities will be required to attain the high yield goals of the Phase III program. Our plan for Phase III is to develop a QA/QC system for feedstock silicon so that a baseline feedstock quality is assured. Impurities introduced from the growth system were also identified. Various particulates were found to either excessively dope the Silicon-Film™ material or act as point shunts. In all cases, the impurities were identified and eliminated.

Defects

Crystalline defects can be the source of electrically active regions in the crystalline lattice that deleteriously affect the minority carrier diffusion length. The three main categories of crystalline defects include planar defects (e.g. grain boundaries), line defects (e.g. dislocations), and point defects (e.g. silicon vacancies and interstitials). Since the grain size of Silicon-Film™ material is in the range of 100 to 5000 μm, and minority carrier diffusion lengths up to 60 μm have been measured, it is not likely that grain size is the present limit to diffusion length.

During the Phase II program, we used defect and grain boundary decoration to determine the effect of growth parameters on crystal growth structure. With the help of this characterization technique, we were able to identify the existence and the cause of a critical performance-limiting defect. Figure 8 shows a cross-section of a crystal structure harboring this defect (called a "puddle grain" because of its appearance). This cross-section was etched with SECCO etch consisting of 0.15 M K_2CrO_7:HF (1:2). Note that along the grain boundary is a highly defected interface marked with arrows. Figure 9 shows a photomicrograph of an EBIC image of a mesa device whose area includes a "puddle grain". Note the wide "dead" region around the grain boundary. These grains lower the open circuit voltage of the device. The mesa of Figure 9 had an open circuit voltage of 321 mV and a short circuit current of 14 mA/cm^2, whereas surrounding mesas with no puddle grains had Voc's of 510 mV with similar currents. These mesas had no performance enhancement features such as AR, front contacts, hydrogenation, or surface passivation.

Figure 8. Cross-section of silicon sheet showing a "puddle grain" (100X magnification)

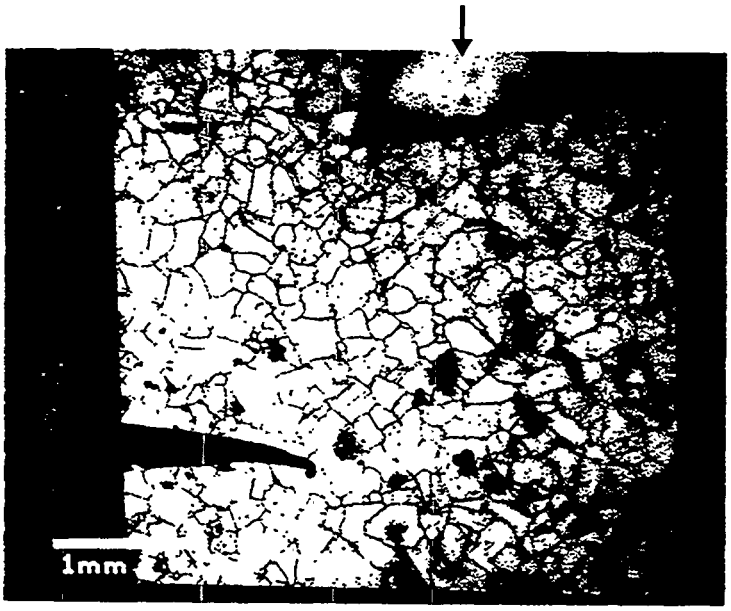


Figure 9. EBIC image of a solar cell mesa with a "puddle grain" (indicated by arrow)

Through hypothesizing the mechanism of grain growth for this particular grain structure and subsequent changes to the "Z" direction thermal profile in the liquid zone, this defect was eliminated. Elimination was verified by both surface and cross-section inspection of the Silicon-Film™ sheets.

Spatial Uniformity

The fabrication of large area photovoltaic solar cells requires the availability of large areas of material that possess uniform electrical and physical properties. Moreover, it is necessary to accomplish spatial uniformity with all subsequent processing of the material on its way to becoming an active device. This section describes the spatial uniformity of the material resistivity and device performance achieved with the present Silicon-Film™ process.

Material Properties

Figure 10 shows Xbar and range charts of the resistivity of undoped wafers grown at an areal generation rate capable of 2.3 MW/yr. Resistivity was measured by four point probe method.

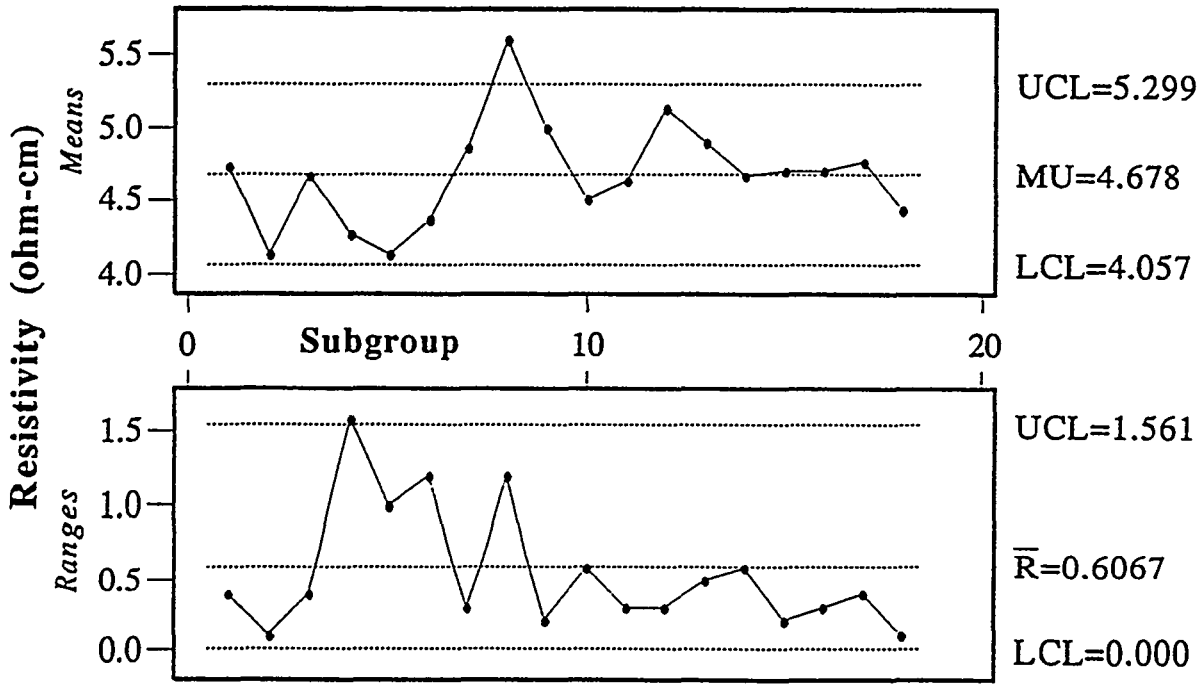


Figure 10. Resistivity Xbar and R charts for wafers fabricated during a 3 hour Silicon-Film™ production run at an areal generation rate capable of 2.3 MW/yr

Device Properties

Small area (0.2 cm^2) test devices are fabricated and evaluated on a continual basis to determine spatial uniformity of device properties across the width of the Silicon-Film™ sheet. Figure 11 shows a representative profile of diffusion lengths measured on test devices across the width of Silicon-Film™ sheets from three different production runs. Figure 12 shows a profile of Voc*Jsc products measured on test devices across the same Silicon-Film™ sheets as represented in Figure 11.

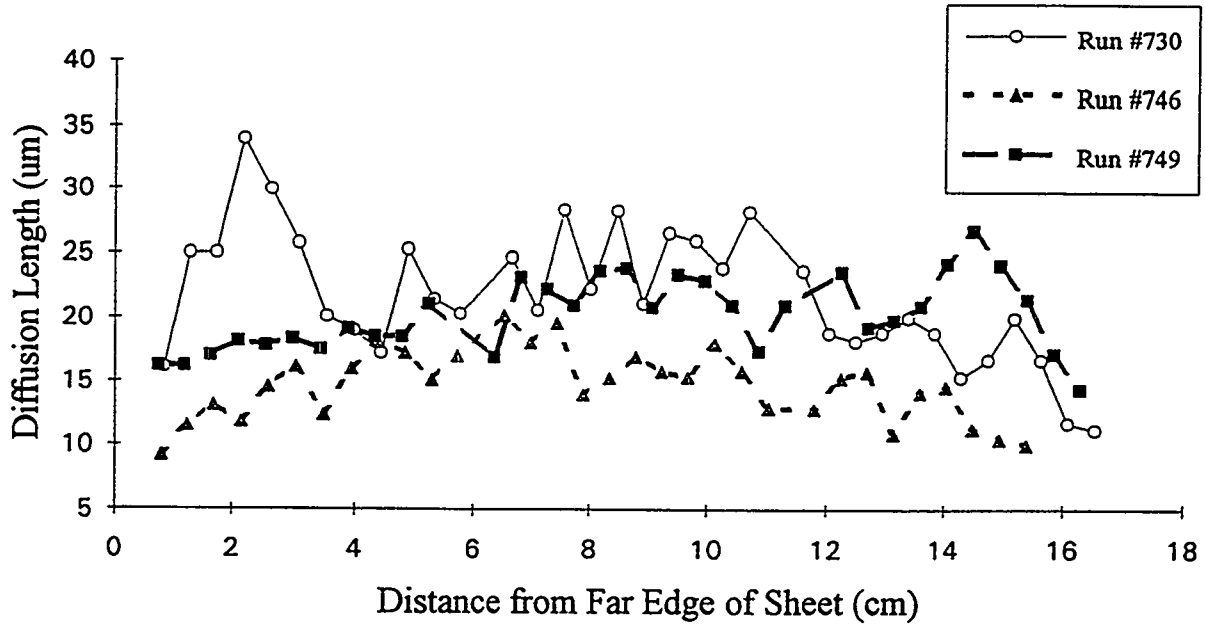


Figure 11. Diffusion length measurements on test devices fabricated across the width of Silicon-Film™ sheets demonstrating current level of spatial uniformity

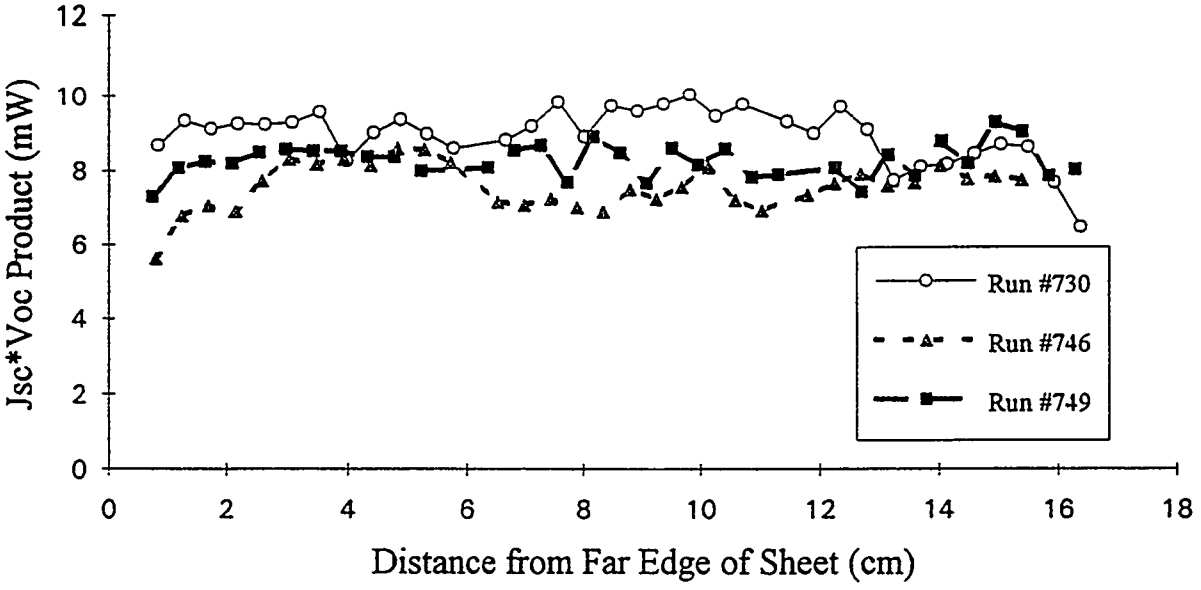


Figure 12. Voc*Jsc from test devices fabricated across the width of Silicon-Film™ sheets demonstrating current level of spatial uniformity

Note that the measurement error on our diffusion length estimates via QE is 10% which may account for some of the jagged edges in Figure 11. Efforts are continuing to both increase and smooth the level of the performance across the sheet. Data show that the thermal profile across the width of the sheet can be improved, and plans for improvement are built into the design of the Phase B production machine.

Statistical Process Control (Task 11)

Material quality was monitored using SPC methods on performance data from small area test devices. However, because the purpose of many of the material production runs was to determine the effect of parameter changes, the control charts that were generated were an exercise in using SPC rather than being representative of a controlled process. An example of a control chart for test devices generated during Phase II is provided in Figure 13.

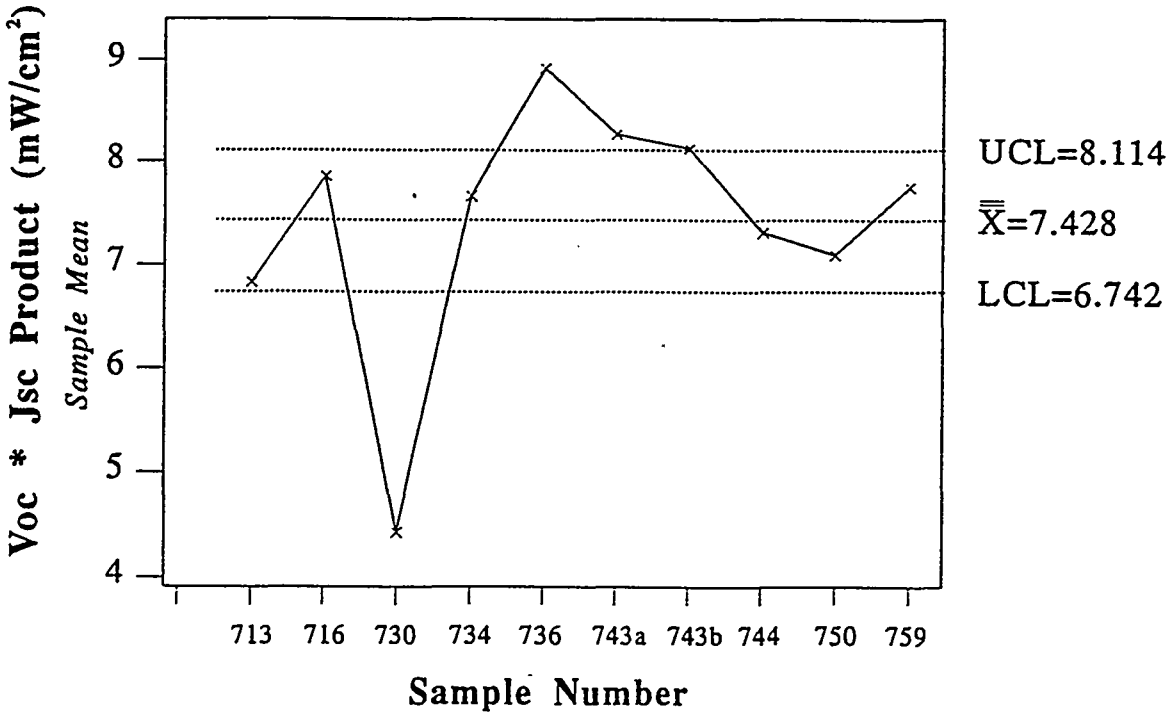


Figure 13. Xbar chart for Jsc*Voc measurements for similar production runs

Solar Cell Fabrication Process

Improvements in Solar Cell Efficiency (Task 12)

During Phase II, the development of a solar cell fabrication process was split into two parallel efforts: (i) a baseline process, and (ii) a champion cell process. This parallel approach allowed us to develop a sound manufacturing baseline process while still attaining Phase II performance goals with champion cells. In Phase III, we will continue parallel efforts while investigating next generation processes for possible incorporation into the baseline process.

Baseline Solar Cell Process Sequence

The baseline solar cell process, listed by step in Table 6, was developed using 10 cm x 10 cm wafers. These wafers produce cells that are representative of the 15 cm x 15 cm cells, but are easier to handle in test investigations (e.g. less chemicals expended, smaller diffusion tube, less ink). By the end of Phase II, 15 cm x 15 cm wafers in lots of 100 were fabricated with the baseline process.

Table 6. Steps in the Baseline Solar Cell Fabrication Process

Process Steps
1) Surface Preparation
2) Gettering Diffusion
3) Etch Gettered Junction
4) Standard Shallow Junction Diffusion
5) PSG Removal
6) Print/Dry/Fire Back Aluminum paste over entire back Ag (98%)/ Al (2%) bus bars
7) Print/Dry/Fire Front Silver ink grid
8) Isolate edges
9) H+ Passivation
10) AR Coating
11) Test

These steps did not change from Phase I to Phase II, but, the process parameters within the steps were optimized. Experimentation for optimization of the parameters is discussed in each of the following sections.

Surface Preparation

Throughout Phase I of this program, surface preparation of the wafers involved a CP (Chemical Polish) etch. Efforts were made to eliminate this etchant from the baseline process due to its expense, hazard during use, and the resulting waste product requiring disposal. Sandblasting followed by etching with NaOH was found to effectively replace the CP etch. Cost benefits of this development are described in a following section titled 'Materials Costs Reduction'.

Diffusion Process and Front Contact Enhancements

Development of a baseline solar cell fabrication process has included investigations involving optimized diffusions, gettering processes, and reduced shading of the front contact. A summary of the effects of these changes on 100 cm^2 Silicon-Film™ wafers can be seen in Table 7.

Table 7. Median Performance and *(Standard Deviation)* as a Function of Processing of 100 cm^2 Silicon-Film™ Solar Cells

Process Description	# of Cells	Voc	Isc	FF	Power
Phase I Baseline	8	0.532 *(0.67%)*	1.656 *(1.656%)*	62.13 *(2.20%)*	0.550 *(2.68%)*
Shallow Diffusion, Gettered, Fine-Line Screen	11	0.542 *(1.17%)*	1.787 *(0.87%)*	63.16 *(7.21%)*	0.609 *(8.29%)*

To obtain low contact resistance with screen printed contacts, high surface dopant concentrations are required. These high concentrations can lead to current losses due to recombination in the emitter layer. We have investigated altering the diffusion sequence to investigate this trade off. The resulting "shallow" diffusion has resulted in higher currents and voltages and no significant increase in series resistance effects.

A phosphorus gettering process has also been investigated that generates significant increase in red response through increased diffusion length. The gettering process involves putting the wafers through a high temperature step in the presence of phosphorus, then stripping a thin surface layer of silicon, then diffusing the wafers in the conventional fashion.

The front contact is a screen printed silver paste. A screen printing mask is being investigated that has grid lines 60% as wide as the production standard. With further screen-print process optimization, the use of this mask is expected to result in a 4% increase in current due to less shading.

The data in Table 7 indicates that the optimized process is 10% higher in power than the control group. This boost is due to the combined effects of the process changes listed above. Significant room for improvement still exists in all three areas of device performance addressed here (blue response, red response, and shading).

Hydrogenation

Both Kaufman ion source hydrogenation and PECVD hydrogen passivation processes were used during Phase II to improve solar cell performance. In general, it was found that Kaufman source hydrogenation significantly improved diffusion length and red response, but also caused permanent surface damage. This damage lowered blue response, resulting in no net change in short circuit current. Figure 14 shows the internal quantum efficiency (IQE) before and after Kaufman hydrogenation. PECVD hydrogen passivation led to modest gains in diffusion length with less permanent surface damage and significant improvements in short circuit current. As a result, we currently use PECVD hydrogen passivation in our baseline solar cell fabrication process. Figure 15 shows a much improved quantum efficiency curve resulting from improvements in material quality and processing. Processing improvements included a low power PECVD hydrogen passivation step directly before front contact deposition followed by a low power CVD oxide deposition step [7].

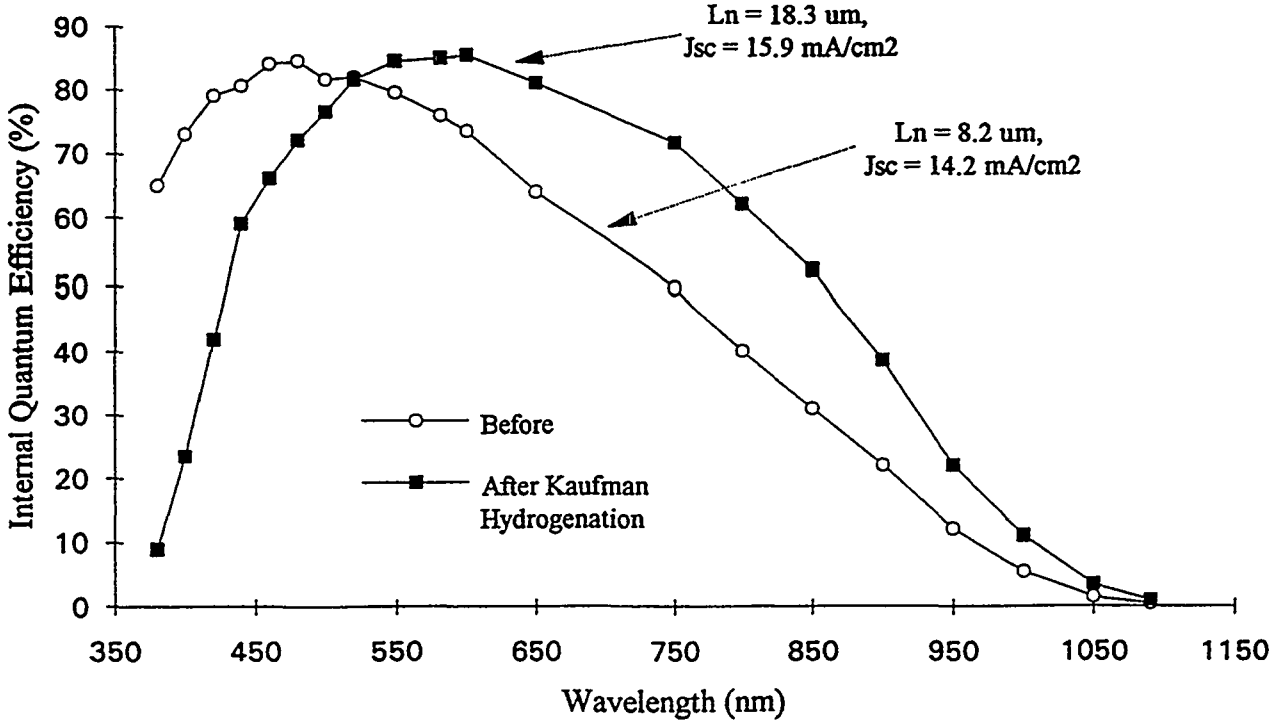


Figure 14. Internal quantum efficiency curves of a Silicon-Film™ solar cell before and after Kaufman hydrogenation

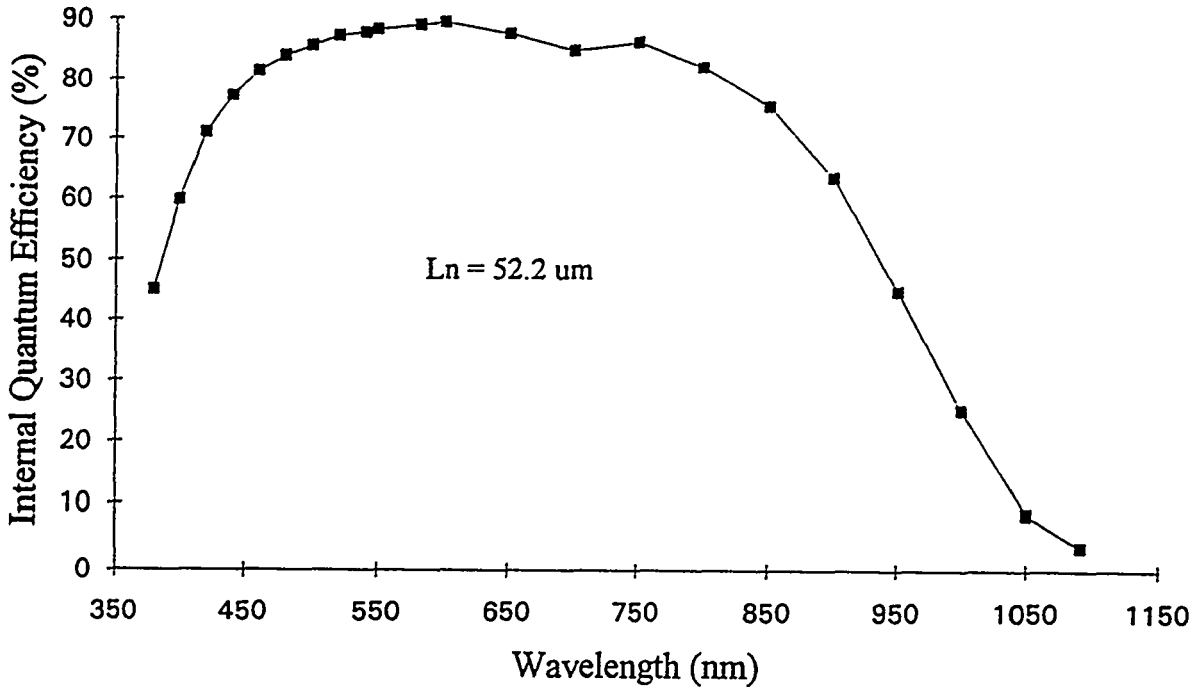


Figure 15. Improved quantum efficiency resulting from improvements in material quality and processing

Anti-Reflection Coating

Two anti-reflection coating processes were investigated for the baseline Silicon-Film™ solar cell process: (i) TiO_X spray pyrolysis method ("spray") which is presently used in our standard solar cell production process, and (ii) PECVD Si_3N_4 process. A sample of 10 cm x 10 cm Silicon-Film™ wafers were fabricated into solar cells using our baseline process. Part of the samples underwent spray AR the other part underwent the PECVD process. The median gain derived from each of the AR processes is given in Table 8. Note that the starting sample of wafers were from two different feedstocks of raw material.

Table 8. Average Gain and (*Standard Deviation*) in Solar Cell Performance as a Function of Anti-Reflection Coating Process

Feedstock ID	# of Samples	Method	Voc	Isc	Power
A	7	Spray	1.006 *(0.005)*	1.319 *(0.028)*	1.321 *(0.058)*
A	8	CVD	1.014 *(0.005)*	1.360 *(0.014)*	1.413 *(0.037)*
B	5	Spray	1.042 *(0.006)*	1.382 *(0.021)*	1.518 *(0.041)*
B	6	CVD	1.041 *(0.011)*	1.397 *(0.014)*	1.541 *(0.036)*

A comparison of the two methods indicates that the production spray method offers similar gains in power to the CVD method. Because the TiOx coating is better matched to the EVA used in module packaging, the "sprayed" wafers are expected to increase a further 6% with module encapsulation. The difference in gains due to feedstock is believed to be due to the effect of contaminants inherent to Feedstock A.

An automated spray anti-reflection coating machine for handling AP-225 wafers is currently under fabrication. In terms of throughput, this new machine will offer over 400 cells per hour of 15 cm x 15 cm solar cells. Larger sample studies than that presented in Table 8 will be conducted to confirm these initial results. Because of the low throughput of CVD-deposited AR processes, comparable performance gains by spray AR would represent a significant manufacturing-line achievement.

Forming Gas Anneal

Another Phase II objective was to understand and quantify the role of forming gas anneal as a potential replacement for hydrogenation in upgrading the quality of Silicon-Film™. A research group at Georgia Institute of Technology led by Ajeet Rohatgi performed a study to assist us in this. The process they used and a summary of their results follows.

Phosphorus diffusion on the front and aluminum treatment on the back were used for gettering, which also form the n^+-emitter and p^+-back surface field, respectively. Thus, gettering is an integral rather than additional part of the cell process sequence. Phosphorus gettering was performed at 930 °C for 25 minutes, using a P_2O_5 solid source. In order to take advantage of phosphorus gettering without paying the penalty of heavy doping effects in the emitter, a controlled etch-back technique was used to partially etch the n+-region. A 20 minute HNO_3:HF:H_2O(1000:1:100) etch was used to increase the emitter sheet resistance from 16 Ω/□ to 80 Ω/□.

Aluminum gettering was performed by evaporating 1μm thick Al on the back of the cells followed by a high temperature drive-in for 35 minutes. Oxide passivation was done during the Al drive-in. After the Al evaporation on the back of the wafers, samples were inserted at 850 °C in the oxygen ambient to first grow an approximately 100 angstrom thick oxide on top of the n^+ emitter region. After 5 minutes of oxide growth, the gas ambient was switched to nitrogen for an additional 30 minute Al drive-in. After the 850 °C aluminum diffusion, the temperature was ramped down to 400 °C in nitrogen and the cells were annealed for an additional two hours in nitrogen or forming gas (10% hydrogen in nitrogen).

This experimental strategy resulted in a matrix of cells with and without forming gas anneal. The front grid contact was formed by evaporation of titanium/silver (600 Å/600 Å), a lift-off technique, followed by 5 μm silver plating. The back contact was formed by evaporation titanium and silver on top of the Al BSF contact region. Contacts were annealed in either nitrogen or forming gas ambient for 45 minutes at 400 °C. Finally, a 600Å SiN/ 950Å SiO_2 double layer AR coating was deposited by PECVD technique on the cells.

Testing at the Georgia Institute of Technology indicated that the cells with the forming gas anneal had a short circuit current 5.5% higher than the cells that went through the nitrogen-only processes. Figure 16 shows the IQE response of forming gas and nitrogen annealed cells, which supports the higher diffusion length in the FGA cells. Estimates of the effective diffusion length based on these curves are 18 microns for the nitrogen-only cell, and 31 microns for the FGA cell. These cells were sent to Sandia for confirmation of the test results. The Sandia test results are summarized in Table 9.

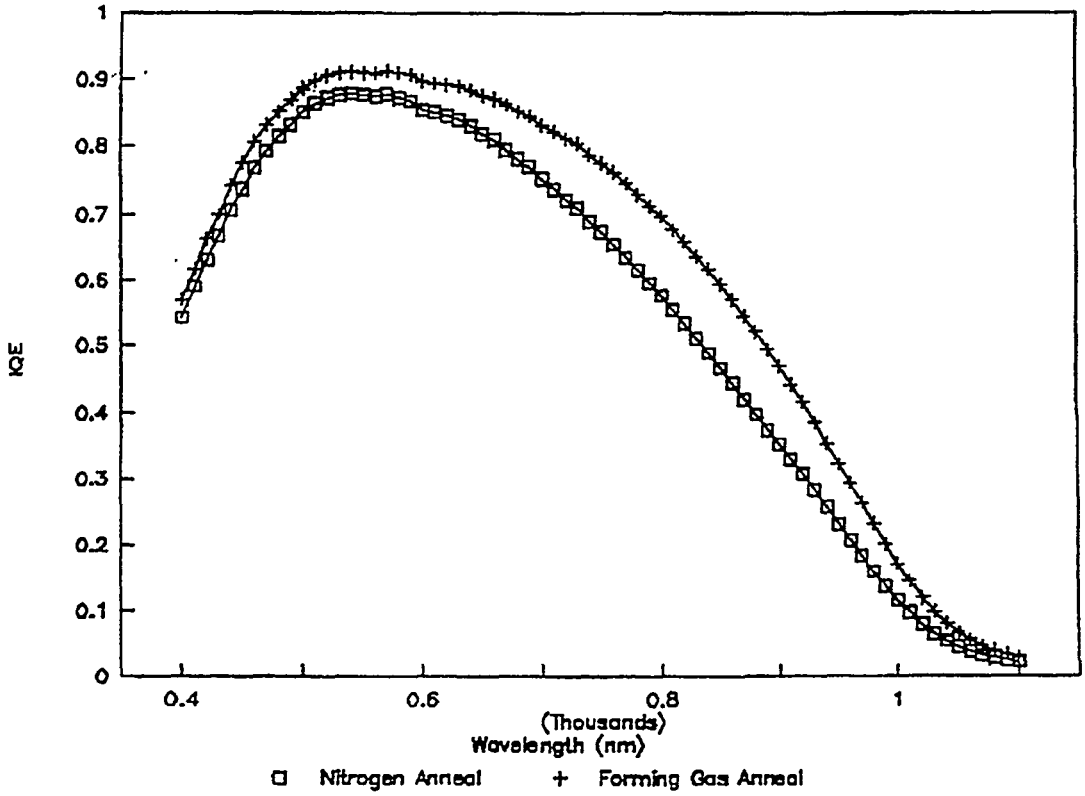


Figure 16. IQE response of forming gas versus nitrogen anneal

Table 9. Sandia Test Results on Silicon-Film™ Solar Cells Fabricated by Georgia Institute of Technology

Anneal Ambient	Voc (mV)	Isc (mA/cm2)	FF	Efficiency
FGA	517	27.1	.717	10.1%
Nitrogen Only	498	25.7	.552	7.0%

The nitrogen-only sample was damaged in post processing and many of the grid lines were lost which led to the poor fill factor on that cell. Sandia also performed spectral response tests which

confirmed that the red response was enhanced on the FGA samples. The Sandia spectral response testing also indicated that red response increased when a white light bias was applied.

Deliverables - Champion Cell Process

A "Champion Cell" process was used to fabricate the deliverables for the Phase II program. This process changed through the project, incorporating the best of newly developed processes. The main difference between the baseline process and the champion cell process was evaporated contacts instead of screen-printed contacts. As previously mentioned, the screen-printed contact technology is one of the most critical processes in developing a low cost manufacturing line. The solar cell contact technology can be tailored to effect the most significant cost savings, and is critical to the performance of the finished product. While the screen-print process was under development, we achieved Phase II deliverable goals using evaporated contact technology.

To meet the module deliverables for Phase II, we started with 181 wafers, 155 solar cells made it to wafer test, and 143 wafers tested provided 2 or more watts under standard test. The performance distribution of the 155 solar cells is shown in Figure 17.

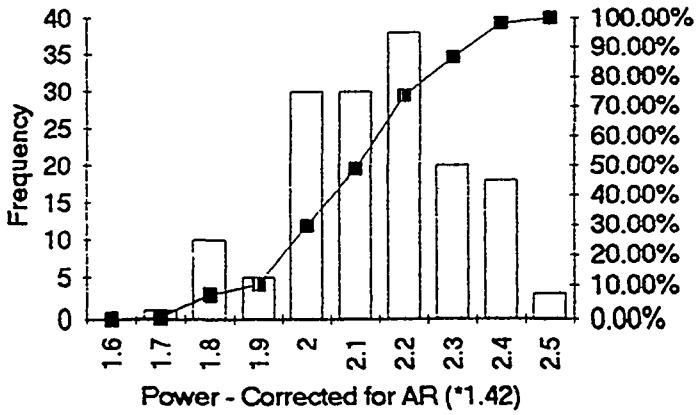


Figure 17. 155 wafers fabricated for the Phase II deliverables including two 36 cell modules and several individual cells

Materials Cost Reduction (Task 13)

The purpose of this task was to reduce the material costs of the Silicon-Film™ solar cell process and reduce the hazardous waste produced. This task was accomplished in two different areas:

1. reduction in caustic chemical usage by:
   - changing the surface preparation process,
   - extending the life of required etchants.
2. developing a fine-line front contact design and process

Table 10 shows the costs of using the chemical polish (CP) etchant for surface preparation before diffusion. As shown in Table 11, a significant cost savings (67%) was realized in changing to a sandblast and NaOH surface preparation process.

Table 10. Costs of Surface Preparation with CP Etchant Before Diffusion

Material	Cost/unit ($)	Units Consumed	Wafers/unit	Cost/wafer ($)
Hydrofluric Acid	0.44	9.4	50	0.0830
Nitric Acid	8.12	2	50	0.3248
Acetic Acid	6.72	0.5	50	0.0672
DI Water	0.024	15	50	0.0072
Sodium Bicarb	0.356	20	50	0.1424
Direct Material per wafer				0.6246
Direct Labor per wafer				0.1600
Total Cost of Process per wafer				0.7846

Table 11. Costs of Surface Preparation with CP Etchant Replaced by Sandblasting and NaOH

Material	Cost/unit ($)	Units Consumed	Wafers/unit	Cost/wafer ($)
Sandblast	0.75	21.6	1800	0.0090
NaOH	1.99	66	1800	0.0730
Muriatic Acid	0.10	100	1800	0.0055
HCl	7.8	12	1800	0.0520
HF	0.44	12.5	3000	0.0018
DI Water	0.024	200	1800	0.0027
Sodium Bicarb	0.356	8	3000	0.0009
Direct Material per wafer				0.1449
Direct Labor per wafer				0.0533
Total Cost of Process				0.1982

Paths to additional cost savings were identified: (i) monitoring the strength of the NaOH solution and replenishing the bath prior to etch exhaustion, and (ii) removing reaction by-products from the solution as they began to accumulate. These practices extend the life of the bath and allow us to process more wafers per milliliter of etchant than was previously possible. We have not yet integrated these improvements into the standard process or determined the exact reduction in cost. These tasks are planned for Phase III. Further cost savings are expected following automation and improvements to the wet chemical process station.

Device Equipment/Process Automation (Task 14)

Plans for process automation focused on two areas: Si_3N_4 deposition for anti-reflection coatings and wet chemical etching for wafer surface preparation. Significant progress was made in both areas. An in-line Si_3N_4 CVD system has been designed for the Silicon-Film™ 15 cm x 15 cm solar cell process. This design has been evaluated by an internal engineering group and outside equipment fabrication firms. Quotations have been received, but no final decision has been made. As previously discussed we are also working on an automated spray anti-reflection coating machine. The automated spray technique has higher throughput with comparable performance gains.

CECON, Chemical and Engineering Consultant Network, has evaluated the wet chemical process and equipment used for surface preparation of the Silicon-Film™ wafers. They have identified key problem areas and proposed a basic action plan. A proposal for automating the wet-chemical process station is currently in negotiation.

Advanced Module and Panel Design (Task 15)

Advances in Solar Cell Tabbing for Improved Performance

Early in Phase II, a reduction in fill factor after tabbing was a recurring problem. Tabbed solar cells experienced a reduction in fill factor as high as 10% from the original un-tabbed test. For the fabrication of the deliverables, the reduction in fill factor after tabbing was reduced to less than 1% by improving the tabbing material. For individual cells, 20 gauge copper wire was used instead of the standard soldered copper ribbon for the front tabbing material which is over three times the cross-sectional area of the standard-sized tabbing ribbon. For the backs of individual cells, we used 3 (instead of 2) tabbing ribbons which were 2.5 times wider than the standard back ribbon.

For cells in the module deliverables, thicker tabbing ribbons were used on both the fronts and the backs. Two ribbons, 0.4 cm wide and 0.0127 cm thick, were used with a total shading of 8%.

Design and Prototyping of Large Modules

Two large area modules were delivered to NREL during Phase II. Both were measured by NREL and were specified as a 71.3 watt and a 78 watt modules. These modules had total areas of 0.95

m2. The performance parameters for these modules were presented in Table 3. A photograph of the 78 watt module is shown in Figure 18.

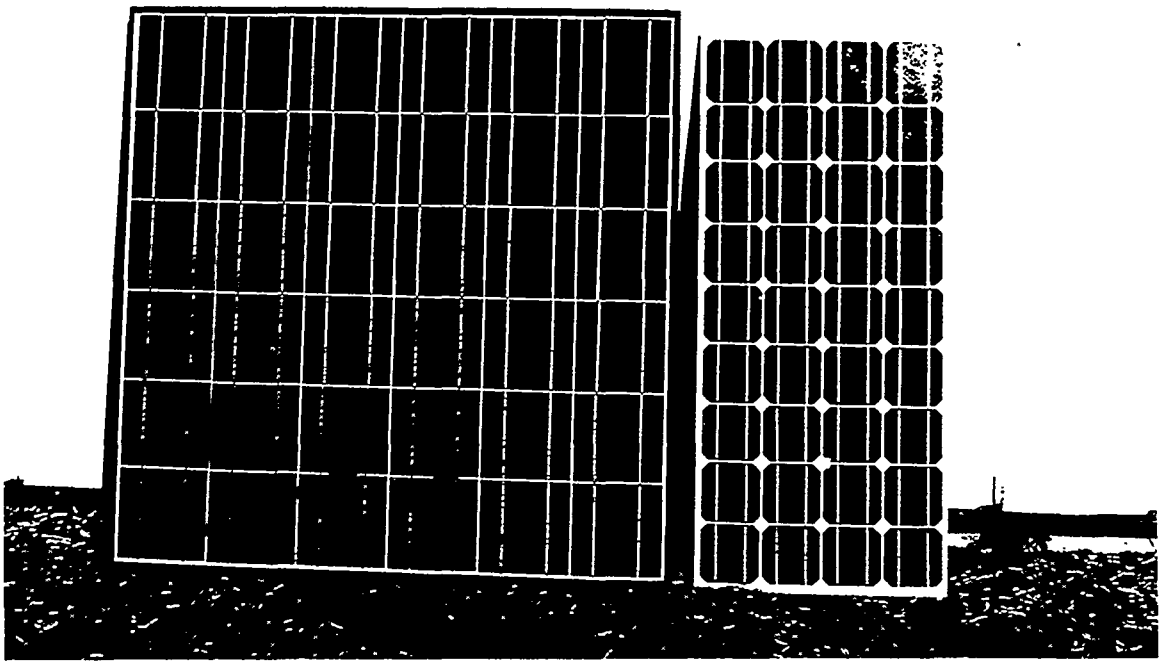


Figure 18. Photograph of a 78 watt, 0.95 m^2 Silicon-Film™ module (left) next to a conventional module, each comprised of 36 solar cells

Next Generation Module Design

The material cost percentage for PV module packages based on the present design will be about 85% of the total cost for the module assembly step. Table 12 shows a breakdown of the direct material cost contribution on a $/$m^2$ basis. The first column shows the costs for the standard package with extruded aluminum frame and 100 cm^2 solar cells. The second column shows the cost for an unframed package which is panelized using steel sections bonded with adhesive to the back for support and attachment to the array structure. The third column shows the cost reduction by the use of larger solar cells in a larger module. The improvement comes from the reduction in the cost of the electrical interface.

AstroPower has an active program with The Dow Chemical Company to design the next generation module--an all plastic module. The fourth column of Table 12 shows the plan for cost reductions. The goal is a 50% cost reduction in materials over the large frameless module (column 3).

Table 12. Cost Reduction Opportunities for Advanced PV Packaging Implementation of All Plastic Module

Package Material Costs	Standard with frame 0.45 x 0.96	Frameless 0.45 x 0.96	Frameless (large) 0.9 x 1.36	Advanced (All Plastic) 0.9 x 1.36
Component/Material	*Cost, $/m²*			
Glass	11.77	11.77	11.77	[a,b]
EVA	13.38	13.38	13.38	[c]
Backsheet	9.00	9.00	9.00	[d]
Frame	24.15	------	------	[b,e]
Gasket	2.24	------	------	[b]
Ribbon	3.92	3.92	3.92	[f]
Solder	4.59	1.00	1.00	[f]
J-Box Molding	7.88	7.88	2.76	[e]
J-Box Hardware	1.16	1.16	0.41	[e]
Diode	1.17	1.17	0.40	[e]
RTV	2.21	2.21	0.77	[b]
Screws	0.91	0.91	0.31	[b]
Panel Support	------	9.54	9.54	[g]
Total	82.38	61.94	53.26	25.00

Examples for Potential Improvements:

[a]: Replace glass with fluorinated polymer film for front cover

[b]: Rigidity provided by RIM, frame
Array attachment point provided on frame
RTV eliminated as j-box bonding adhesive
Gasket eliminated

[c] Reduce EVA usage by 50%, 0.91 mm ⇒ 0.46 mm
Continuous lamination

[d] Consider simpler back sheet structures

[e] RIM frame incorporates integrally molded j-box
All electrical hardware and connections contained in RIM molding

[f] Replace interconnects with conductive graphite fiber and conductive graphite epoxy.
Eliminate hazardous waste from silver cleanup

[g] Panel support function provided by RIM support members.

Module Equipment/Process Automation (Task 16)

During Phase II, a large area laminator was built with a lamination area of 111.8 cm by 135.9 cm. This laminator was used in packaging the 36 cell modules delivered in Phase II and will laminate the 170 watt modules to be packaged in Phase III. Jigs for stringing and lay-up were designed with plans for near-term fabrication.

References

[1] A.M. Barnett, M.G. Mauk, J.C. Zolper, R.B. Hall, J.B. McNeely, *Technical Digest of 1st International PVSEC*, Kobe, Japan (1984) pp. 241-244.

[2] A.M. Barnett, R.B. Hall, D. Fardig, J.Culik, *Proceedings of the 18th IEEE Photovoltaic Specialists Conference*, Las Vegas, Nevada (1985) pp. 1094-1099.

[3] Measurement by SERI; data taken November 19,1986.

[4] Measurement by Sandia National Laboratories, included with June 1, 1987 letter from P.A. Basore.

[5] A.M. Barnett, F.A. Domian, D.H. Ford, C.L. Kendall, J.A. Rand, M.L. Rock, R.B. Hall, *Technical Digest of the 4th International PVSEC*, Sydney, Australia (1989) pp. 151-158.

[6] C.L. Kendall, J.C. Checchi, M.L. Rock, R.B. Hall, and A.M. Barnett, "10% Efficient Commercial-Scale Silicon-Film Solar Cells," *Proceedings of the 21st IEEE Photovoltaics Specialists Conference*, Orlando Florida (1990), pp. 604-607.

[7] Z. Chen, S.K. Pang, K. Yasutake, and A. Rohatgi, *Journal of Applied Physics* 74(4) (1993), p. 2856.

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S. R. Collins, R. B. Hall

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13. ABSTRACT *(Maximum 200 words)*

This report describes work to develop an advanced, low-cost manufacturing process for a new utility-scale, flat-plate photovoltaic module. The process starts with the production of continuous sheets of thin-film, polycrystalline silicon using the Silicon-Film™ process. Sheets are cut into wafers that are nominally 15 cm x 15 cm. Fifty-six of these wafers are then fabricated into solar cells that are strung together in a 170-W module. Twelve of these modules form a 2-kW array. The program has three main components (1) to develop a Silicon-Film™ wafer machine that is capable of manufacturing wafers that are 225-cm^2 in size with a total product cost reduction of 70%; (2) to develop an advanced solar cell manufacturing process that is capable of turning the Silicon-Film™ wafer into a 14%-efficient solar cell; and (3) to develop an advanced module design based on these large-area, efficient silicon solar cells with an average power of 170 W for 56 solar cells and 113 W for 36 solar cells.

14. SUBJECT TERMS

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