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SEQUENTIAL PURIFICATION AND CRYSTAL GROWTH FOR THE PRODUCTION OF LOW COST SILICON SUBSTRATES

Quarterly Technical Progress Report No. 5 for the Period January 1—March 31, 1981

By
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AND
SOLAR ENERGY RESEARCH INSTITUTE
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MOTOROLA PROJECT NO. 2376

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I. INTRODUCTION

The need for low cost silicon for solar cell applications has stimulated the study of direct purification of metallurgical-grade silicon(MG-Si). The technique of sequential purification of molten silicon was investigated.[1,2] The sequential purification steps included (1) physical separation of insoluble impurities, 2) reactive gas treatment, 3) slagging and 4) impurity redistribution using ingot pulling. The results have shown that the ingot pulling is the most effective step of the purification process. This has been predicted since the majority of metal impurities in silicon have very low segregation coefficients (from 10^{-2} to 10^{-6}). In theory the ingot pulled from the molten silicon will be two to six orders of magnitude lower in the metal concentration than that in the original silicon used for melting. By the same token the pulled ingots can be remelted and repulled. The purity of the silicon can be improved by another 2 to 6 orders of magnitude. The process can be repeated for further purification. The purpose of this paper is to report the purity, structural and electrical characteristics of silicon ingots obtained by various number of crystal pulling.

2. EXPERIMENTAL PROCEDURES

The polycrystalline silicon pulled (1-pull) directly from the MG-Si melts was used as feed stock for second crystal pulling (2-pull). The 1-pulled ingots contain non-uniform distribution of grain size along the crystal axis[1-2]. The seed end contains large grains with polygonal structure, while the tang end contains small grains with lamellar structure. The metallic impurities at the seed end are in the range of tens of ppm, while at the tang end are hundreds of ppm.

The 2-pulled ingots have also been used as feedstock for the additional pull (3-pull). The percents of melt pulled are approximately 60%, 80% and 85% for 1, 2, and 3-pulled crystals respectively. An NRC cyrstal puller was used with a melt size of 2 Kg. Occcasionally a Hamco 800 crystal puller was used for a larger melt size (4 Kg). The NRC puller produced 5.5 cm diameter crystals, while the Hamco produced 7.5 cm diameter crystals. The crystals were pulled along the <100> direction. The crystal growth was done in an argon ambient at one atmosphere pressure. The pull rate was in the range of 6 to 8 cm/hr. The crystal rotation rate was 19 rpm while crucible rotation rate was 7rpm.

The impurity concentration in silicon was measured by the spark source mass spectrometer. The structure of silicon wafers was characterized by chemnical etching/optical microscopic method and by X-ray topographic technique. A 4-point probe was used for the measurement of electrical resistivity. The majority carrier mobility was measured by the van der Pauw method.

Silicon wafers were further characterized by the formation of a p-n junction for photoresponse measurement. The junction was made by solid state diffusion of phosphorus impurity either directly into the silicon substrate or into the epitaxial layer. The sheet resistance of the N^+ layer is in the range of 20 to 40 Ω/sq. The junction depth is approximately 0.3μm. When an epitaxial layer is applied, it is 20 μ m thick with a resistivity of 2.5 Ωcm.

Two different types of devices were built for photoresponse measurement: (1) gated diodes with a size of 4.2×10^{-3} cm^2 per doide. 2) uncomplete solar cells with the sizes of one cell/wafer. The solar cells were only processed up to diffusion and mesa etch. Neither metallization nor AR coating was applied. Open circuit voltage (Voc) and short circuit current (Isc) were taken under a vertical illumination condition (AMI). The products of Voc and Isc is used as a parameter for the material evaluation.

3. EXPERIMENTAL RESULTS

3.1 Purity of Crystals

Two crystal from 1-pulled, four each from 2-pulled and 3-pulled ingots have been analyzed by spark source mass spectrometer. Table 1 lists the maximum impurity concentration found at the seed and tang ends of crystals. The concentration of impurities at the seed end of 1-pulled crystals is comparable with that at the 2-pulled or 3-pulled cyrstals with the exceptions of Fe, Al and C. This results agree with the previous finding analyzed by the emission spectrographs. The high concentration of impurities at the tang end of 1-pulled crystals is primarily due to the samples with a lamellar grain structure, which is due to the constitutional supercooling during the crystal pulling. The table also shows that the purity of ingots is progressively improved by each additional crystal pulling. However, the improvement in the 3-pulled ingots over 2-pulled ingots is not as dramatic as expected. This is probably due to the fact that the concentration in the 2-pulled crystals already approaches the defection limit of the instrument. The improvement in purity by each additional crystal pulling can be easily analyzed by taking the concentration ratio of two consecutively pulled crystals. Table 2 lists the ratio for the predominate elements found in MG-Si. This table shows that the second-pull effectively improves the purity at the tang end of crystals. It also shows that only slight improvement was made for the third-pull over the second-pull with the exception of Al. Since Al exhibits a low segregation coefficient (3×10^{-2}) as compared to other metal impurities ($<10^{-5}$), the reduction of aluminum concentration to 10^{-8} from the original value in MG-Si (10^{-2}) needs at least three crystal pulling process, if other purification methods are not applied during the crystal pulling. The results shown in Table 1 are quite agreeable with this prediction.

TABLE 1

Comparison of maximum impurity concentration in 1,2 and 3-pulled ingots analyzed by spark source mass spectrometer (ppm wt)

	1 PULL		2 PULL		3 PULL	
Element	Seed	Tang	Seed	Tang	Seed	Tang
Cd	0.16	0.44	0.16	0.16	0.16	0.16
Mo	0.10	0.96	0.19	0.19	--	--
Zr	--	13.0	0.04	--	--	--
Cu	0.02	.05	0.01	0.02	0.01	--
Ni	0.53	19.0	0.97	0.97	0.96	1.20
Fe	2.4	560.0	0.28	0.11	0.09	0.24
Mn	0.63	29.0	0.23	0.41	0.63	0.32
Ti	0.08	120.0	0.03	0.02	0.02	0.02
Ca	--	49.0	0.37	0.38	0.20	0.56
K	--	--	0.19	0.08	--	- -
Cl	2.3	2.4	0.01	0.01	0.01	0.01
P	1.6	3.7	0.74	0.74	0.45	1.20
Al	36.0	3300	5.2	8.2	0.02	0.03
Mg	0.27	36	0.05	--	0.08	0.16
Na	0.20	0.82	0.04	0.05	--	0.21
C	12.0	28	0.8	0.59	0.30	0.83
B	0.42	0.73	1.20	1.20	0.60	1.30

TABLE 2

Impurity ratio in Si ingots of each consecutive pull

	1-pull/2-pull		2-pull/3-pull	
Element	**Seed**	**Tang**	**Seed**	**Tang**
Cu	2	25	1	--
Fe	8.5	5.5×10^3	3	--
Mn	2.7	7.1×10^2	0.28	1.3
Ti	2.7	6.0 c 10^3	1.5	1
Al	6.9	4.0×10^2	2.6×10^2	2.7×10^2

3.2 Crystal Perfection

3.2.1 2-Pulled Crystals

The majority (over 75%) of the 2-pulled crystal are single crystals. Four growth facets are un-disrupted and distinctly present along the direction of crystal axis. This morphology is characteristically regarded by the crystal growers as "free-of-dislocations". X-ray topographic study revealed no dislocations at the seed end of the crystals. The etching study confirmed the X-ray work. However, wafers etched by a preferential etchant exhibit dull surfaces. Microscopic examination showed a high density of shallow etch pits on the surfaces. On the other hand, chemical etching and the X-ray studies have shown that the tang end of the "dislocation-free" crystals is not crystallographically perfect. Figure 1 shows the X-ray topograph of a silicon wafer cut from the tang end of a 2-pulled ingot. Figure 2 (a) is a higher magnification of Figure 1 taken at the center region of the wafer. This figure shows high strain field in the crystal lattice, which is primarily due to the precipitation of a second phase or impurities. Figure 2 (b) shows a higher magnification of Figure 1 taken at the periphery of the wafer. The line defects shown in this photograph are primarily dislocations.

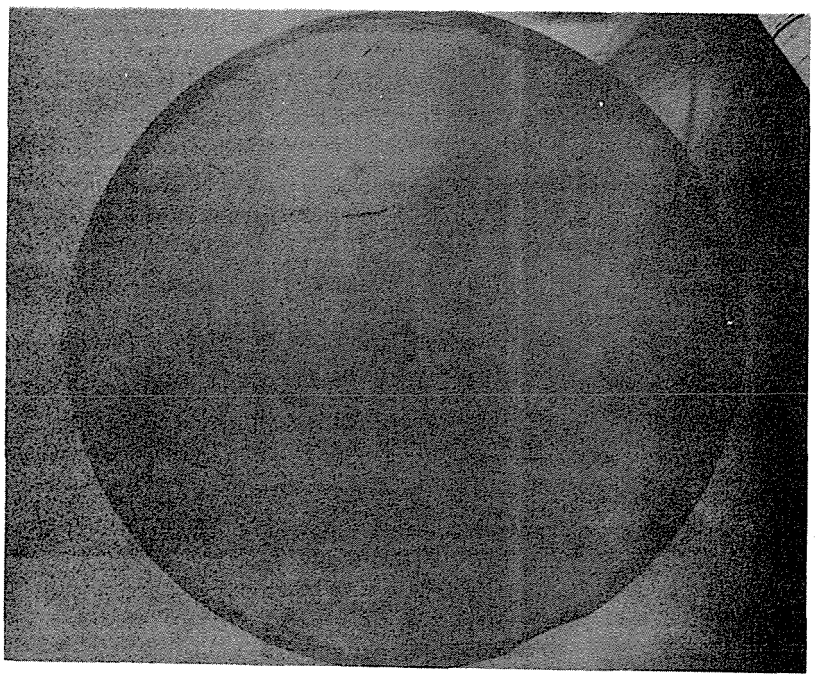
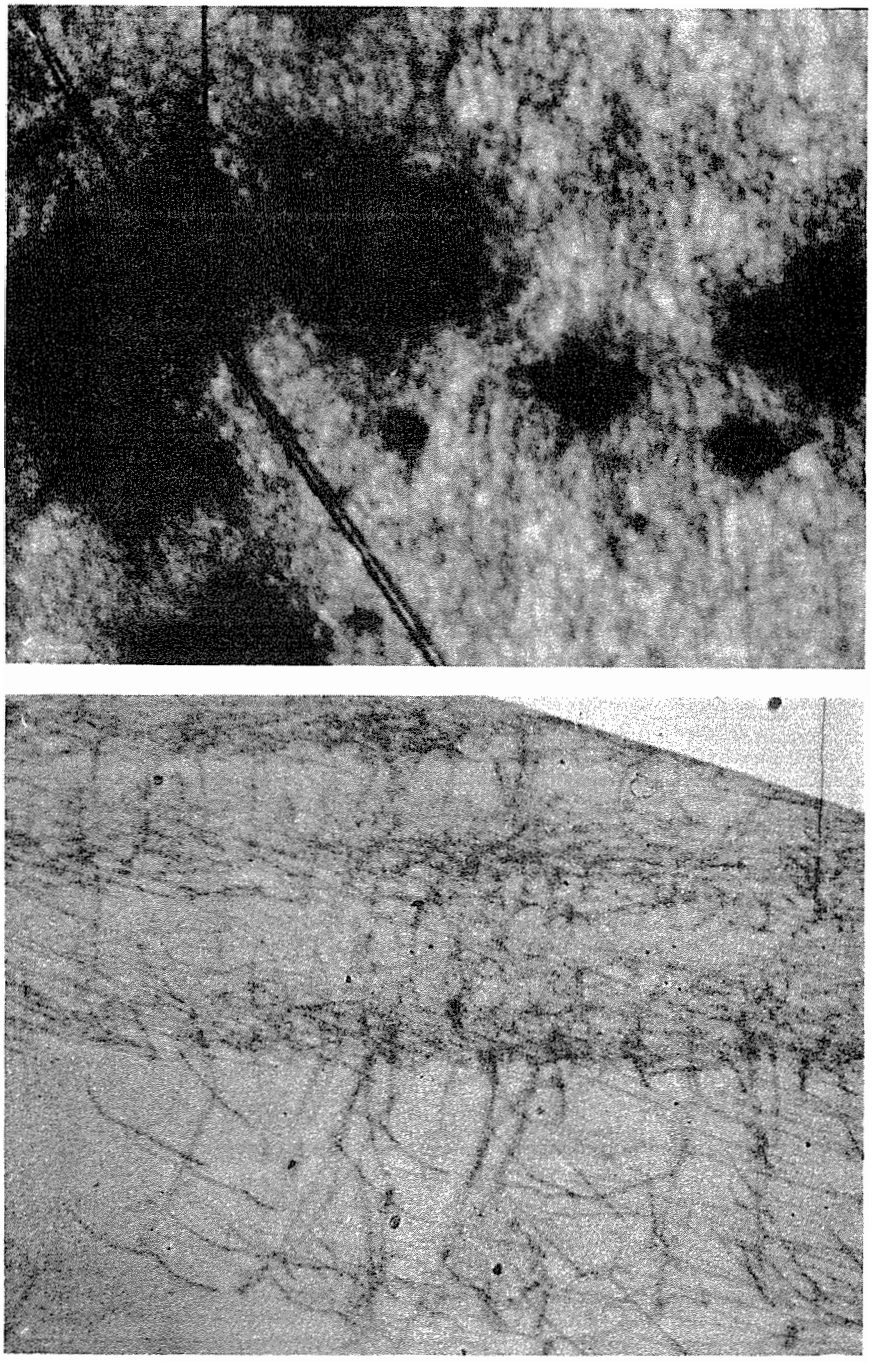


Figure 1. X-Ray topograph of a silicon wafer cut from the tang end of a 2-pulled ingot.



(a)

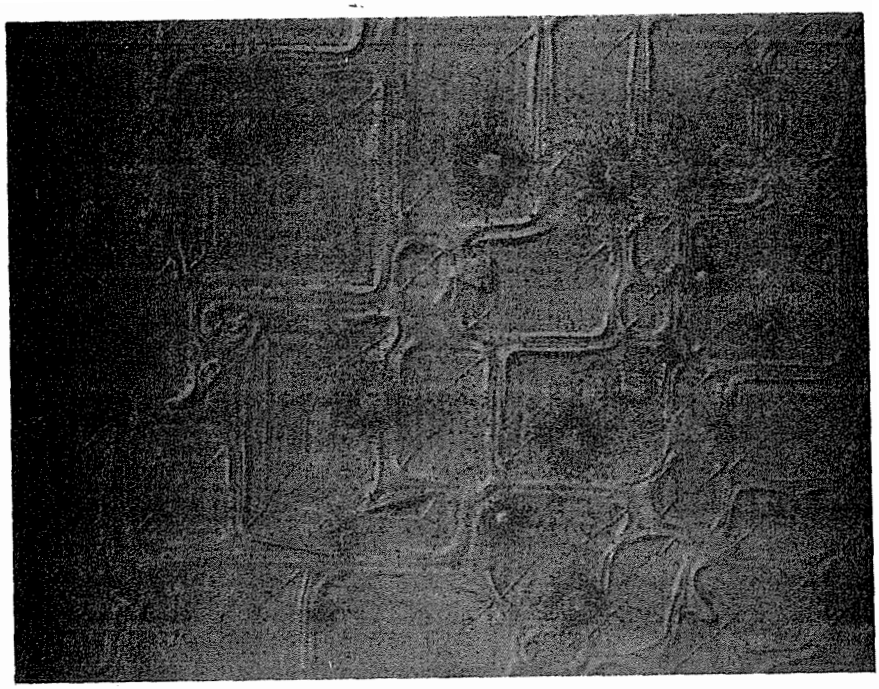
(b)

Figure 2. A higher magnification of Figure 1,
(a) center region of the wafer,
(b) periphery region of the wafer

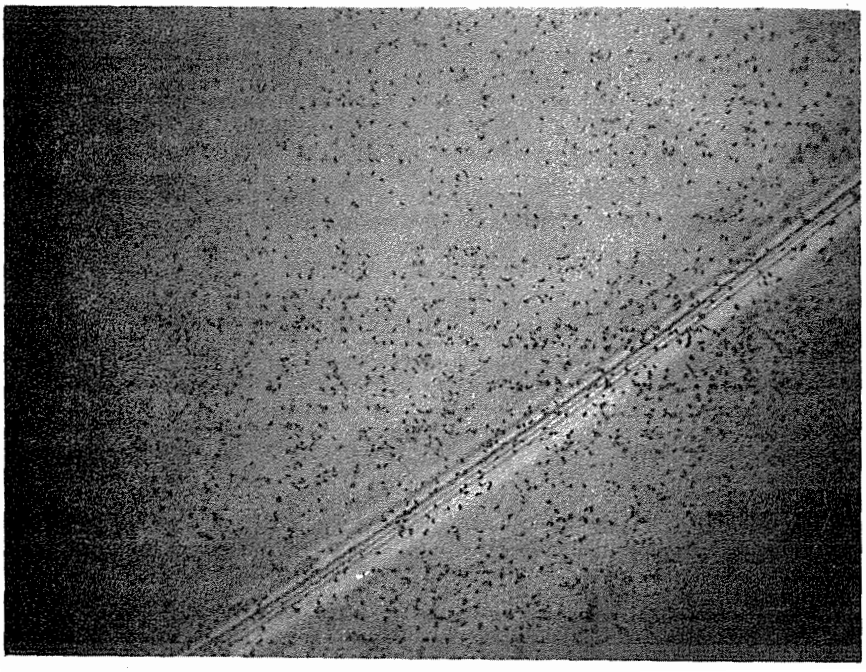
A better insight to these crystal imperfections exhibited at the tang end of 2-pulled crystals was obtained from chemical etching studies. Figure 3 (a) shows the etched surface taken from the center region of the wafer shown in Figure 1 . Three types of crystalline defects are revealed: (1) cellular cells with square or rectangular shape of irregular sizes. The formation of the cellular cells resulted from the constitutional supercooling of the melt. (2) precipitates of impurities which are located either within the cellular cells or at the edge of the cells. (3) dislocations which surround the precipitates and are manifest as small dark pits by the chemical etching. The formation of dislocations are likely due to the relief of lattice strain created by the impurity precipitates. Chemical etching reveals the same result as the X-ray topograph at the edge of wafer. Figure 3(b) shows the dislocation pits observed at the edge of the same wafer.

3.2.2 Three Pulled Crystals

Crystal perfection of the 3-pulled cyrstal shows considerable improvement over that of 2 - pulled crystals. Dislocation-free crystals can be consistently grown. The tang end of the 3-pulled crystals exhibit neither cellular-cell structure nor precipitates. However, the shallow etch pits still remain. Figure 4 (a) show a surface etched by Wright etch for 10 minutes followed by Sirtl etch for 3 minutes. Two types of shallow etch pits are found. One is the larger in size and distributed not uniformly. The other is smaller in size and distributed uniformly over the entire surface. The density of the small shallow etch pits approaches 10^8 cm^{-2}. This type of shallow etched pits are also observed on heavily doped semiconductor grade(S.G.) wafers as shown in Figure 4 (b).

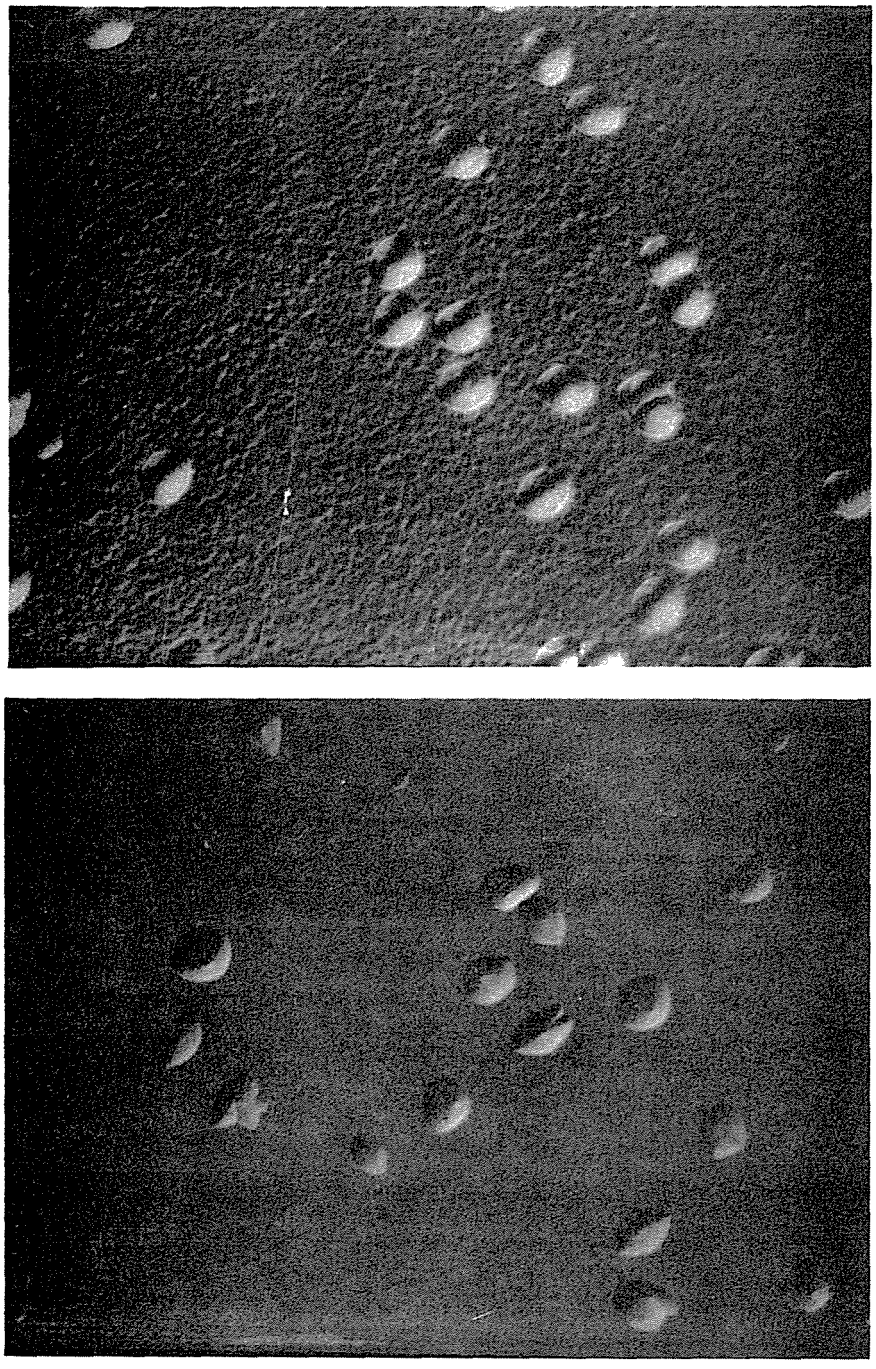


(a)



(b)

Figure 3. Etched surfacrs of the wafer shown in Figure 1
(a) center region,
(b) periphery region



(a)

(b)

Figure 4. (a) shallow etch pits observed on the wafer cut from a 3-pulled ingot.
(b) shallow etch pits observed on a S.G. wafer.

3.3 Electrical Resistivity and Carrier Mobility

Crystals pulled from the MG-Si melts are always P-type. This confirmed by chemical analysis given in Table 1 that the sum of B and Al concentration is always greater than P concentration in crystals. The electrical resistivity for the 1-pulled cyrstals is always in the range of 0.04 to 0.06 Ωcm. The resistivity in the 2-pulled and 3-pulled crystals remains at 0.06 Ωcm. However, the hole mobility measured by the van der Pauw method shows that the mobility steadily increases with the number of crystal pulls (Figure 5). Typically the hole mobility in the 1-pulled crystals is in the range of 80-90 cm^2/Vsec. The mobility was increased to 100cm^2 /Vsec for 2-pulled crystals and to 120-150 cm^2/Vsec for 3-pull crystals. However, the mobility in 3-pulled crystals is still approximately 20% lower than that of the same resistivity, semiconductor-grade crystal.

3.4 Photoresponse

3.4.1 Gated Diodes

Photoresponse of the gated diodes has been tested using an iodine quartz lamp as light source. The light intensity of the lamp is equivalent to 5×10^{-3} sun. Table 3 summarizes the average values for various crystals. The Isc of semiconductor grade crystals is only slightly higher than that of 3-pulled crystals. Among the 2-pulled crystals the wafers cut from the seed end of crystals give higher Isc's than that of the tang or middle portion of crystals.

Table 3 also shows that Voc is apparently affected by the number of crystal pulls. However, in one case the Voc of a 2-pulled crystal is as high as 3-pulled or SG crystals. The product of Isc and Voc increases with materials of the following order: tang or middle portion of 2-pulled crystals, seed end of 2-pulled crystals, 3 - pulled crystals, semiconductor grade crystals.

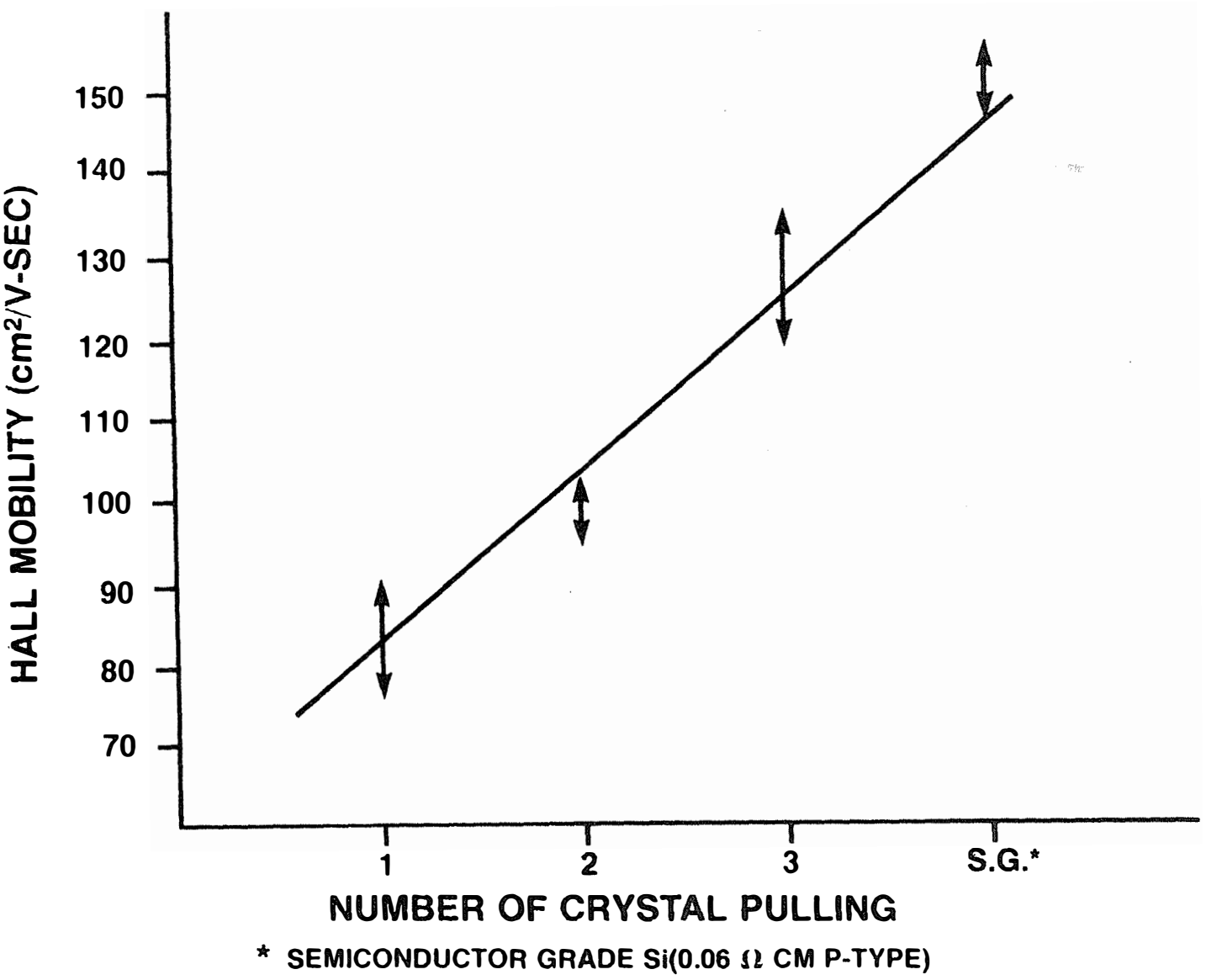


Figure 5. Plot of Hall mobility vs number of crystal pulling

TABLE 3

Average short circuit current (Isc) and open circuit voltage (Voc) for diodes illuminated under 5×10^{-3} sun

# Pull	Crystal #	Resistivity(Ω cm)	Isc(ma/cm^2)	Voc (mv)	Isc X Voc
2	6S	0.06	71.8	364	26.1
	10S	0.06	74.1	327	24.2
	10T	0.06	74.1	285	21.1
	24M	0.06	68.5	264	18.1
3	19S	0.06	93.1	359	33.4
	35	0.06	100.5	401	40.3
S.G.	15S	0.02	93.4	393	36.7
	2C	1.00	114.0	365	41.7

* stands for the seed end of crystals

** stands for the tang end of cyrstals

*** means the middle part of crystals

3.4.2 Silicon Wafers with a Shallow p-n Junction

Measurement of Isc and Voc was made on N^+ diffuused wafers of (1) 2-pulled crystals, 2) 3-pulled crystals, and 3) semiconductor grade crystals with various resistivities. One experiment used the wafers with textured surface on the front and P^+ diffused layer on the back for the reflect field. The other experiment aplied neither texturing nor back P^+ diffusion. Table 4 lists the results of the measurement for the latter one. This table shows that the improvement of 3-pulled crystals over 2-pulled crystals is primarily at Isc. It also shows that the Isc for all 3-pulled wafers is confined to the range between 17.27 to 18.09 ma/cm^2, while Voc is also confined to a narrow range from 0.592 to 0.602 volts. A wider range of variation of both Isc and Voc was observed for the semiconductor grade wafers. It is interesting to see that the semiconductor grade wafers with the same resistivity as 3-pulled crystals (i.e., 0.06 Ωcm) give almost identical Isc x Voc as those of 3- pulled crystals.

Table 5 lists the Isc and Voc values for wafers with a textured front surface and P^+ diffused back surface. It shows that considerable improvement of Isc was made over the wafers without texture and back reflect field. The semiconductor grade wafers with the same resistivity as 3-pulled crystals have only very slight higher Isc. The higher resistivity S.G. wafers, however, have much higher Isc's than that of 3-pulled cyrstals.

TABLE 4

Comparison of Isc and Voc of 2 and 3 pulled crystals with those of S.G. wafers of various resistivities (measured under AMI)

Crystal	Resistivity (Ωcm)	Isc (ma/cm^2)	Voc (V)	Isc x Voc (ma/cm^2 V)
2 pull 10S	0.06	13.6	.584	7.9
10S	0.06	14.6	.585	8.6
3 pull 35	0.056	17.65	.593	10.40
40	0.060	17.27	.598	10.33
61	0.073	17.44	.592	11.02
63	0.076	17.76	.599	10.64
67	0.075	17.72	.592	10.89
93	0.076	18.09	.602	10.89
SG* 51	0.060	18.88	.578	10.9
25	0.090	21.90	.562	12.30
05	0.50	18.71	.581	11.36
49	1.20	20.82	.566	11.75
18	8.6	23.35	.536	13.21

TABLE 5

Comparison of Isc and Voc of 3-pulled N^+ Wafers
with those of S.G. wafers of various resistivities.
(The front of wafers was textured and the back was P^+diffused.)

Crystal		Resistivity	Isc ($\frac{ma}{cm^2}$)	Voc (V)	Isc x Voc
3-pull	Mg35	0.056	25.25	.542	13.69
	Mg67	0.075	25.65	.544	13.95
SG	51	0.060	25.72	.549	14.12
	05	0.50	29.7-	.565	16.78
	49	1.20	29.03	.559	16.23
	18	18.0	31.10	.505	15.71

3.4.3 Epitaxy Wafers with a P-N Junction

Table 6 shows Isc and Voc of the N^+ diffused epitaxy layers on the various substrates. It shows that very little difference was observed from the substrates of the 2-pulled or 3-pulled cyrstals. The epitaxy layers deposited on the semiconductor grade substrate do not give a significantly better Isc and Voc than those deposited on 2-pull substrate.

3.4.4 Isc x Voc Product and Predicted Maximum Cell Efficiency

The data given in Tables 4 and 6 can be used to predict the maximum solar cell efficiency. Two assumptions were made: (1) The field factor is assumed constant (0.75). (2) 3% is added to the solar cell effficiency of both the texture surface and back reflect field are applied. Based on these assumptions, a plot of cell efficiency vs Isc x Voc was made and shown in Figure 6 for the use of various materials. The straight line indicates the linear proportionality between the cell efficiency and Isc x Voc. Three dotted loops are shown along the straight line of the plot. The loop at the lower region of the straight line consists of the data points of 2-pulled crystals. The loop at the middle region of the line consists of the data points of 3-pulled crystals. The loop at the upper region is primarily the data points of epitaxial structure or the high resistivity (0.09 cm) semiconductor grade substrates.

4. DISCUSSIONS

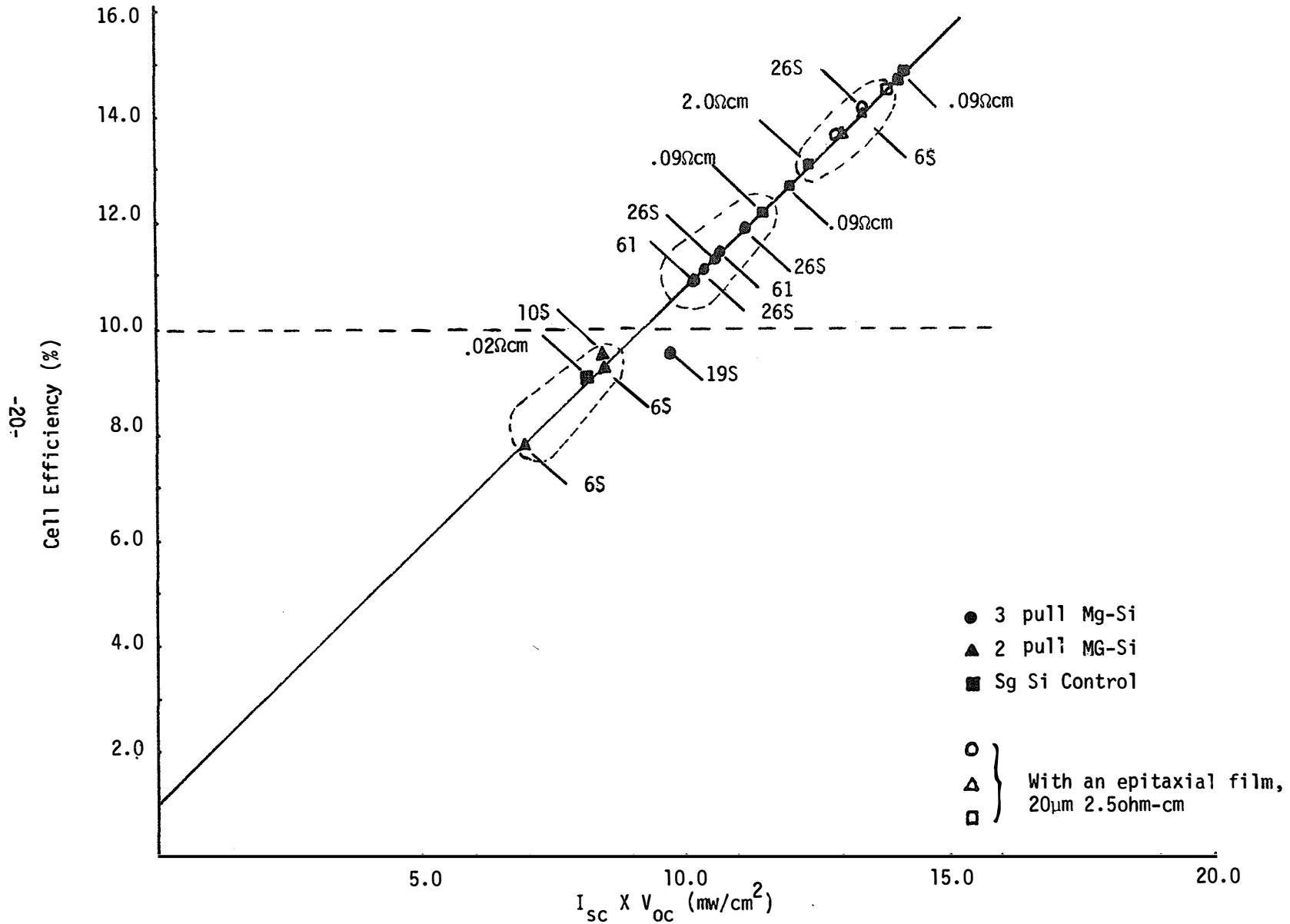
The present study has reconfirmed that the crysal pulling is an effective method of removing metallic impurities from silicon. This is clearly seen by comparing the impurity concentration in metallurgical-grade silicon with the 1-pulled crystals, or comparing the 1-pulled crystals with 2-pulled crystals.

TABLE 6

Isc and Voc of N^+ diffused wafers (2" dia.)
with an Epitaxial layer on the substrates
of various numbers of crystal pulling

Substrate	Isc(ma/cm^2)	Voc(V)	Isc Voc
2-pull 6S	22.2	.573	12.8
10S	21.7	.567	12.3
3-pull 19S	22.2	.582	13.0
26S	27.2	.566	12.6
S.G. (0.02 cm)	21.7	.599	13.0
(1.0 cm)	22.8	.559	12.7

Figure 6. Plot of cell efficiency vs I_{sc} x V_{oc} for various materials.



The slight impurity difference between the 2-pulled and 3-pulled crystals is primarily due to (1) the sensitivity of the analytical instrument, or (2) the contamination to 3-pulled crystals during the material processing. The structural and electrical characterization of the crystals confirm that the steady improvement of crystal quality by the additional crystal pulling.

The 1-pulled crystals which were used as feedstock for the second crystal pulling contain a lamellar structure at the tang end. The transition from polygonal grain structue to lamellar structure accompanies an increase in impurity concentration of 2-3 orders of magnitude[1-2]. If the portion of the lamellar structure is eliminated for use as feedstock, the purity in the 2-pulled crysals should be improved considerably. It seems likely that it may need only 2 crystal pulling steps to purify metallurgical grade silicon to semiconductor grade quality. This may not be difficult to realize since the recent separate study has developed techniques to grow large grain 1-pulled crystals with considerable extended length.

The high density shallow etch pits existed in the 2-and 3-pull cyrstals is an unique feature of this material. The shallow etch pits may be likely resulted from the impurity complexes, although the chemical and electrical data were not able to verify this speculation. The high density of the shallow etch pit lead to the dull surfaces, which can be regarded as "cosmetic defects".

The primary limitation of this process is the ineffective removal of impurities with low segregation coefficients, e.g., boron, oxygen and germanium. The presence of oxygen and germanium in silicon will not seriously affect the silicon quality. This is because both are electrically in-active and do not contribute to the deep energy levels in the bandgap. However, the existance of boron in the range of five ppm seriously limits the usage of this material to heavy-doped P-type applications.

REFERENCES

1. H.M. Liaw and Frank Secco d'Aragona, Quarterly Report, DOE/SERI-8-119-3/2 Aug. (1980).

2. Frank Secco d'Aragona, H.M. and Liaw D.M. Heminger, "Materials and New Processing Technologies for Photovoltaics" Eds. J.A. Amick, P. Rai-Chouchury, E. Sirtl, and J.P. Dismukes, Electrochem. Soc. (1981).

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